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COMMUNICATION

Low voltage and high ON/OFF ratio field-effect transistors based on CVD MoS_2 and ultra high-*k* PZT gate dielectric

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MoS_2 and other atomic-level thick layered materials have been shown with high potential for outperforming Si transistor at the scaling limit. In this work, we demonstrate a MoS_2 transistor with low voltage and high ON/OFF ratio. A record small equivalent oxide thickness of ~ 1.1 nm has been obtained by using ultra high-*k* $Pb(Zr_{0.52}Ti_{0.48})O_3$ gate dielectric. The low threshold voltage (< 0.5 V) is comparable to that of the liquid/gel gated MoS_2 transistor. The small subthreshold swing of 85.9 mV/dec, high on/off ratio of ~ 10^8 and negligible hysteresis ensure a high performance MoS_2 transistor operated at 1V. The extracted field-effect mobility of 1-10 $cm^2/V{\cdot}s$ suggests a high crystalline quality of CVD-grown MoS_2 flakes. The combination between two-dimensional layered semiconductor and ultra high-k dielectric may enable the development of low-power electronics application.

The advent of various two-dimensional layered materials, including graphene[1] and transition-metal dichalcogenides (TMD), [2] paves the way to miniaturize semiconductor devices down to a truly atomic scale.[3]As a typical member in the TMD family, MoS_2 has been demonstrated for its applications in transistors,[4] photodetecors[5] and integrated circuits (ICs).[6] Unlike the gapless graphene, single-layer MoS_2 has an ultrathin-thickness around 0.7 nm and a direct bandgap of 1.9 eV and lacks of dangling bonds. These characteristics make it quite resistant to short-channel effect and outperform the Si transistor at the scaling limit.[7, 8]

As the feature size of IC technology scales downwardly and the density of transistors increases dramatically, the power consumption of the IC continues to go up and becomes the most difficult challenge. Therefore, it is of significant importance to reduce the power consumption without comprising the device performance in other respects. First, the operation voltage V_D has to be reduced to decrease the dynamic switching power. Second, the off-state leakage current is required to be decreased to minimize the standby power.[9] Ultra high-*k* dielectrics have to be introduced to realize an equivalent oxide thickness (EOT) of less than 1 nm. However, they still retain a certain off-state leakage current.[10] Third, it requires a small sub-threshold swing (SS) to turn on the transistor with a low voltage. Fourth, the transistor should exhibit negligible hysteresis for digital computing. Up to now, some efforts have been devoted to this end by using different gate high-*k* dielectrics such as HfO_2,[4, 6] Al_2O_3,[11] and ion liquid /gel gate.[12, 13] For the high-*k* dielectrics which are formed by atomic layer deposition (ALD) technique, the absence of dangling bonds makes it very challenging to deposit uniform ultra-thin dielectrics directly on the MoS_2 layer. Surface treatment or buffer layer is usually required before the ALD process,[14-16] which degrades the quality of MoS_2 and limits the achievable minimum dielectric thickness. Theoretical simulation suggests that a low voltage of 0.5 V could be applied to MoS_2 transistor with ~ 0.5 nm EOT.[8] Until now, it has not been demonstrated experimentally yet. The ion liquid/gel gated MoS_2 transistors demonstrate good performance at a low voltage, but this technique is not suitable for small feature size devices and it is also incompatible with standard CMOS processing technology. In this study, we demonstrate field-effect transistors based on CVD synthesized MoS_2 atomic layer and ultra high-*k* $Pb(Zr_{0.52}Ti_{0.48})O_3$ (PZT) gate dielectrics. A low operation voltage of less than 1 V and a high ON/OFF ratio of ~ 10^8 have been achieved with the ultra high-*k* PZT dielectric of 100 nm thickness (~ 1.1 nm EOT).

Fig. 1(a) shows the three-dimensional schematic of the PZT gated MoS_2 transistor and Fig. 1(b) illustrates the process flow for fabricating the proposed MoS_2 transistor. For PZT preparation, we started with a 300 nm SiO_2/ Si wafer, on which a layer of Pt/Ti (100 nm/10 nm) was sputtered as the bottom gate material and also the seed layer for PZT deposition. Then a layer of ~100 nm PZT film was prepared by radio frequency sputtering method using a ceramic target. As-prepared PZT was then annealed at 650 °C in N_2/O_2=1:1 atmosphere for 1 min by rapid thermal annealing. Fig. 2(a) shows the XRD patterns of the annealed PZT thin film. The film clearly exhibits polycrystalline perovskite structures, with its typical crystal orientation annotated in Fig. 2 (a). Mechanically exfoliated single-layer or few-layer MoS_2 flakes have very limited sizes for practical applications, although

they usually exhibit better crystal quality. Recently, CVD has been largely explored to synthesize large-area, layer-controlled crystalline MoS_2 flakes,[17-24] making MoS_2 a promising semiconducting channel material for the field-effect transistors to extend CMOS to the end of the roadmap. In this work, single-layer MoS_2 was grown by direct vapor phase reaction method using a setup similar to that reported in Ref 21. The synthesized MoS_2 flakes were transferred onto PZT substrate by conventional PMMA-mediated method. The source/drain electrodes were patterned onto the final substrate using conventional photolithography followed by Au/Ti (100 nm/ 10 nm) evaporation and lift-off processes. Fig. S1 shows one typical device after the electrode formation.

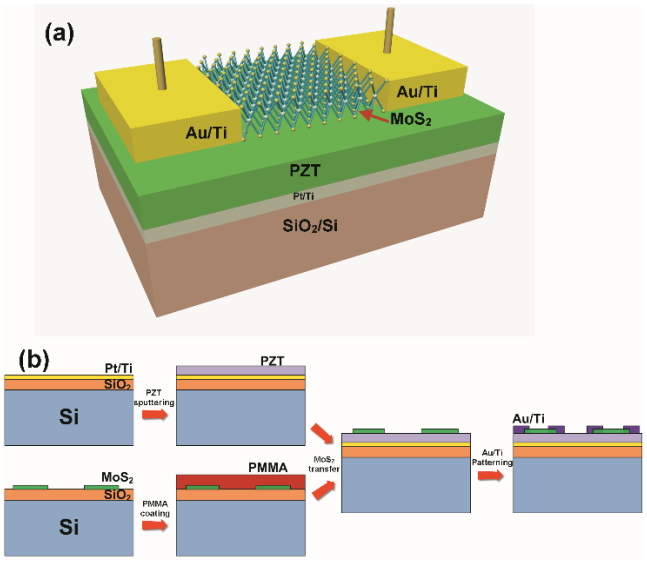

Fig. 1 (a) Schematic structure of the PZT gated MoS_2 transistor (not to scale); (b) Process flow for fabricating the proposed MoS_2 transistors.

Fig. 3(a) and Fig. 3(b) show typical optical images of the transferred MoS_2 flakes on the SiO_2 and PZT substrate, respectively. The triangular shape of the MoS_2 flakes can be clearly identified in Fig. 3 (a), while it is not so apparent in Fig. 3(b) due to the poor optical contrast of the PZT substrate. The typical size of the MoS_2 flakes is ~ 20 µm, measured as the side length of the triangular (See also Fig. S1). It is shown that these triangular flakes could merge into a single flake or even a continuous film if the growth time is long enough, as also reported in Ref. 21. Raman spectrum of the MoS_2 flake is presented in Fig. 3(c). There are two active Raman modes, with their peak frequencies located at 384.7 cm^{-1} and 404.6 cm^{-1}, respectively. The E′ mode results from the in-plane vibration of the two S atoms with respect to the Mo atom and the A_1 mode results from the out-of-plane vibration of the two S atoms in opposite directions. The difference between the two peak frequencies is used as a convenient indicator to determine the layers of the MoS_2 sample. [25, 26] In this work, the peak difference is usually less than 20 cm^{-1}, suggesting that the synthesized MoS_2 flakes are monolayers.[20, 25] The full width at half maximum (FWHM) of the peak is ~ 3 cm^{-1}, which is comparable with the mechanical exfoliated monolayer MoS_2, indicating a high crystalline quality of the synthesized sample.[20] The photoluminescence (PL) spectra show two peaks at ~625 nm (1.98 eV) and 673 nm (1.84 eV), corresponding to the B1 and A1 direct excitonic transition, respectively. The prominent intensity of A1 peak is attributed to the gap transition at the K point of the Brillouin zone in monolayer MoS_2.[27] The thickness of the MoS_2 flake is about 7 Å as measured by atomic force microscopy (Fig. 3(e) and (f)), also confirming its single-layer characteristic.

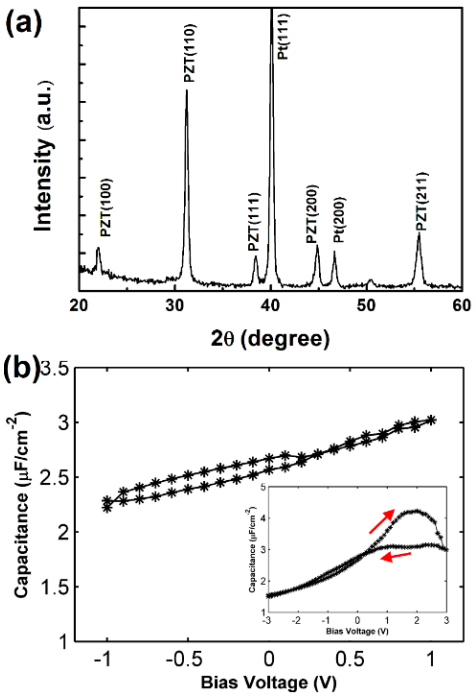

Fig. 2 (a) X-ray diffraction spectrum of the annealed PZT thin film. (b) Capacitance-voltage characteristic of the PZT thin film. Inset shows the measurement results under a larger sweeping voltage (3V) and the arrows indicate the sweeping directions.

With the relatively large area of transferred MoS_2 flakes, it is quite convenient to fabricate multiple devices without resorting to the costly electron beam lithography. In this work, we have successfully fabricated MoS_2 transistors with channel lengths ranging from 1.5 µm to 4 µm. The current-voltage characteristics were measured by B1500 system under vacuum ambient (pressure lower than 10^{-6} Torr) using a Lakeshore TTPX cryogenic probe station. Fig. 4(a) presents the transfer characteristic of a transistor with 1.5 µm channel length and nominal 20 µm channel width. The device shows clearly switching characteristics in the scanned gate voltage range of -1 V to 1V under various drain-source voltages (V_d). The low voltage characteristic is attributed to the small EOT (~ 1 nm).

Fig. 4(b) illustrates the transfer characteristic of the transistor under V_d=0.6 V. The inverse slope of the red straight line in Fig. 4(b) represents the SS of the device. A small SS of 85.9 mV/dec is obtained, which is comparable to recently reported top-gate or dual-gate MoS_2 transistors[4, 11] based on ALD high-*k* dielectrics and mechanically exfoliated MoS_2 flakes. It is shown in Fig. 4(b) that the OFF-state current near V_g=0 V is less than 10^{-13} A and the on current is ~ 10^{-5} A. Thus a high ON/OFF ratio of ~10^8 is achieved, which is also comparable to the best results reported for mechanically exfoliated devices. We have used the extrapolation in the linear region method to extract the threshold voltage (V_T).[28]

In the linear region, the channel current I_{ds} is in linear proportional to V_g as expressed by $I_{ds} \propto (V_g - V_T - V_d/2)$.

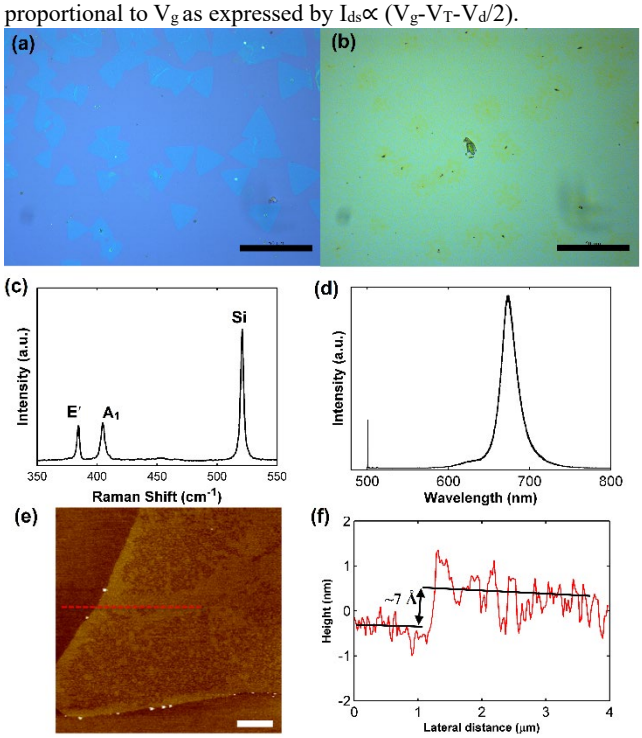

Fig. 3 Optical image of the transferred MoS_2 flakes onto (a) SiO_2/Si substrate and (b) PZT substrate; Scale bars 50 μm for (a) and (b). (c) Typical Raman spectrum of the synthesized MoS_2 flake. E′ and A_1 denote the in-plane and out-of-plane vibration modes of the sulfur atoms. (d) Photoluminescence spectrum of the MoS_2 flake. The laser wavelength for Raman and PL measurement is 488 nm. (e) Atomic force microscope image of a MoS_2 flake on the SiO_2 substrate, scale bar 1μm. (f) Cross-section plot of the MoS_2 flake along the red dashed line in (e).

By finding the V_g axis intercept of the linear extrapolation of the I_{ds}-V_g curve at the maximum slope point, and the value of V_T is calculated by subtracting $V_d/2$ from the intercept value. For this device, the V_T is about 0.37 V, as indicated in Fig. 4 (c). It is noticed that the slope (transconductance) starts decrease toward saturation at a low drain bias of 0.1 V, as shown in Fig. 4(c). While this saturation phenomena are not observed when the drain bias is slightly larger, the velocity saturation effect could be excluded as a contribution. Considering the relatively large as-obtained contact resistances at the source/drain terminals and the well-studied crowding effect in kinds of thin film transistors, it is most likely that the slope saturation is due to the low bias current crowding effect Fig. 4 (d) shows the output characteristics of the device. The drain-source current I_{ds} exhibits clearly saturation behavior at a low drain voltage, suggesting the good control of the carrier transport by the gate voltage. It is noteworthy that the present device is a normally-off n-channel transistor. As a switching device, normally-off behavior is desirable for low-power electronics. However, this behavior was not observed for many reported MoS_2 transistors. [4, 6, 11, 18, 21] In the present study, the Pt gate has a higher work function (Φ_m) than Ti, Cr and Al which were used as the adhesive layer in direct contact with the gate dielectrics. We explain the observed normally-off behavior in terms of energy band diagrams. The single-layer MoS_2 has a bandgap of 1.84 eV, as suggested by the PL measurement, and the work function (Φ_{MoS2}) is assumed as ~ 4.9 eV and the electron affinity is 4 eV.[29] Assuming the bulk value of the work function for the bottom gate (Φ_m=5.6 eV), the band diagram at equilibrium suggests the carrier depletion at zero gate bias, as shown in Fig. 4(e). Thus the device is maintained at OFF state at zero gate bias and negative gate bias. When the applied positive gate voltage increases, the MoS_2 band diagram will evolves from the depletion region to the accumulation region and the device is biased at ON state. Similarly, it is reported that a bilayer MoS_2 transistor could be changed from depletion mode to enhance mode by replacing the Al gate with Pd gate. [6]

The field-effect mobility is derived using the expression $\mu = [\Delta I_{ds}/\Delta V_g] \times [L/(WC_iV_d)]$, where L and W are the channel length and width, respectively, and C_i is the capacitance per area. We made a test structure of metal-PZT-metal capacitor to measure C_i. Unlike commonly used dielectrics such as SiO_2 or HfO_2, the PZT dielectric shows clearly voltage-dependent capacitances, as shown in Fig. 2(b). The relative dielectric constant of the PZT dielectric is calculated to be in the range of 250-350, with the maximum value obtained under the largest positive voltage bias. The mobility of the MoS_2 transistor is around 1.39-1.88 $cm^2/V{\cdot}s$, estimated using the maximum and minimum capacitance, respectively. Using the same method, we have calculated the mobility for multiple devices on the same substrate. Fig. S2-S4 present the transfer characteristics with different channel dimensions, in which a high mobility of 10.01 is achieved for a device with 2 μm channel length (Fig. S2). Generally, the mobility is in the range of 1-10 $cm^2/V{\cdot}s$ and the threshold voltage is about 0.2-0.4 V. These results suggest the high quality of the CVD MoS_2 flakes and the applicability of the proposed PZT dielectric MoS_2 transistors for low voltage electronics. Considering the device working at 1 V bias, a dielectric constant of ~350 is obtained and the EOT is ~ 1.1 nm. This EOT is the smallest value among the MoS_2 transistors in the existing literatures. This level of low voltage operation has only been reported in ion liquid/gel gated MoS_2 transistors.

It is well known that the interdiffusion between silicon and PZT constrains the reliability of PZT ferroelectric transistor. The interdiffusion happens because the PZT is deposited on the Si substrate and the Pb diffuses into the silicon at a high temperature which is used for crystallization of the PZT. In this study, the MoS_2 flakes were transferred onto the polycrystalline PZT film and no high-temperature processes were used after the transfer process. This is in distinct to the interface of the traditional structure consisting of PZT and bulk semiconductor material. The interface trap density could be evaluated using the equation:The interface trap density could be evaluated using the equation:

$$D_{it} = \frac{C_i}{q^2}\left(\frac{q \cdot SS}{KT \ln 10} - 1\right) \quad (1)$$

Using the measured data of C_i (2.2 ~ 3 μF/cm^2) and SS (85.9 mV/dec), the trap density at room temperature (T=300 K) is estimated as 6.3~ 8.6 $\times 10^{12}$ /cm^2 • eV. The interface traps between atomic-level-thick semiconductor and substrate is a common problem for the 2D based electronics. These interface traps are possibly resulted from the transfer process of 2D layered materials or the atomic-level roughness of the substrate. To further improve the interface, researchers have developed new transfer process like dry-transfer process to avoid the potential chemical contamination during the PMMA-mitigated transfer

process.

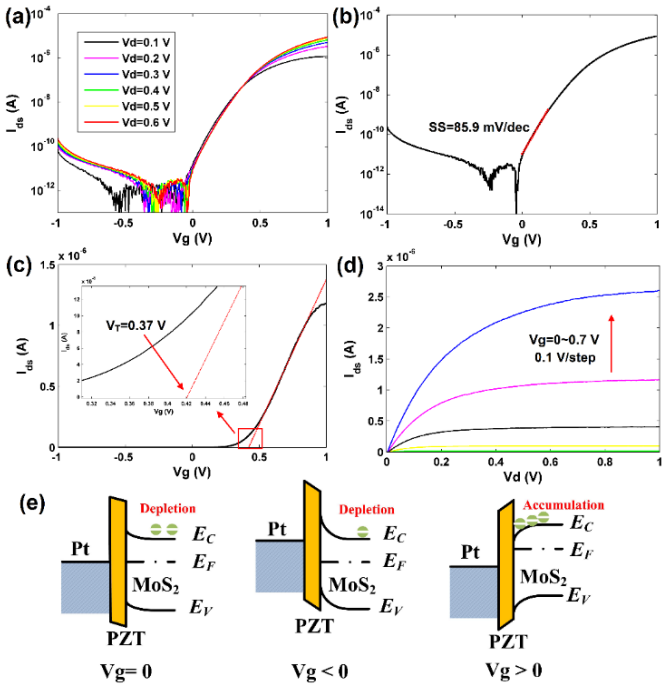

Fig. 4 Electrical characteristics of the PZT gated MoS_2 transistors with 1.5 μm channel length and 20 μm nominal channel width. (a) Transfer characteristics of the MoS_2 transistors with various V_d ranging from 0.1 V to 0.6 V. (b) Extraction of the subthreshold swing (SS) from the transfer characteristics at V_d=0.6 V, the SS is about 85.9 mV/dec for this device. (c) Extrapolation method to obtain the threshold voltage, which is 0.37 V. (d) Output characteristics of the MoS_2 transistor. The device shows good saturation properties. (e) Energy-band diagrams for the Pt/PZT/MoS_2 structures under different bias.

It is known that PZT thin film has been widely studied for the applications, including ferroelectric memory,[30] micromechanical systems[31] and high-density integrated capacitors.[32] The ferroelectric hysteresis of the PZT thin film with ~ 100 nm thickness appears when a large sweeping voltage (3 V) is used (See inset of Fig 2(b)), indicating the relatively large coercive field of the PZT film. It is well known that the coercive field of ferroelectric thin film with 100 nm thickness is much larger than that in micrometer range. [30] If we consider the inactive layer near the electrode interface, this value could be even larger. For the present PZT thin film, the coercive field is larger than 10^7 V/m. Also, it shows asymmetric gating effect which is mainly due to the difference of the top electrode (Au/Ti) and bottom electrode (Pt/Ti) in terms of material and also thermal processing, because the bottom electrode endured a high temperature process when the PZT was annealed. While sweeping with a large voltage can induce the ferroelectric memory effect, the gate current is relatively larger especially when the gate is biased at a large positive voltage. With a smaller sweeping range, PZT can be regarded as a dielectric material with a limited hysteresis and an ultra-high dielectric constant. In this study, we conducted the gate voltage sweep within 1 V, thus both the leakage current and the capacitance hysteresis has been reduced.

Fig. 5(a) shows the hysteresis behavior of the transfer characteristics. For normally operational PZT gated MoS_2 transistors, the hysteresis is ~ 0.01 V, which is only 1% of the sweeping range. The performance is very remarkable considering the usually reported large hysteresis in MoS_2 transistors even with dielectric encapsulation process.[33] Since the measurement is conducted in vacuum, we can exclude the effect due to the absorption of the oxygen/water molecules. There are two origins of the hysteresis. First, the defects of the MoS_2 formed during the growth or the transfer process can give rise to a large hysteresis. We fabricated and measured the MoS_2 transistor using the 300 nm SiO_2 as the gate dielectric. The device also shows very small hysteresis (See Fig. S5, S6). This suggests that the MoS_2 itself has very limited defects density. Second, as a typical oxide ferroelectric material, the polycrystalline PZT is usually oxygen deficient.[30] In the regions near the interface, there are more oxygen deficiencies than in the bulk. Oxygen vacancies act as electron traps when the MoS_2 is biased at a positive voltage, thus induces the clockwise hysteresis of the transfer curves. Furthermore, we have characterized the device under a low temperature of 150 K. The MoS_2 transistor shows hysteresis-free transfer characteristics, as indicated in Fig. 5(b). The resultant hysteresis-free behavior suggests that highly mobile oxygen vacancies don't come into play at a low temperature and the density of the surface traps is very small at room temperature.

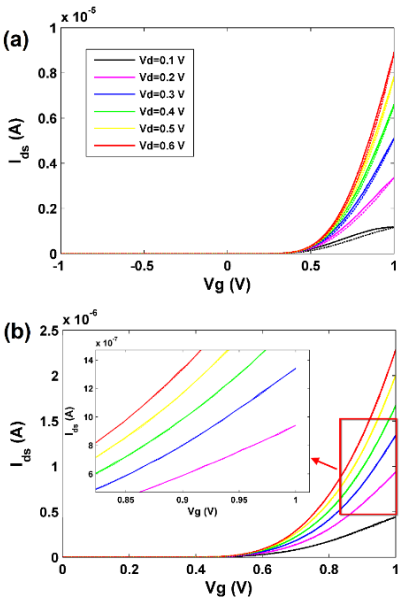

Fig. 5 Hysteresis characteristics of the MoS_2 transistors measured at (a) 300 K and (b) 150 K. The dashed lines show the backward sweeping results and the inset shows the magnified figure of the right part indicated by the red arrow.

In summary, we presented the MoS_2 transistors with a low voltage of 1 V and a high on/off ratio of ~ 10^8 by combing the ultra high-*k* PZT dielectric and CVD MoS_2 flakes. The features of the low threshold voltage (< 0.5 V), small SS (85.9 mV/dec), and the normally-off characteristic suggest the high potential of the proposed device for low power digital circuit applications. The small hysteresis indicates the high quality of the CVD synthesized MoS_2 flakes and the clean interface between the MoS_2 and PZT. The record small EOT obtained with ~ 100 nm PZT could be scaled down for even smaller voltage operation,

either by decreasing the PZT thickness or increasing the dielectric constant with the optimization of the PZT deposition process.

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