Design of a 1 kW PFC Power Supply Based on Reduced Redundant Power Processing Principle

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Abstract— **This paper presents a single phase power factor correction (PFC) power supply topology based on a non-cascading connection of a current-fed full-bridge converter and a buck-boost converter, both converters being operated in continuous conduction mode (CCM). Due to the reduced redundant processing of power, the non-cascading structure can inherently achieve a higher overall efficiency compared to the classical two-stage cascade structure. An analysis of the reduced redundant power processing (R^2P^2) principle is given and the associated practical problems discussed. Experimental results verify the effectiveness of the non-cascading structure of the proposed topology as an appropriate solution for increasing the overall efficiency.**

I. Introduction

Power factor correction (PFC) and tight output voltage regulation are the essential requirements of ac-dc power supplies that derive power directly from the ac mains [1]–[2]. In general, such a power supply contains two basic converters and a low-frequency (100 Hz or 120 Hz) energy storage element. It usually consists of a PFC pre-regulator for input current shaping and a voltage regulator for producing the desired output voltage. The energy storage element is a necessary component in any PFC power supply, as it serves as the buffer for maintaining power balance between the input and output powers. Fig. 1 shows a power flow diagram that describes the power processing of the classical two-stage PFC power supply. Since the input power is processed by the pre-regulator and the voltage regulator serially, the overall efficiency is degraded.

To solve this efficiency problem, non-cascading structures have been proposed for ac-dc power supplies [3]–[7]. Unlike the classical approach, these ac-dc power supplies allow part of the input power to be processed by only one power stage, thereby reducing the amount of power redundantly processed by the two constituent power stages. The power flow diagram of the proposed power supply is shown in Fig. 2. Based on the reduced redundant power processing (R^2P^2) principle, 15 configurations of non-cascading structures can be developed using a power flow consideration [8],[9]. The power supply proposed in this paper belongs to Type I-IIIB configuration of [8]. Similar non-cascading structures have also been reported elsewhere [10]. Our objective in this paper is to apply the R^2P^2 principle for designing a 1 kW non-cascading ac-dc PFC power supply. The system consists of a current-fed full-bridge converter which serves as the PFC pre-regulator and a buck-boost converter which acts as the voltage regulator. Both converters operate in continuous-conduction-mode (CCM) for high power applications and are controlled separately. The prototype has been constructed for verification purposes. Our aim is to show the improved overall efficiency in comparison with the classical approach, as well as the low harmonic input current characteristic and tight output voltage regulation.

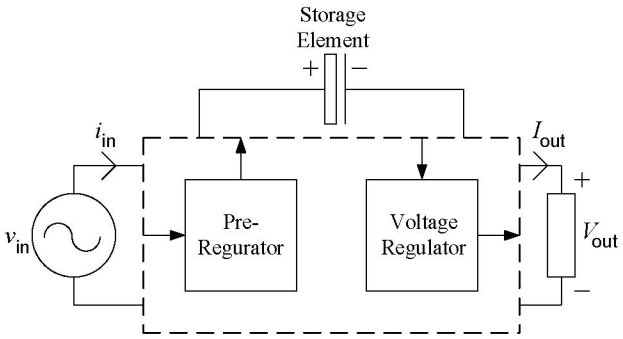

Fig. 1. Power flow diagram for classical PFC power supply

Section II details the theoretical analysis of an ideal non-cascading structure for ac-dc power supply using the R^2P^2 principle. Section III presents some practical problems related to circuit implementation of the power supply including the value of the storage element and the conversion ratio of the pre-regulator. In Section IV, some experimental results under various operating conditions will be given. Finally, a conclusion is given in Section V.

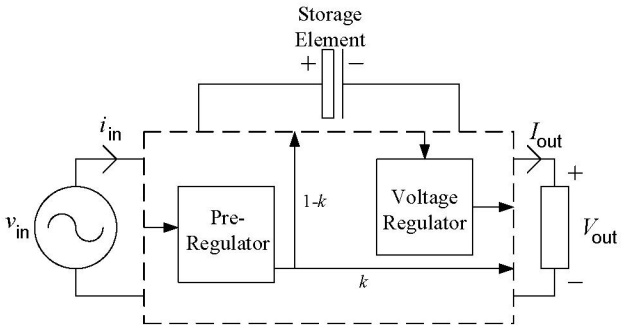

Fig. 2. Power flow diagram for the proposed power supply.

II. Theoretical Analysis Using R^2P^2 Principle

A. The Proposed Power Supply Topology

The schematic diagram of the proposed power supply, consisting a non-cascade connection of a current-fed full-bridge converter and a buck-boost converter, is shown in Fig. 3. To maintain power balance, a low-frequency storage element is required to buffer the difference between the instantaneous input power and output power. Capacitor C_B serves as the storage element and is connected in series with C_o. The series combination forms the loading for the current-fed full-bridge converter. Therefore a portion of the output energy from the converter is transferred directly to the output because C_o is in parallel with the load. The voltage of C_o should be free of

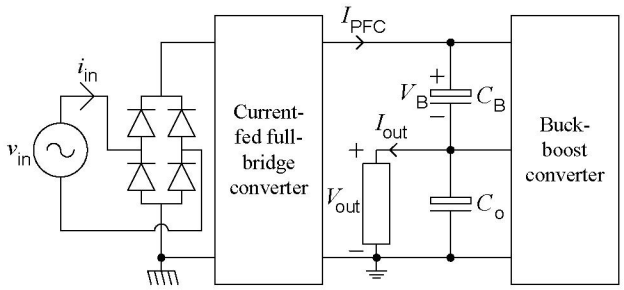

Fig. 3. The proposed power supply schematic diagram.

low-frequency voltage ripple because it is the actual output of the whole power supply. On the other hand, $C_{\rm B}$ has a low-frequency ripple voltage. The buck-boost converter takes energy from $C_{\rm B}$ and delivers the energy to the load.

B. Efficiency Gain

The efficiency of the classical power supply can be represented by

$$\eta_{\rm classical} = \eta_{\rm C1}\eta_{\rm C2}, \tag{1}$$

where $\eta_{\rm C1}$ and $\eta_{\rm C2}$ are the efficiency of the pre-regulator and the voltage regulator, respectively, of the classical power supply.

For achieving PFC and voltage regulation, it is indeed not necessary to process all the input power by both converters because part of the input power can go directly to the load through only one converter. The theoretical efficiency of the proposed power supply can be evaluated by followed equations,

$$\begin{aligned}\eta_{\rm proposed} &= (1-k)\eta_{\rm P1}\eta_{\rm P2} + k\eta_{\rm P1} \\ &= \eta_{\rm P1}\eta_{\rm P2} + k\eta_{\rm P1}(1-\eta_{\rm P2}),\end{aligned} \tag{2}$$

where $\eta_{\rm P1}$ and $\eta_{\rm P2}$ are the efficiencies of the pre-regulator and the voltage regulator, respectively, and k is the ratio at which the amount of the input power is split at the output of the pre-regulator to the output load. The efficiency gain of the proposed power supply is $k\eta_{\rm P1}(1-\eta_{\rm P2})$. Obviously, the pre-regulator efficiency is influential to the overall efficiency of the proposed power supply, because the total input power from the ac mains must be processed by the pre-regulator before it is transferred to the load or the voltage regulator.

Comparison of these two power supplies is made on the basis of the converters efficiency. Assuming that the overall efficiency of these two power supplies are equal. The total input power of the power supplies are processed by its pre-regulators. By using (1) and (2), and assuming that $\eta_{\rm C1} = \eta_{\rm P1}$, we get

$$\eta_{\rm C2} = \eta_{\rm P2} + k(1-\eta_{\rm P2}). \tag{3}$$

Clearly, the classical approach can provide a higher overall efficiency of the proposed power supply, only when $\eta_{\rm C2} > \eta_{\rm P2} + k(1-\eta_{\rm P2})$.

C. Factor k in Terms of Circuit Parameters

In the proposed power supply, the factor k affects the efficiency gain and the load dynamic response. The total current harmonic distortion is independent of this factor, due to the input current being fully processed by the PFC pre-regulator. It will be useful if the factor k can be determined in terms of the circuit parameters of the proposed power supply. Referring to Figs. 2 and 3, we can write

$$P_{\rm PFC} = I_{\rm PFC}(V_{\rm B} + V_{\rm out}) \tag{4}$$

$$P_{\rm direct} = I_{\rm PFC}V_{\rm out} \tag{5}$$

From (4) and (5), we have

$$P_{\rm direct} = \frac{V_{\rm out}}{V_{\rm B}+V_{\rm out}}P_{\rm PFC}, \tag{6}$$

where $P_{\rm PFC}$ and $I_{\rm PFC}$ are the output power and the output current of the current-fed full-bridge converter and $P_{\rm direct}$ denotes the amount of output power of the converter directly transferred to the load. Therefore, the factor k can be determined by

$$k = \frac{V_{\rm out}}{V_{\rm B}+V_{\rm out}}. \tag{7}$$

To improve the overall efficiency, it is clear that the factor k should be made as large as possible. On the other hand, the factor k should be kept small enough such that the buck-boost converter can provide fast output voltage transient response.

III. Circuit Overview

A. Value of the Storage Element

The storage element plays an important role in ac-dc PFC power supplies. For a constant load with output power of $P_{\rm out}$, the power drawn from the ac mains has a value of $P_{\rm out}(1-\sin 2\omega t)$ for ideal active power factor correction. The minimum stored energy necessary for unity-power-factor operation is the difference between the energy consumed by the constant-power load and the energy delivered by the ac mains during one-quarter of its period $\frac{\pi}{2\omega}$ starting with zero energy.

The energy consumed by the load during $0<t<\frac{\pi}{2\omega}$ is

$$E_{\rm dc} = P_{\rm out}\frac{\pi}{2\omega}, \tag{8}$$

where ω is the frequency of the ac mains. The energy delivered by the ac mains during $0<t<\frac{\pi}{2\omega}$ is

$$E_{\rm ac} = \int_0^{\frac{\pi}{2\omega}} P_{\rm out}(1-\sin 2\omega t)dt = P_{\rm out}(\frac{\pi}{2\omega} - \frac{1}{\omega}). \tag{9}$$

The minimum stored energy of the storage element is the difference between the two energies,

$$E_{\rm C_s min} = E_{\rm dc} - E_{\rm ac} = \frac{P_{\rm out}}{\omega}. \tag{10}$$

If the storage element is a capacitor $C_{\rm s}$, the energy stored in the capacitor is

$$E_{\rm C_s} = \frac{1}{2}C_{\rm s}({v_{\rm C_s}}^2_{\rm max} - {v_{\rm C_s}}^2_{\rm min}) = C_{\rm s}V_{\rm C_s}|\Delta v_{\rm C_s}|, \tag{11}$$

where $V_{\rm C_s}$ is the static value of $v_{\rm C_s}$, and $|\Delta v_{\rm C_s}|$ is the peak-to-peak variation of the $v_{\rm C_s}$. Using (10) and (11), we get

$$|\Delta v_{\rm C_s}| = \frac{P_{\rm out}}{\omega C_{\rm s}V_{\rm C_s}}. \tag{12}$$

Therefore, the amount of ripple voltage can be reduced by using a large capacitor under a high static stress.

In the case of the classical ac-dc power supplies with PFC, for maintaining the unity-power-factor operation, the minimum capacitance can be obtained if the capacitor voltage is allowed to vary from zero to its peak value during each half of the ac mains period, i.e., $|\Delta v_{C_s}| = 2V_{C_s}$. The resulting minimum capacitance is

$$C_{s_{min}} = \frac{2P_{out}}{\omega |\Delta v_{C_s}|^2}. \tag{13}$$

In the case of the proposed power supply, for maintaining unity-power-factor operation, the minimum capacitance can be obtained if the output voltage of the current-fed full-bridge converter is allowed to vary from V_{out} to its peak value during each half of the ac mains period because the output voltage of the converter must contain a dc voltage which is larger or equal to the output voltage. The maximum ripple voltage of the storage element capacitor in the proposed power supply is equal to $2V_B$. Using (12), the required minimum capacitance for energy storage is

$$C_{B_{min}} = \frac{P_{out}}{2\omega V_B (V_B + V_{out})}. \tag{14}$$

In general, the capacitance of the proposed power supply requires a larger value than that of the classical power supplies because the allowable voltage ripple Δv_{C_s} is usually kept at a smaller value; otherwise a large variation in the duty cycle of the buck-boost converter is required. However capacitor C_B clearly enjoys a lower voltage stress when compared with that of the classical power supplies.

B. Pre-Regulator Stage

Isolated boost type converters used for PFC at high-power applications are reported recently by [4], [11]–[13]. A current-fed full-bridge converter is chosen as the PFC pre-regulator for the proposed power supply because its input current can be fully controlled for achieving the required PFC action. Furthermore, the converter can offer a number of additional advantages, e.g., the size and the cost of the input boost inductor can be reduced due to its frequency-doubling effect; its transformer provides galvanic isolation and step-down output voltage for reducing the voltage rating of the bulk capacitor, the energy storage element. In terms of transformer core utilization, the current-fed full-bridge converter clearly provides better performance than that of flyback and forward converters. However, the leakage inductance of the transformer generates high voltage spikes on the power switches, when the switches are turned off. A simple method to suppress the voltage spikes is by using a passive or active snubber circuit at the expense of power loss penalty.

The simplified circuit of the current-fed full-bridge converter is shown in Fig. 4 (a). The set of waveforms that relate the ideal gate timing with the corresponding inductor current and transformer voltage is shown in Fig. 4 (b). It is easy to see that the operation of this converter resembles that of a typical boost converter. Energizing intervals of L_i begin at the time when both S_1 and S_2, or S_3 and S_4 are turned on. De-energizing intervals of L_i begin at the time when both S_1 and S_4, or S_2 and S_3 are turned on. The input energy is stored in L_i in the energizing intervals, and released through the

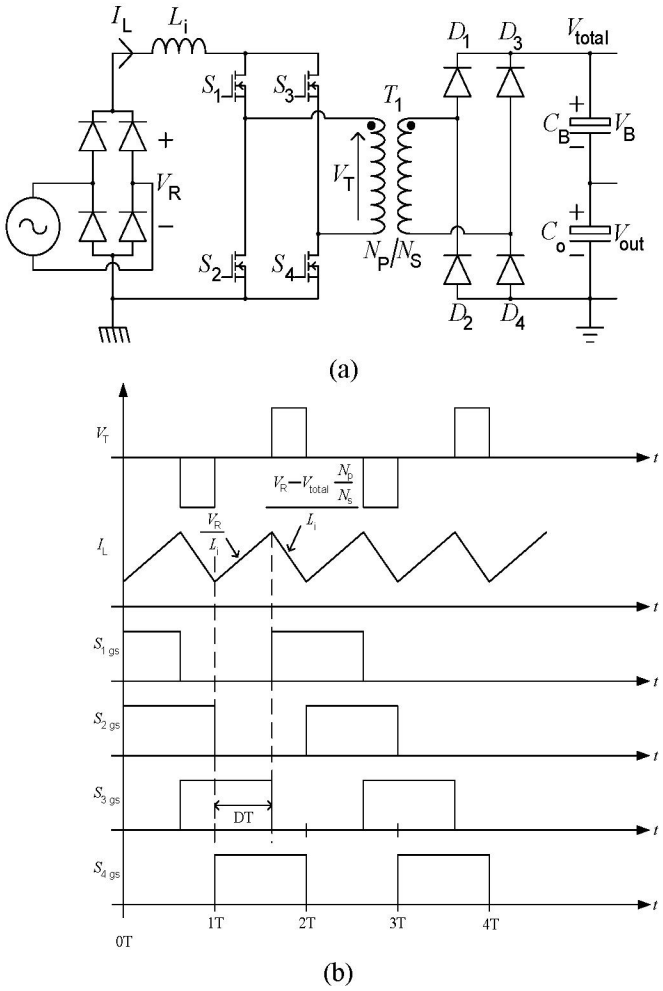

Fig. 4. Current-fed full-bridge converter. (a) Simplified circuit and (b) gate timing diagram with corresponding waveforms.

transformer T_1 in the de-energizing intervals. The conversion ratio is controlled by the phase difference between S_1 and S_2. It can be easily derived by applying the principle of volt-second balance to the inductor current waveform, i.e.,

$$\frac{V_R}{L_i} DT = -\left(\frac{V_R - V_{total}\frac{N_p}{N_s}}{L_i}\right)(1-D)T \tag{15}$$

Thus, the conversion ratio is

$$\frac{V_{total}}{V_R} = \frac{N_s}{N_p}\frac{1}{(1-D)} \tag{16}$$

which is similar to that of a typical boost converter conversion ratio with an additional factor of $\frac{N_s}{N_p}$ due to the transformer turns ratio. This phase shift control resulted in the zero voltage switching at S_2 and S_4, and the zero current switching at S_1 and S_3.

C. Voltage Regulator Stage

Based on the description in Section II, the voltage regulator processes only part of the total output power, therefore its power rating is always less than the total output power. It is certainly not necessary to design the voltage regulator for serving the total output power. Clearly the size of the voltage regulator can be minimized and the component current

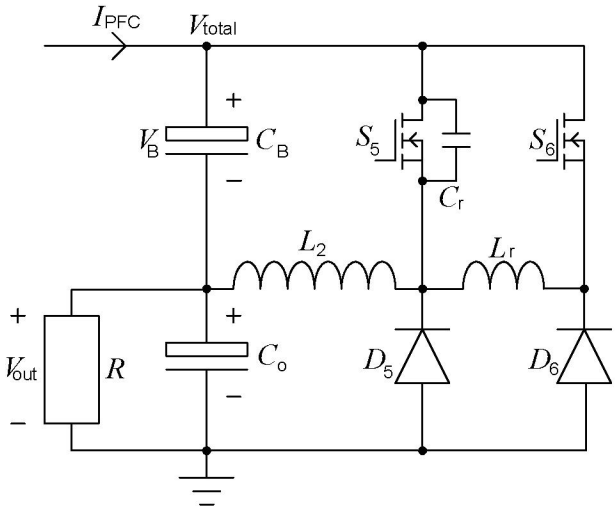

Fig. 5. Simplified schematic circuit of buck-boost converter using ZVT technique.

ratings are lower in comparison with those of its classical counterparts. The buck-boost converter and the Ćuk converter are suitable as the voltage regulator because, in this non-cascading configuration, the negative of its input terminal must be connected to the positive of its output terminal according to Fig. 3. The buck-boost converter is chosen because the control circuit design for buck-boost converter is simpler than for the Ćuk converter. In [9] a detailed discussion is provided on the synthesis of converters for the proposed power supplies with various topological arrangements.

However, the buck-boost converter is still required to process part of the output power depending on the value of k. A high value of k keeps the duty cycle of the converter at a large value. The controller of the converter provides only a narrow headroom for changing the duty cycle, and high values of k imply that only small amount of the output power is controlled by the fast feedback loop of the controller for responding a fast load transient. Therefore, in practice, 0.44 is an appropriate value of k for optimizing the performances between the overall efficiency and the fast load transient response. As result, the output power of the converter is around 560 W. Hence, the converter employs a zero-voltage-transition (ZVT) technique [14]. The voltage stress of this buck-boost converter's switching devices are clamped and the voltage stress is V_B+V_{out}. The simplified voltage regulator is shown in Fig. 5. The basic components of the buck-boost converter are S_5, D_5, and L_2. The ZVT is achieved by an auxiliary switch, S_6, a power diode, D_6, and a resonant network, which consists of L_r and C_r. This technique can provide zero voltage switching in S_5, and also reduce power loss in D_5 due to a longer reverse recovery time.

IV. Experimental Verification

A. Implementation

A laboratory prototype based on the proposed topology has been constructed to meet the following major design specifications: the input voltage is 180 V_{ac}, the voltage of the energy storage element is 70 V_{dc}, the output voltage is 56 V_{dc}, the output power is 1 kW, and the switching frequency for both regulators is 50 kHz. The lists of components of the pre-regulator and voltage regulator are shown in Tables I and II, respectively. Fig. 6 shows the implemented schematic diagram of the proposed PFC power supply with the control circuitries. Two passive snubber circuits are added in the primary side to suppress the primary switches voltage stress. In the voltage regulator, for preventing the parasitic ringing between L_r and the output capacitor of S_6, two diodes, D_7 and D_8, are added. A turn-off snubber circuit is also attached in the secondary side power switch, S_5, to clamp the voltage stress.

TABLE I
Components and their values/types for the current-fed full-bridge converter.

Parameters	Components/Values
L_{in}	500 μH
BR_1	20ETF10 X 4
S_1, S_2, S_3, S_4	IXFK 27N80
D_1, D_2, D_3, D_4	DESP 30-03A
Transformer	
Core	ETD 54 Philips 3C90
Magnetizing Inductance	18 mH
Leakage Inductance at Primary Side	9.4 μH
Primary Winding	58 T
Secondary Winding	21 T
C_{S1}, C_{S2}	4.7 nF 2 kV
R_{S1}, R_{S2}	100 Ω 25 W
D_{S1}, D_{S2}	MUR4100

TABLE II
Components and their values/types for the buck-boost converter.

Parameters	Components/Values
S_5	IXFK73N30
S_6	IXFK48N50
D_5	APT30D30
D_6, D_7, D_8	BYV29-400
L_2	100 μH
L_r	10 μH
C_B	2700 μF × 5 160 V
C_o	680 μF × 4 100 V
C_r	2.2 nF 630 V
C_{S3}	2 nF 1 kV
R_{S3}	360 Ω 2 W
D_{S3}	MUR460

Average current mode control based on the PFC controller UC3854A is employed to control the current-fed full-bridge converter. There are four active switches, which have to be controlled for realizing the PFC function. Thus, additional logic circuits are required to generate the required gating pulses according to Fig. 4 (b). Peak current mode control based on UC3842 is employed in the buck-boost converter for providing the voltage regulation and the output power limitation. The gate signal of the auxiliary switch for ZVT operation is attained by a voltage comparator with a simple logic circuit.

B. Experimental Results

In this section we attempt to demonstrate the advantages of the proposed power supply experimentally. Fig. 7 shows the efficiency comparison of the proposed connection over

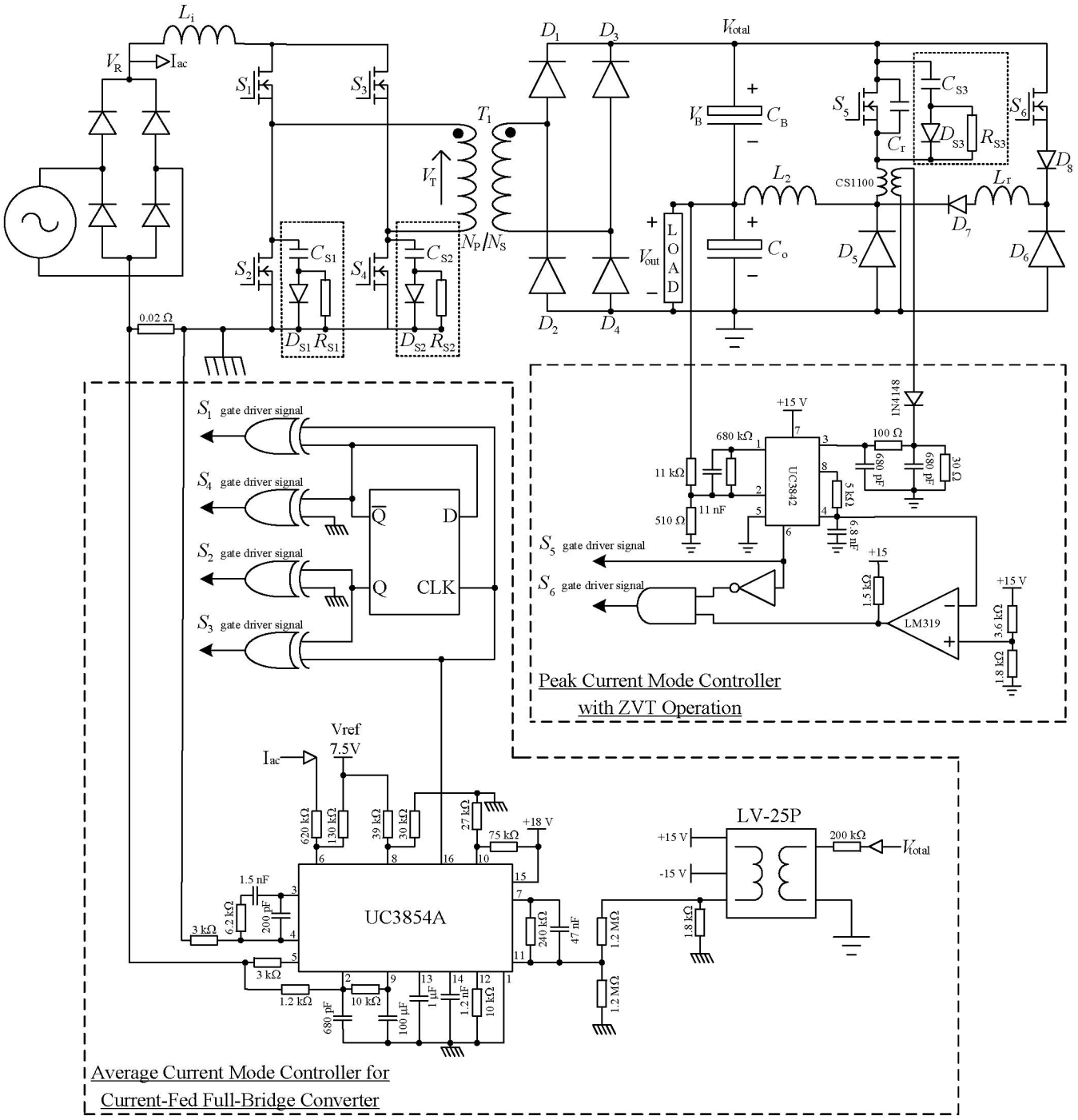

Fig. 6. The schematic diagram of the proposed PFC power supply prototype.

the classical two-stage cascade structure. The circuit is tested over a power range from 170 W to 600 W, as the buck-boost converter is only designed for 600 W output power. The efficiency gain of the proposed structure is around 3 % to compare with the classical structure. Fig. 8 shows two overall efficiency curves for confirming the efficiency formula. The measured overall efficiency of the proposed power supply is 84.3 % at 1 kW output power. The lost power mainly dissipates in the snubber circuits of the pre-regulator.

Figs. 9 and 10 show the waveforms of the current-fed full-bridge converter at 1 kW output power. The upper trace is the current of inductor, $L_{\rm i}$. The middle trace and the lower trace are $V_{\rm ds}$ of S_2 and $V_{\rm ds}$ of S_4, respectively. The voltage spikes on the switches are around 750 V at full load condition. The spikes are generated by a resonant network, which is composed of the leakage inductance of the power transformer and the output capacitors of the switches.

Fig. 11 shows the voltage waveforms of the main power switch, S_5, of the voltage regulator. The upper trace and the middle trace show that S_5 is operated in zero voltage switching. The lower trace is the voltage waveform of the power diode, D_5.

Finally, to verify the PFC function, the harmonic distortion are measured for different output power levels, as shown in

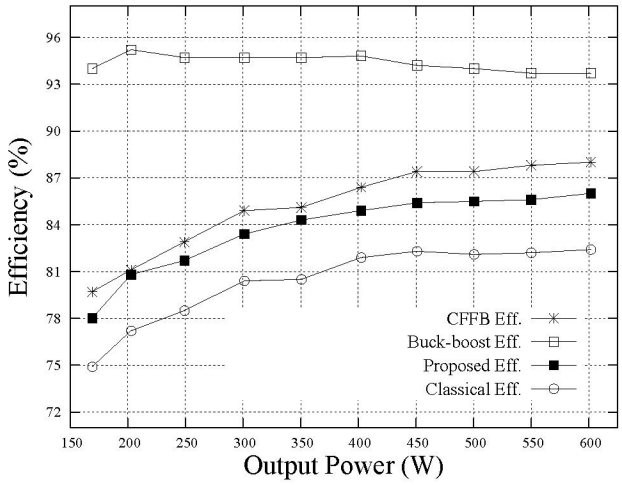

Fig. 7. Efficiency comparison of the proposed connection [Fig. 3], showing improved overall efficiency over the classical structure (k=0.44).

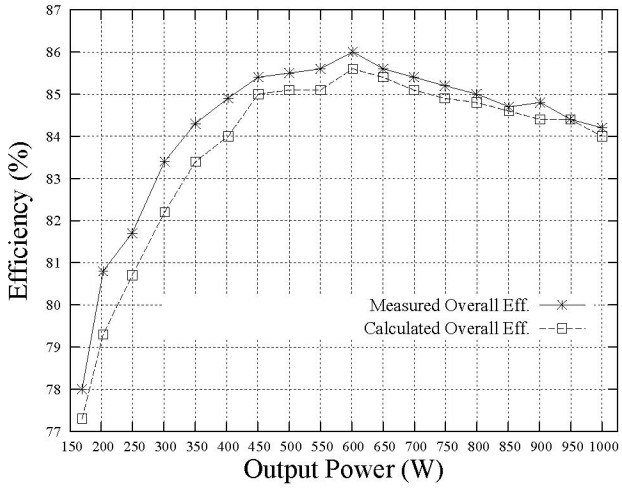

Fig. 8. Efficiency versus output power from 170 W to 1 kW for k=0.44, confirming the efficiency formula [Eqn. 2]; calculated curve is based on efficiency formula and measured value of η_{P1} and η_{P2}; experimental curve is from direct measurement of the overall efficiency.

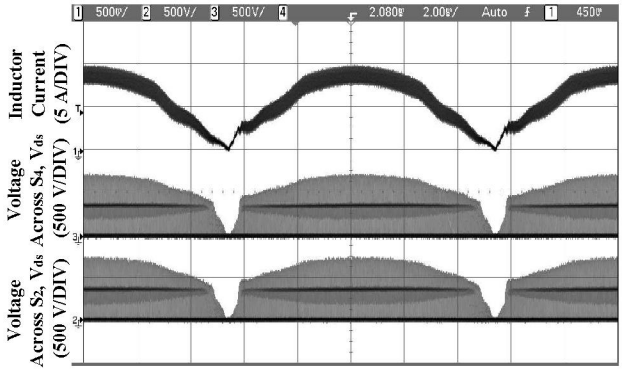

Fig. 9. The measured waveforms of the pre-regulator: input inductor current (upper trace), V_{ds} of S_4 (middle trace), and V_{ds} of S_2 (lower trace). Time scale is 2 ms/DIV.

Fig. 12, and the input voltage (upper trace) and the input current (lower trace) at full load condition are shown in Fig. 13.

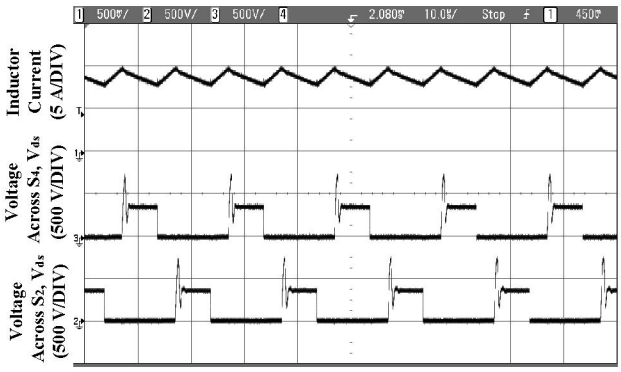

Fig. 10. The measured waveforms of the pre-regulator: input inductor current (upper trace), V_{ds} of S_4 (middle trace), and V_{ds} of S_2 (lower trace). Time scale is 10 μs/DIV.

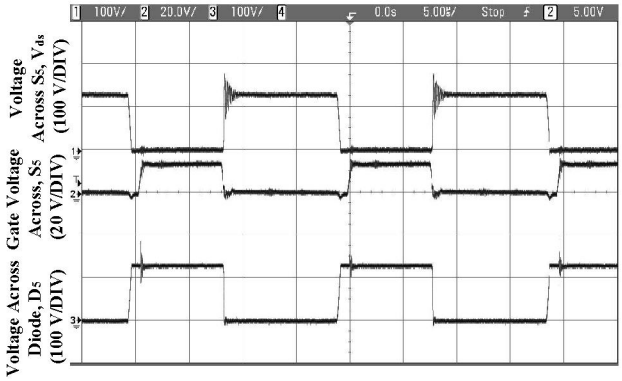

Fig. 11. The measured waveforms of the voltage regulator with ZVT operation: V_{ds} of S_5 (upper trace), V_{gs} of S_5 (middle trace) and the voltage across D_5. Time scale is 5 μs/DIV.

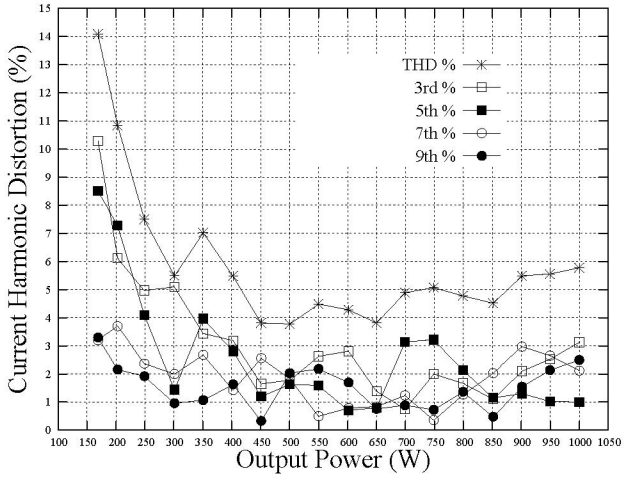

Fig. 12. The measured harmonic distortion versus output power.

V. Conclusion

In this paper, a 1 kW isolated PFC power supply using a non-cascade connection of a current-fed full-bridge converter and a buck-boost converter has been proposed. According to the R^2P^2 principle, the overall efficiency of the proposed power supply can be improved because part of the output power of the pre-regulator is transferred directly from the input to the regulated output. We have presented some design

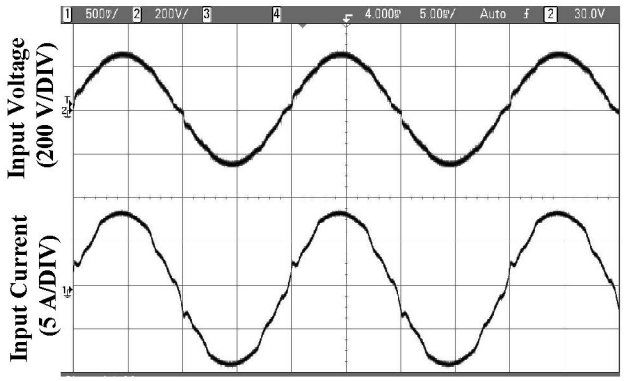

Fig. 13. The measured waveforms of the input voltage (upper trace) and the input current (lower trace) at full load condition. Time scale is 5 ms/DIV.

criteria for the proposed power supply, such as the choice of value of the capacitance of the energy storage capacitor, the conversion ratio of the current-fed full-bridge converter and some practical problems related to the implementation of the current-fed full-bridge converter. Also discussed is the role of the parameter k and its choice. A 1 kW experimental prototype has been built with ZVT incorporated in the voltage regulator stage. The measured results are reported to validate the theoretical prediction on the improved efficiency for the proposed power supply in comparison with the classical two-stage cascade structure.

REFERENCES

[1] European Standard EN 61000-3-2 Ed. 2:2001. Electromagnetic Compatibility (EMC), Part 3. Section 2. Limits for Harmonic Current Emission (Equipment Input up to and Including 16 A Per-Phase).

[2] IEEE Industry Applications Society/Power Enginnering Society. IEEE Std 519-1992 IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Sytem. Revision of IEEE Std 519-1992. Recognized as an American National Standard (ANSI).

[3] M. H. Kheraluwala, R. L. Steigerwald, and R. Gurumoorthy, "A Fast-Response High Power Factor Converter with a Single Power Stage," in *IEEE PESC Rec.*, pp. 769-779, 1991.

[4] Y. Jiang, F. C. Lee, G. Hua, and W. Tang, "A Novel Single-Phase Power Factor Correction Scheme," in *Proc. IEEE APEC*, pp. 287-292, 1993.

[5] R. Srinivasan and R. Oruganti, "Single-Phase Parallel Power Processing Scheme with Power Factor Control," in *Int. J. Electronics*, Vol. 80, No. 2, pp. 291-306, 1996.

[6] M. Madigan, R. Erickson, and E. Ismail, "Integrated High Quality Rectifier-Regulators," in *IEEE Trans. Industrial Electronics*, Vol. 46, No. 4 pp. 749-758, 1999.

[7] O. García, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "An Alternative to Supply DC Voltages with High Power Factor," in *IEEE Trans. Industrial Electronics*, Vol. 46, No. 4 pp. 703-709, 1999.

[8] C. K. Tse and M. H. L. Chow, "Theoretical Study of Switching Converters with Power Factor Correction and Output Regulation," in *IEEE Trans. Circuits Syst. I*, vol. 47, pp. 1047-1055, July 2000.

[9] C. K. Tse, M. H. L. Chow, and M. K. H. Cheung, "A Family of PFC Voltage Regulator Configurations with Reduced Redundant Power Processing," in *IEEE Trans. Power Electron.*, Vol. 16, No. 6, pp. 825-830, November 2001.

[10] O. García, J. A. Cobos, R. Prieto, J. Uceda, and S. Ollero, "A New Family of Single Stage AC/DC Power Factor Correction Converters with Fast Output Voltage Regulation," in *IEEE PESC Rec.*, pp. 536-542, 1997.

[11] A. Chibani and M. Nakaoka, "A New Control Topology of Single-Stage HF Link Switch-Mode-Rectifier with Sinusoidal Line Current," in *Industry Applications Society Annual Meeting Rec.*, pp. 1157-1162, 1990.

[12] N. Fröhleke, R. Mende, H. Grotstollen, B. Margaritis, and L. Vollmer, "Isolated Boost Fullbridge Topology Suitable for High Power and Power Factor Correction," in *IEEE IECON Rec.*, pp. 405-410, 1994.

[13] M. Qiu, G. Moschopoulos, H. Pinheiro, and P. Jain, "Analysis and Design of a Single Stage Power Factor Corrected Full-Bridge Converter," in *Proc. IEEE APEC*, pp. 119-125, 1999.

[14] G. Hua, C. S. Leu, Y. Jiang, and F. C. Y. Lee,"Novel Zero-Voltage-Transition PWM Converters," in *IEEE Trans. Power Electron.*, Vol. 9, No. 2, pp. 213-219, 1994.