Boundaries Between Fast- and Slow-Scale Bifurcations in Parallel-Connected Buck Converters

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***Abstract*— This paper studies a system of parallel-connected dc/dc converters under master-slave current sharing and proportional-integral (PI) PWM control. Two distinct types of bifurcations can be identified. Depending on the value of the integral time constant, the system exhibits either a slow-scale bifurcation (Neimark-Sacker bifurcation) or a fast-scale bifurcation (period-doubling). Extensive simulations are used to capture the behaviour. Trajectories before and after these bifurcations are shown. The boundaries between these two types of bifurcations are located. Parameter spaces of the feedback controller for stable and unstable operation are presented.**

I. Introduction

Power supplies based on paralleling switching converters offer a few advantages over a single, high-power, centralized power supply. They enjoy low component stresses, increased reliability, ease of maintenance and repair, improved thermal management, etc. [1]– [2]. Paralleling of standardized converters is an approach used widely in distributed power systems for both front-end and load converters.

In parallel converter systems, mandatory control is needed to ensure proper current sharing, and many effective control schemes have been proposed [1]– [4]. One widely used method for balancing the currents among the modules is the *master-slave current sharing* method. Under the master-slave scheme, one of the converters is the master and the other is the slave. The master has a simple feedback loop, consisting of a typical proportional-integral (PI) control, to regulate the output voltage. The slave basically sets its current to equal that of the master via an active loop involving comparison of the currents of the two converters, as shown in Fig. 1.

Generally, two distinct types of bifurcations have been identified for parallel converter systems, namely slow-scale bifurcation [5] and fast-scale bifurcation [6]. Under the master-slave current sharing and PI PWM control, the system can exhibit either slow-scale or fast-scale bifurcation. The determining parameter is the integral time constant τ_{F1} (τ_{F2}). Parameter spaces of the feedback controller are shown to be completely different under these two bifurcations. In this paper, we will study the effects of τ_{F1} (τ_{F2}). We will also identify the boundaries between these two types of bifurcations.

II. System Description and Operation

A. Proportional and Integral (PI) PWM Control

Figure 1 (a) shows two buck converters connected in parallel. In this circuit, S_1 and S_2 are switches, which are controlled by a standard pulse-width modulator consisting of a comparator that compares a control signal with a ramp signal. The ramp signal is given by

$$V_{\rm ramp} = V_L + (V_U - V_L)\left(\frac{t}{T_s} \bmod 1\right) \qquad (1)$$

where V_L and V_U are the lower and upper thresholds of the ramp respectively, and T_s is the switching period. Basically, switch S_i (i = 1, 2) is closed if $v_{{\rm con}i} > V_{\rm ramp}$ and is open otherwise.

The control signal $v_{\rm con1}$ and $v_{\rm con2}$ are derived from the feedback compensator, as shown in Figs. 1 (b) and (c). Here the compensator is a PI controller, i.e.,

$$\frac{V_{\rm con1}(s)}{V_e(s)} = -K_p\left(1 + \frac{1}{T_i s}\right) \qquad (2)$$

where $V_{\rm con1}(s)$ and $V_e(s)$ are the Laplace transforms of $v_{\rm con1}$ and v_e; v_e is the error between the reference voltage $V_{\rm ref}$ and the output voltage v_o; K_p and T_i are the parameters in the PI controller. As for the slave-converter, an extra current sharing signal is included, as shown in Fig. 1 (c).

B. Exact State Equations

The system can be regarded as a variable structure that toggles its topology according to the states of the switches. We assume that the converters are operating in continuous conduction mode, diode D_i is always in complementary state to switch S_i, for $i = 1, 2$. That is, when S_i is on, D_i is off, and vice versa. Hence, only four switch states are possible during a switching cycle, namely (i) S_1 and S_2 are on; (ii) S_1 is on and S_2 is off; (iii) S_1 is off and

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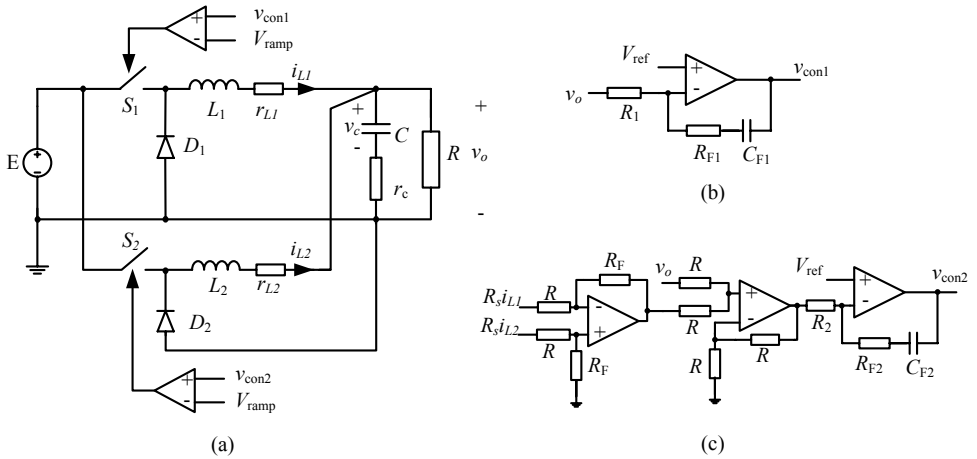


Fig. 1. Parallel connected buck converters under master-slave current sharing and PI control. (a) Converter stage; (b) controller for the master; (c) controller for the slave.

S_2 is on; (iv) S_1 and S_2 are off. The converter stage's state equations corresponding to these switch states are generally given by

$$\begin{array}{ll} \dot{x} = A_1 x + B_1 E & \text{for } S_1 \text{ and } S_2 \text{ on} \\ \dot{x} = A_2 x + B_2 E & \text{for } S_1 \text{ on and } S_2 \text{ off} \\ \dot{x} = A_3 x + B_3 E & \text{for } S_1 \text{ off and } S_2 \text{ on} \\ \dot{x} = A_4 x + B_4 E & \text{for } S_1 \text{ and } S_2 \text{ off,} \end{array} \tag{3}$$

where E is the input voltage, x is the state vector defined as

$$x = \left[i_{L1} \;\; i_{L2} \;\; v_c \right]^T, \tag{4}$$

and the A's and B's are the system matrices.

According to the feedback circuits, we can derive the control equations for $v_{\rm con1}$ and $v_{\rm con2}$

$$\frac{dv_{\rm con1}}{dt} = -K_1 \frac{dv_o}{dt} - \frac{K_1}{\tau_{F1}} v_o + \frac{K_1}{\tau_{F1}} V_{\rm ref}, \tag{5}$$

$$\begin{aligned} \frac{dv_{\rm con2}}{dt} &= -K_2 \frac{dv_o}{dt} - \frac{K_2}{\tau_{F2}} v_o + K_2 K_i \left(\frac{di_{L1}}{dt} - \frac{di_{L2}}{dt} \right) \\ &\quad + \frac{K_2 K_i}{\tau_{F2}} (i_{L1} - i_{L2}) + \frac{K_2}{\tau_{F2}} V_{\rm ref}. \end{aligned} \tag{6}$$

where K_1 and K_2 are the proportional gains, τ_{F1} and τ_{F2} are the integral time constants, K_i is the current sharing coefficient, and $V_{\rm ref}$ is the reference voltage (expected output voltage). In circuit terms, $K_1 = R_{F1}/R_1$, $\tau_{F1} = R_{F1}C_{F1}$, $K_2 = R_{F2}/R_2$, $\tau_{F2} = R_{F2}C_{F2}$, $K_i = R_F R_s/R$, where R_s is the current sensing resistance.

Also, the output voltage dv_o/dt can be written as

$$\frac{dv_o}{dt} = \frac{R}{R + r_C} \left[\frac{dv_c}{dt} + r_C \left(\frac{di_{L1}}{dt} + \frac{di_{L2}}{dt} \right) \right] \tag{7}$$

Substituting equations (3) and (7) into (5) and (6), we obtain

$$\begin{aligned} \frac{dv_{\rm con1}}{dt} &= M_1 x_1 + M_2 x_2 + M_3 x_3 - \\ &\quad \frac{K_1 R r_C}{(R + r_C)} \left(\frac{q_1 E}{L_1} + \frac{q_2 E}{L_2} \right) + \frac{K_1}{\tau_{F1}} V_{\rm ref} \end{aligned} \tag{8}$$

and

$$\begin{aligned} \frac{dv_{\rm con2}}{dt} &= N_1 x_1 + N_2 x_2 + N_3 x_3 - \frac{K_2 R r_C}{(R + r_C)} \left(\frac{q_1 E}{L_1} + \frac{q_2 E}{L_2} \right) \\ &\quad + K_2 K_i \left(\frac{q_1 E}{L_1} - \frac{q_2 E}{L_2} \right) + \frac{K_2}{\tau_{F2}} V_{\rm ref}, \end{aligned} \tag{9}$$

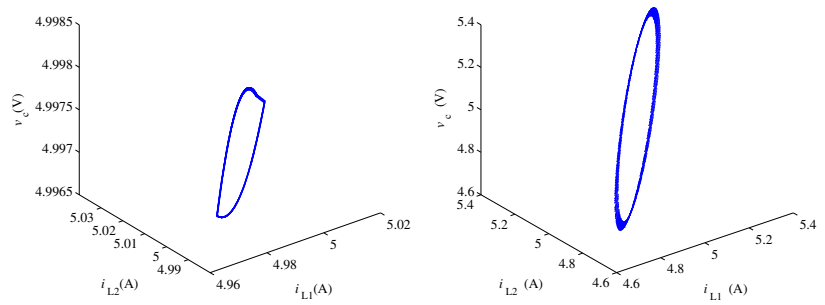
where M_1, M_2, M_3, N_1, N_2 and N_3 are the simplified coefficients related to the circuit parameters, and q_1, q_2 are the switching functions determined by the output of the controllers, which are given by

$$q_i(t) = \begin{cases} 1, & \text{if } v_{\rm coni} \geq V_{\rm ramp}, \quad \text{i.e., } S_i \text{ on,} \\ 0, & \text{if } v_{\rm coni} < V_{\rm ramp}, \quad \text{i.e., } S_i \text{ off.} \end{cases} \tag{10}$$

Controller equations (8) and (9), together with the power stage equation (3), form the complete set of state equations of the system. It is a fifth order system.

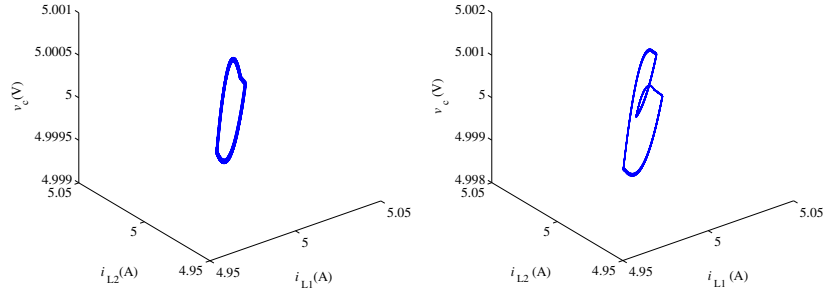
III. Identification of Slow-scale and Fast-scale Bifurcations

In this section, some observed bifurcation phenomena from numerical simulations that employ an exact piecewise-switched model will be presented. The simulations are based on the state equations derived in the foregoing section. We will primarily investigate the effects of the choice of the controller's parameters K_1, K_2, τ_{F1} and τ_{F2}, which are important design parameters in practice. The following circuit parameters are used in our simulations: switching period T_s = 10μs, input voltage E = 12V, reference voltage $V_{\rm ref}$ = 5V, ramp voltage V_L, V_U = 3V, 8V, inductance L_1 = 550μH, r_{L1} = 0.01Ω, inductance L_2 = 600μH, r_{L2} = 0.05Ω, capacitance C= 126μF, r_C = 0.01Ω, load resistance R = 0.5Ω and current sensing resistance R_s = 0.01Ω. We identify two types of bifurcations, namely, slow-scale bifurcation and fast-scale bifurcation.



(a) (b)

Fig. 2. 3-dimensional trajectories. (a) Stable period-1 trajectory for $K_1 = K_2 = 1.9$, $\tau_{F1} = \tau_{F2} = 0.3/\omega_0$, $K_i = 1$; (b) quasi-periodic trajectory after the slow-scale bifurcation for $K_1 = K_2 = 2$, $\tau_{F1} = \tau_{F2} = 0.3/\omega_0$, $K_i = 1$.



(a) (b)

Fig. 3. 3-dimensional trajectories. (a) Stable period-one trajectory for $K_1 = K_2 = 560.5$, $\tau_{F1} = \tau_{F2} = 1/\omega_0$, $K_i = 1$; (b) period-2 trajectory after the fast-scale bifurcation for $K_1 = K_2 = 561$, $\tau_{F1} = \tau_{F2} = 1/\omega_0$, $K_i = 1$.

A. Slow-Scale Bifurcation

In the simulation, we set $K_1 = K_2$, $\tau_{F1} = \tau_{F2}$ for simplicity. Normally, the PI controller will introduce a zero, $1/\tau_{F1}$ $(1/\tau_{F2})$, to the control loop, to cancel the effect of double poles of the circuit. So, we compare τ_{F1}, τ_{F2} with the system's inherent natural frequency ω_0, which is defined as $\omega_0 = 1/\sqrt{L_e C}$. Here, L_e is the equivalent inductance of the paralleled converters. When τ_{F1} (τ_{F2}) is relatively small, e.g., $\tau_{F1} = \tau_{F2} = 0.3/\omega_0$, we can identify slow-scale bifurcation (Neimark-Sacker bifurcation) as we increase K_1 (K_2). The 3-dimensional trajectories of the period-1 orbit before the bifurcation and the quasi-periodic orbit after the bifurcation are shown in Fig. 2 (a) and Fig. 2 (b), respectively.

B. Fast-Scale Bifurcation

When τ_{F1} (τ_{F2}) is relatively large, e.g., $\tau_{F1} = \tau_{F2} = 1/\omega_0$, we can identify fast-scale bifurcation (period-doubling) as we increase K_1 (K_2). The 3-dimensional trajectories of the period-1 orbit before the bifurcation and the period-2 orbit after the bifurcation are shown in Fig. 3 (a) and Fig. 3 (b), respectively.

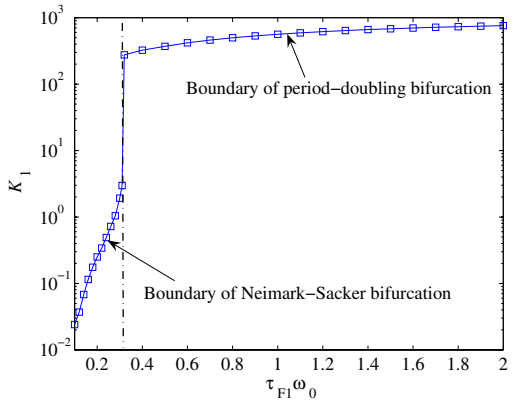


Fig. 4. Boundaries of slow-scale and fast-scale bifurcations for $K_i = 1$. The dash line shows the boundary between the two types of bifurcation.

C. Boundaries Between the Two Types of Bifurcation

From the above simulations, we know that two types of bifurcation will occur in the parallel-connected buck converters under PI control. Computer simulations reveal

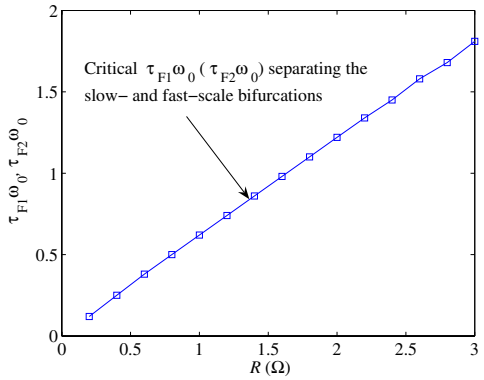


Fig. 5. Critical $\tau_{F1}\omega_0$ ($\tau_{F2}\omega_0$) separating the slow- and fast-scale bifurcations for different output power levels with $K_i = 1$. For $\tau_{F1}\omega_0$ ($\tau_{F2}\omega_0$) below the critical value, slow-scale bifurcation occurs as K_1 (K_2) is increased. Fast-scale bifurcation occurs otherwise.

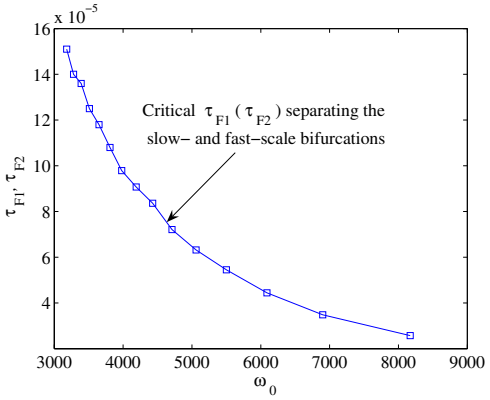


Fig. 6. Critical τ_{F1} (τ_{F2}) separating the slow- and fast-scale bifurcations for different ω_0 with $K_i = 1$. For $\tau_{F1}(\tau_{F2})$ below the critical value, slow-scale bifurcation occurs as K_1 (K_2) is increased. Fast-scale bifurcation occurs otherwise.

that the crucial parameter that determines the type of bifurcation is τ_{F1} (τ_{F2}). For each value of $\tau_{F1}\omega_0$ ($\tau_{F2}\omega_0$), we first determine the critical value of K_1 (K_2). Then, we may construct the stability boundaries, as shown in Fig. 4. Moreover, we can locate the critical value of $\tau_{F1}\omega_0$ ($\tau_{F2}\omega_0$) that determines the type of bifurcation occurred. The boundary between slow-scale and fast-scale bifurcations is shown as dash line in Fig. 4. The parallel converters work in the normal stable period-1 operation when the values of control parameters are located below the boundary curve. However, the system undergoes Neimark-Sacker bifurcation when K_1 (K_2) crosses the boundary at the left side of the critical value of $\tau_{F1}\omega_0$ ($\tau_{F2}\omega_0$), and period-doubling at the right side. In the figure, the boundary of Neimark-Sacker bifurcation is much lower than that of period-doubling, which is very important for practical design. In practice, we avoid the occurrence of slow-scale bifurcation and prefer to set a large value of $\tau_{F1}\omega_0$ ($\tau_{F2}\omega_0$) in order to get a wide range of K_1 (K_2).

We can adjust the output power by changing the load resistance R (the output voltage is kept at a constant value). For different levels of the output power (with fixed ω_0=$\frac{1}{\sqrt{L_e C}}$), we have collected the critical values of $\tau_{F1}\omega_0$ ($\tau_{F2}\omega_0$). A graphical presentation is shown in Fig. 5. We observe that the critical value of $\tau_{F1}\omega_0$ ($\tau_{F2}\omega_0$) increases linearly with the increase of load resistance R. Then, we fix the output resistance R and change the value of C, i.e., ω_0, and again collect the the critical values of τ_{F1} (τ_{F2}). A graphical presentation is shown in Fig. 6. From the figure, the critical value of τ_{F1} (τ_{F2}) decreases significantly with the growth of ω_0.

IV. Conclusion

In this paper, a system of parallel connected buck converters under master-slave current sharing and proportional-integral (PI) PWM control is studied. Fundamentally different types of nonlinear phenomena are observed in these systems. Depending on the value of the integral time constant τ_{F1} (τ_{F2}), either fast-scale or slow-scale bifurcation occurs. For small τ_{F1} (τ_{F2}), Neimark-Sacker bifurcation will occur, and for large τ_{F1} (τ_{F2}), period-doubling bifurcation occurs. The ranges of parameter space of the feedback controller are shown to be different under these two bifurcations. Extensive computer simulations are used to identify the bifurcation boundaries. The critical values of τ_{F1} (τ_{F2}) for different values of power and natural frequency ω_0 are collected. The simulations and numerical analysis reveal the fact that two types of bifurcation will occur in the system, and τ_{F1} (τ_{F2}) will determine the type of bifurcation. The results presented provide a useful reference for practical design of parallel converters in a wide range of control parameters.

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References

[1] V. J. Thottuvelil and G. C. Verghese, "Analysis and control of paralleled dc/dc converters with current sharing," *IEEE Trans. Power Electron.,* vol. 13, no. 4, pp. 635–644, Jul 1998.

[2] K. Siri, C. Q. Lee and T. F. Wu, "Current distribution control for parallel connected converters: Part I and Part II," *IEEE Trans. Aerospace Electron. Syst.,* vol. 28, no. 3, pp. 829–851, Jul 1992.

[3] R. Giral, L. Martinez-Salamero and S. Singer, "Interleaved converters operation based on CMC," *IEEE Trans. Power Electron.,* vol. 14, no. 4, pp. 643–652, Jul 1999.

[4] X. Zhou, P. Xu and F. C. Lee, "A novel current-sharing control technique for low-power high-current voltage regulator module applications," *IEEE Trans. Power Electron.,* vol. 15, no. 6, pp. 1153–1162, Nov 2000.

[5] Y. Huang and C. K. Tse, "On the basins of attraction of parallel connected buck switching converters," in *Proc. IEEE Int. Symposium Circ. Syst.,* pp. 5647–5650, May 2006.

[6] H. H. C. Iu and C. K. Tse, "Bifurcation behaviour in parallel-connected buck converters," *IEEE Trans. Circ. Syst. Part I,* vol. 48, no. 2, pp. 233–240, Feb 2001.