A Programmable, Cost-Effective, Real-Time High Frequency Ultrasound Imaging Board Based on High-Speed FPGA

Weibao Qiu, Yanyan Yu, Lei Sun

Department of Health Technology and Informatics, The Hong Kong Polytechnic University, Hong Kong, China

Email: htsunlei@inet.polyu.edu.hk

***Abstract*—High frequency (>20MHz) ultrasound imaging has made it possible to delineate small structures with fine spatial resolution. Previously, a high frequency high frame rate imaging system had been developed for small animal cardiac imaging [2, 5]. This paper presents further development of a programmable, low-cost, real-time high frequency ultrasound imaging board based on high-speed FPGA. Utilization of FPGA facilitates programmable applications with high flexibility. The printed circuit board (PCB) design achieves cost-effectiveness and compactness. The PCI bus interface allows high speed data transfer and real-time imaging. The dedicated front-end electronics showed a minimum detectable signal of 18μV, allowing a 50dB dynamic range at a total gain of 50dB. The high–speed analog to digital converter (ADC) with a typical 10.8 bit ENOB was employed to accomplish high speed data acquisition. Algorithms such as band-pass filter, envelope detection and digital scan converter were implemented in the FPGA with high speed and high flexibility. Finally, wire phantom experiment showed good performance of such a programmable and compact design.**

Keywords; high frequency ultrasound, FPGA, PCB, programmable, real- time

I. INTRODUCTION

Ultrasound imaging is a well established and widely used technique in medical diagnosis with the excellent features of non-invasiveness and real-time. High frequency (>20MHz) ultrasound imaging has made it possible to delineate small structures with fine spatial resolution on the order of tens of microns, which could provide better understanding about certain physiological mechanism. This technique significantly improves the performance in ophthalmic, dermatologic, intravascular, small animal imaging, disease prognosis and treatment strategies [1], [2]. A number of such high-frequency single-element devices had been developed in recent years [3], [4]. In addition, a commercial system is also available for small animal imaging (Vevo 770, Visualsonics, Inc., Toronto, Canada). However, a high resolution, high frame rate system with high flexibility and cost-effectiveness are still needed for many medical and biological applications.

A high frequency high frame rate ultrasound imaging system had been developed previously for small animal cardiac imaging. [2] [5]. This paper presents the further design and implementation of high speed FPGA based imaging board to achieve programmability, real-time, high resolution, compactness and fully digital control. The ultrasound image data are acquired and displayed simultaneously. Such a design is capable of high frame rate (up to 200 fps) imaging up to 80MHz.

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II. METHODOLOGY

The entire imaging system incorporated a high speed imaging board with analog front-end electronics and digital back-end unit, a high speed mechanical sector probe [5] and a high frequency bipolar pulse generator [6]. The block diagram is shown in Fig.1. The FPGA based programmable and cost-effective imaging board was implemented in a 12 layers PCB scheme. This board utilized 64-bit PCI bus for high-speed data transfer and real-time imaging.

A. Analog electronics

High resolution imaging is not only subject to the ultrasound frequency range, but also related to the noise level in the analog circuits. Poor circuit design will increase the noise sharply in the dedicated analog part particularly in high frequency application. When the signal is lost in the front parts, it can no longer be compensated even super algorithms have been achieved in the post imaging processing.

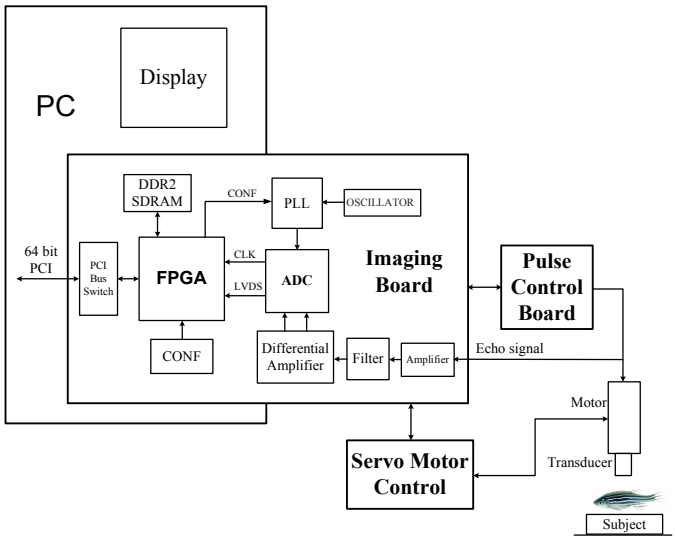

Figure 1. The real-time high frequency ultrasound imaging system.

In this design, echo signals from the transducer will be amplified by a low noise amplifier (SMA231, Tyco Electronics Co., Berwyn, PA). The maximum noise figure is 1.7dB and the minimum gain is 26dB with gain flatness lower than ±0.2dB in the frequency spectrum of 20-80MHz. A low pass filter (RLP83+, Mini-Circuits, Brooklyn, NY) with a cut frequency of 93MHz was used for anti-aliasing. The insertion loss is lower than 1dB. A low noise, low distortion amplifier (THS4509, Texas Instruments Inc., Dallas, Texas) is employed to transmit the single end signal to differential pair for high speed ADC.

B. ADC

The ultrasound radio-frequency (RF) data are digitized with a high speed ADC (ADS5517, Texas Instruments Inc., Dallas, Texas). The maximum sampling rate is 200MSPS. The typical ENOB is 10.8 bit. It could support fully differential DDR (double data rate) LVDS clock. Flexible output clock position programmability is available to ease capture and trade-off setup for hold times. The signal to noise ratio (SNR) is 66.9dB when input a 70MHz signal. After the digitization, the signal will be transferred to FPGA through LVDS bus.

C. FPGA

A high performance FPGA (Stratix II EP2S60F672I4, Altera Corporation, San Jose, CA) with great signal integrity was employed, which can support data processing at an adequate speed. This component includes 39 DSP blocks (total 288 9×9Multipliers) which can efficiently implement high speed digital signal processing algorithms. It demonstrated up to 287MHz high order FIR, Hilbert transform and high speed DSC algorithms. It can also support DDR2 SDRAM and PCI interface. A total of 512 Mb memory combined with double DDR2 SDRAM (MT47H16M16, Micron Technology Inc., Boise, ID) was implemented to buffer temporary DSC data. The processed data were transferred to the computer through a 64bit 66MHz PCI bus. To improve data transfer efficiency, a special FIFO was implemented in the FPGA to buffer the data.

Fig.2 shows the algorithms which were implemented in this high-speed FPGA. There are three steps of data preconditioning before digital scan conversion (DSC), which are, in the order of execution: band-pass filter, digital time gain compensation (TGC) and envelope detection. The TGC and logarithm compressor is user configurable. Raw RF data can also be transferred to the computer for storage and later processing when chosen by the user.

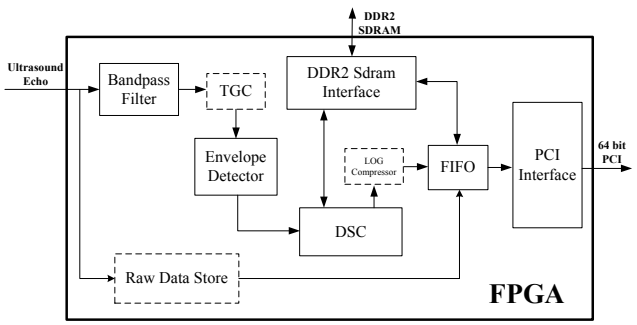

Figure 2. The algorithms implemented in FPGA.

1) Band-pass filter

Ultrasound echo signal collected by the high speed ADC contain noises which have large spectral components in the low frequency and high frequency range. They distort the echo signal and prevent an accurate calculation of the envelope. In the back-end unit, undesirable noise cancellation will be performed by implementing a digital band-pass FIR filter. The symmetric of FIR characteristics is used to decrease the usage of multiplier which is limited in the FPGA. To attain high speed calculation, FPGA employs internal high speed DSP blocks which are faster than ALM-based (adaptive logic module) implementations. The simulation result which is shown in TABLE.I indicates that the maximum speed of the FIR filter can be achieved up to 287MHz. High order FIR filter can obtain a better SNR, but it also had long latency and long ripples. A 63-tap FIR is implemented in the FPGA with a good trade-off.

2) Envelope detector

The amplitude of echo signal represents the property of physiological tissue. Since ultrasonic echo signals are broadband, the proposed solution to extract envelope is based on Hilbert transform. Fig.3 presents brief architecture of the designed envelope detection method. To synchronize the in-phase (I) signal with the quadrature (Q) signal, a delay algorithm was used in parallel with the Hilbert transform.

The square root function $\sqrt{R_I^2 + R_Q^2}$ was needed to fulfill the envelope detector after I/Q data were acquired. It can be realized by several algorithms [7], [8]. To acquire a high speed computation in FPGA for real-time imaging, Cordic (coordinated rotation digital computer) algorithm is suitable for this purpose. The achieved speed is 281.61MHz currently which is shown in TABLE.II and it can be further improved if the practical application needed.

3) High Speed Digital Scan Conversion

The acquired ultrasound data by using a sector motor are in polar coordinates. Therefore, a conversion from the polar coordinates to the Cartesian coordinates is necessary. A previous high speed DSC method based on the FPGA was utilized [9]. It can be implemented in the FPGA based on RAM structure. The linear implementation performs only angular interpolation, thus calculating a pixel value V_p by

$$V_p = \frac{S1 \times \alpha + S2 \times \beta}{\alpha + \beta} \tag{1}$$

Where S1 and S2 are two nearest samples to an object pixel along the radius direction, α and β are angular difference between the object pixel and the two samples.

TABLE I. PERFORMANCE OF THE FIR FILTER IN FPGA WITH SYMMETRIC STRUCTURE

FIR Order	Area(ALUTs)	9 × 9 Multipliers in High Speed DSP Block	Speed(MHz)
63	1953 (4%)	64(22%)	287.44

TABLE II. PERFORMANCE OF THE CORDIC SQUARE ROOT ALGORITHM IMPLEMENTED IN FPGA

Area(ALUTs)	Speed(MHz)
1278 (3%)	281.61

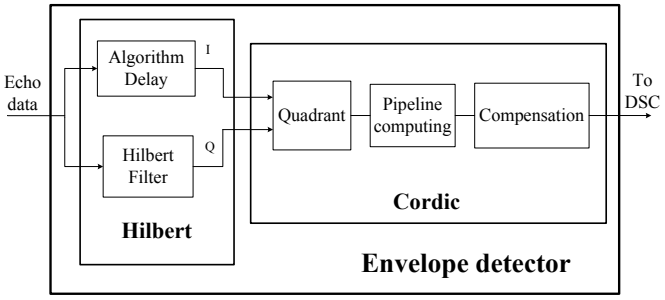

Figure 3. Envelope detector based on Hilbert transforms.

This method limited the implementation of a large image due to the limited size of RAM memory in FPGA. When a new application is coming, the program has to re-synthesize, it is inconvenient and also time consuming. So a novel effective method based on high speed DDR2 SDRAM is proposed in this paper.

Fig. 4 shows a functional block diagram of the high speed DSC adopting the linear interpolation algorithm which is expressed by (1). In this implementation, all angle and position data will be stored in a DDR2 SDRAM which can run at 267MHz. So the size of image can be easily increased and adjustable. Before the data acquisition start, the DSC setting will be pre-transferred into the RAM. Data management is used to control the dual port RAM which is used to buffer the ultrasound scan lines. Three dual port RAM, which are used in turn to buffer high speed data flow, could improve the effective of computation. When the acquisition is finished, the calculation will be launched to do the transform using the position and angle parameters which are stored in the DDR2 SDRAM.

The ultrasound imaging configurable parameters, such as focus length of the transducer, swing angle, numbers of scan-line etc. can be easily changed by the computer software in real time.

III. RESULTS

The prototype of imaging board is shown in Fig. 5. It is a 12 layers PCB design incorporating high speed FPGA, ADC and low-noise analog electronics. The size of the imaging board is 16.8cm × 10.6cm. A 64 bit PCI bus is designed for high speed data transfer and real-time imaging.

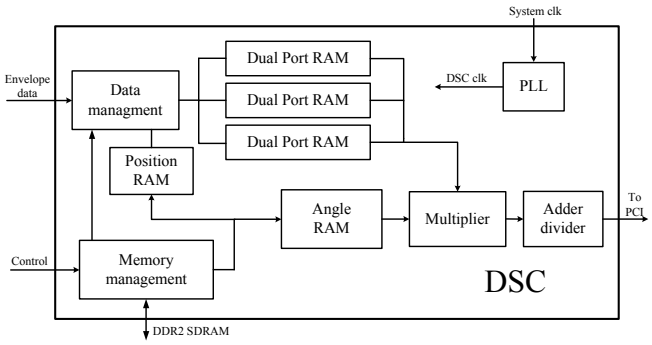

Figure 4. Functional block diagram of high-speed digital scan converter with linear interpolation.

A. *Performance of front-end part*

The performance of front-end part was tested by a set of RF instruments. Signal generator (HP8656B, Hewlett Packard) and spectrum analyzer (HP8591E, Hewlett Packard) are employed to test the RF performance of analog electronics such as gain linearity and flatness. The experiment resulted show that the circuit had good linearity and the maximum fluctuation in the pass band was lower than ±1dB.

A function generator (AFG 3251, Tektronix Inc., Beaverton, OR) and a series of attenuators (Mini-Circuits, Brooklyn, NY) were connected to test the dynamic range. Function generator generated five-cycle sinusoid signals to the imaging board after attenuation. Then acquire the amplified sinusoid signal in the FPGA after digitalization by ADC. The result indicates that the analog circuits have a minimum detectable signal of 18μV, allowing a 50dB dynamic range when the total gain is approximately 50dB and the central frequency of RF signal is 50MHz.

B. *Test of processing speed*

In order to evaluate the speed of the image processing, a four-cycle burst signal was generated by a function generator (AFG 3251, Tektronix Inc., Beaverton, OR) with particular central frequency (45MHz). Fig. 6 shows the acquired image. The experiment shows that the maximum processing speed could be more than 500 images per second.

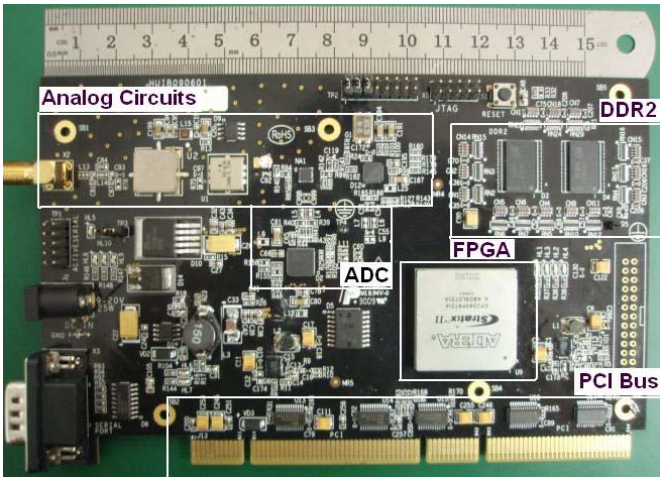

Figure 5. Photograph of imaging processing board.

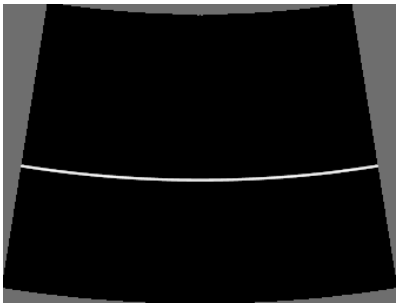

Figure 6. Burst signal test.

C. *Imaging a wire phantom*

The quality of the designed system was evaluated by tungsten wire phantom (California Fine Wire Co., CA). The ultrasound image of a tungsten wire phantom is shown in Fig.7, demonstrating the image quality of designed system. The wire phantom consists of five 20 um diameter tungsten wires of which distance intervals along vertical and horizontal direction are approximately 1.35 mm and 0.45 mm respectively. In this experiment, a 35MHz single element transducer was employed in the system.

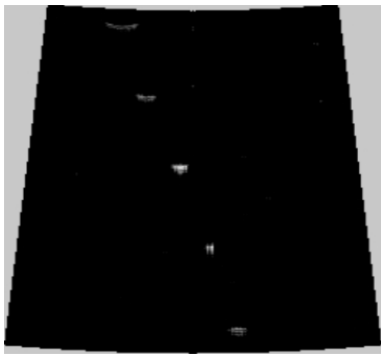

Figure 7. Wire phantom image of designed system.

IV. CONCLUSION

A programmable, cost-effective, high-frequency ultrasound imaging board has been described in this paper. The experimental results show that the minimum detectable signal of 18uV, allowing a 50dB dynamic range when the total gain is approximately 50dB. The system is capable to achieve high frame rate (up to 200 fps) ultrasound B-mode imaging up to 80MHz. This system can be used in ophthalmic, dermatologic and small animal imaging etc. The clinical performance of the system will be further improved. And more experiments in vivo will be carried on in the next step.

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