1 × 4 All-Optical Packet Switch at 10 Gb/s

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***Abstract*—We demonstrated a 1 × 4 all-optical packet switch with all-optical header processing at a header rate of 5 Gb/s and payload rate of 10 Gb/s using injection-locking in a single Fabry–Pérot laser diode at each output port of the switch.**

***Index Terms*—All-optical devices, all-optical header processing, all-optical packet switching, Fabry–Pérot laser, injection-locking.**

I. Introduction

ALL-OPTICAL packet switches in which both header processing and packet forwarding are carried out in the optical domain eliminate the need for optical–electrical conversion and are expected to play an important role in future high-speed networks. A 1 × 2 all-optical switch was implemented using a semiconductor laser amplifier in loop optical mirror structure and an optical flip-flop memory [1]. The packet payload data rate is 2.5 Gb/s and the payload is Manchester encoded. The header is 7.5 μs long and consists of a repeated hexadecimal pattern. In this letter, we demonstrated a 1 × 4 all-optical packet switch with all-optical header processing using injection-locking in a single Fabry–Pérot laser diode (FP-LD) at each output port of the switch [2]. The data rates of the header and the payload are 5 and 10 Gb/s, respectively. No special format is required for the payload.

II. Operating Principle

Fig. 1 shows a schematic of the proposed $1 \times N$ all-optical packet switch. An incoming packet is first split into N parts using a $1 \times N$ coupler into the N output ports of the $1 \times N$ switch. The packet processor (PP) at each output port transmits a packet only if the packet header address matches with the address of the output port and blocks the packet otherwise. For an incoming packet, only one of the N PPs will transmit while the other $(N-1)$ PPs will block the data packet. The packet forwarding function is, thus, realized. Because of the splitting of the signals by the coupler, in practice, the data packets will have to be amplified after splitting. The size of the proposed all-optical packet switch is, therefore, limited by the signal-to-noise ratio of the amplified data packets after the splitting. In order to simplify the requirement in optical signal processing and to eliminate the need of optical table lookup, we implemented the self-routing address format proposed in [3] which identifies each output port of every node in a network by a different bit in the address header. Since the address length scales linearly with the total number of output ports of all the nodes in the network, the self-routing address is suitable for small to medium size networks only. Using the proposed address format, a PP only needs to process a single bit in the data packet address header to determine whether to pass or block a packet.

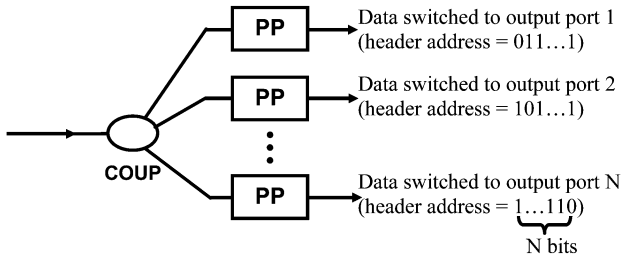

Fig. 1. Proposed $1 \times N$ all-optical packet switch. COUP: Coupler.

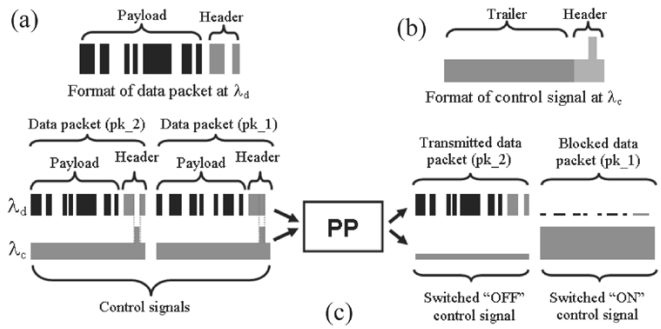

Fig. 2. Formats of the (a) data packet and (b) control signal. (c) The switching mechanism of the PP in time domain.

The formats of the data packets and the local control signals are described as follows. A data packet indicates its intended output port at a node by setting the corresponding address bit in the header to "0" and the rest of the address bits to "1s." Fig. 2(a) shows the format of a data packet with address headers "1011" intending for output Port 2 in a 1 × 4 switch. (The header is shown in gray for illustration.) For simplicity, we assume in the following that the header of a data packet contains only the address of an output port of a single node. The bit-duration of the data header and the payload need not be the same and no special encoding formats are required in the payload. The special two-level local control signal is in packet format with both address header and trailer. The length of the control signal is equal

Manuscript received October 11, 2004; revised January 16, 2005. This work was supported in part by the Research Grant Council of the Hong Kong Special Administrative Region, China, under Project PolyU5242/03E, and in part by Photonic Manufacturing Service Ltd.

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Digital Object Identifier 10.1109/LPT.2005.846492

to that of the data packet. The control packet header contains the complement of the address of the output port to which the PP is attached [2], [4]. Fig. 2(b) shows the format of the local control signals for output Port 2 with the address "0100," the complement of "1011." The trailer of the control signal contains all "0" bits. The control signals are designed such that the light intensity of the "0" bits is nonzero [Fig. 2(b)]. The guard periods between the control signals and the data packets, however, do not contain any light intensity.

We utilize the property of multimode injection-locking and bistability characteristic of injection-locking in a single FP-LD to realize the all-optical header processing and data packet switching required in the PP. In multimode injection-locking, the injection-locking threshold of an FP-LD by external light injection at a wavelength λ_c with a wavelength detune of $\Delta\lambda_c$ from one of the free-running longitudinal modes of the FP-LD can be lowered by injecting another optical signal near a different longitudinal mode of the FP-LD with less power and wavelength detune $(\Delta\lambda_d)$, where $(\Delta\lambda_c > \Delta\lambda_d)$ [4], [5]. Injection-locking threshold power is the power required for an external injected signal to injection-lock an FP-LD. By proper choices of the powers and detunes of the data packets and control signals, the outcome of signal processing by multimode injection-locking at a single bit at the control signal header, i.e., whether injection-locking is initiated or not, can last the entire duration of the control signal through the bistability property of the FP-LD.

To realize the PP, we simultaneously injected the data packet, the special two-level control signal, and a continuous-wave (CW) stabilizer signal into an FP-LD. The wavelengths of the CW stabilizer signal $(\lambda_{\rm cw})$, the data packets (λ_d) and the control signal (λ_c) are chosen to be on the longer wavelength sides of three different longitudinal modes of the FP-LD such that any one of the signals can injection-lock the FP-LD if the respective injection-locking power threshold is reached. The control signals and the data packets are assumed to be synchronized. The powers and detunes of the data packets, the control signal, and the CW stabilizer signal are chosen according to the following criteria: 1) A "1" bit in the control signal will injection-lock the FP-LD at λ_c only in the presence of a "1" bit in the data packet. 2) If the FP-LD is not injection-locked at λ_c, a "0" bit in the control signal cannot injection-lock the FP-LD at λ_c even in the presence of a "1" bit in the data packet. 3) The "0" bits in a control signal can maintain injection-locking of the FP-LD at λ_c if the FP-LD is already injection-locked by the control packet at λ_c. 4) The CW stabilizer signal injection-locks the FP-LD only in the absence of both the control signals and data packets, i.e., in the guard periods only. Criterion 1 and 2 are the consequence of multimode injection-locking while Criteria 3 is possible because of the bistable nature of FP-LDs [4]. The functions of the CW stabilizer signal are to suppress the power of the FP-LD modes when the intensities of both the data packet and control signal are low, i.e., in the guard period only, and to increase the speed of injection-locking by stimulated emission. Note that the FP-LD is injection-locked by one of the three signals: control, data, or CW at any time.

Fig. 2(c) shows an example of the operation of the PP which consists of a single FP-LD. Data packets pk_1 and pk_2 with headers "0111" and "1011," respectively, are input to the FP-LD

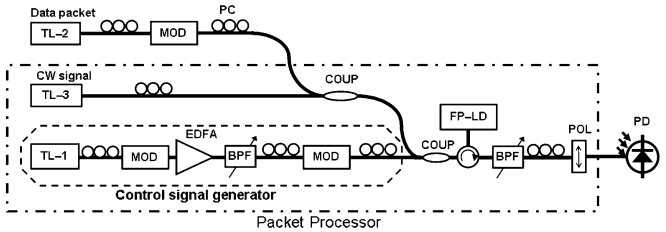

Fig. 3. Experimental setup. TL: Tunable laser. PC: Polarization controller. MOD: Modulator. COUP: Intensity coupler. ATT: Variable attenuator. CIR: Circulator. BPF: Variable bandpass filter. EDFA: Erbium-doped fiber amplifier. ODL: Variable optical delay line. POL: Polarizer. PD: Photodiode.

at wavelength λ_d. Control signals with header "0100" are input to the FP-LD at wavelength λ_c. For pk_1, the address header of the data packet does not match with that of the local control signal, thus, the "1" bit in the control packet header coincides with a "1" bit in the data packet header. The control signal injection-locks the FP-LD at λ_c because of multimode injection-locking (Criterion 1) and able to maintain injection-locking because of bistability until the end of the control signal (Criterion 3). The resulting red-shift of the FP-LD mode comb suppresses the data packet gain [2]. The output of the FP-LD at λ_c will be high while that at λ_d will be low. As a result the FP-LD blocks the data packet as shown in right-hand side of Fig. 2(c). For pk_2, the address of the data packet matches with that of the control signal, the "1" bit in the control signal header coincides with the "0" bit in the data packet header. Thus, the control signal does not injection-lock the FP-LD at λ_c for the entire duration of the packet because of Criterion 1 and 2. The output of the FP-LD at λ_c will be low while that at λ_d will be high. The FP-LD will, therefore, transmit the data packet, as shown in Fig. 2(c). By this design, the outcome of the signal processing at one bit location in the data packet header is able to switch ON or OFF the entire data packet.

III. Experimental Results

Fig. 3 shows the experimental setup. We used a commercially available FP-LD with a multiquantum-well structure. The FP-LD is around 300 μm long with a free-spectral range of 0.93 nm. The control signals at 1539.99 nm are generated using a 10-Gb/s nonreturn-to-zero (NRZ) pulse pattern generator, a 155-MHz pulse pattern generator, and two modulators, one at 10-Gb/s and the other at 2.5-Gb/s $LiNbO_3$, on the output of a tunable laser (TL-1). The peak power and trailer power are $\sim$0.4 and -1.1 dBm, respectively (extinction ratio $\sim$1.5 dB). The wavelength detune is $+0.17$ nm. The output of the 155-MHz pulse pattern generator is triggered by the clock/32 output of the 10-Gb/s NRZ pulse pattern generator for synchronization. The 10-Gb/s data packets at 1535.21 nm are generated by externally modulating another tunable laser (TL-2) using another 10-Gb/s NRZ pulse pattern generator and a $LiNbO_3$ modulator. The injected power is -15.00 dBm and the wavelength detune is $+0.08$ nm. The two 10-Gb/s pattern generators are synchronized using an external 10-GHz clock. The CW stabilizer signal at 1537.02 nm is generated by a third tunable laser (TL-3) with an injected power of -8.50 dBm and the wavelength detune is $+0.02$ nm. We note that bistability occurs only for wavelength detune larger than $+0.08$ nm with the FP-LD used here. Thus,

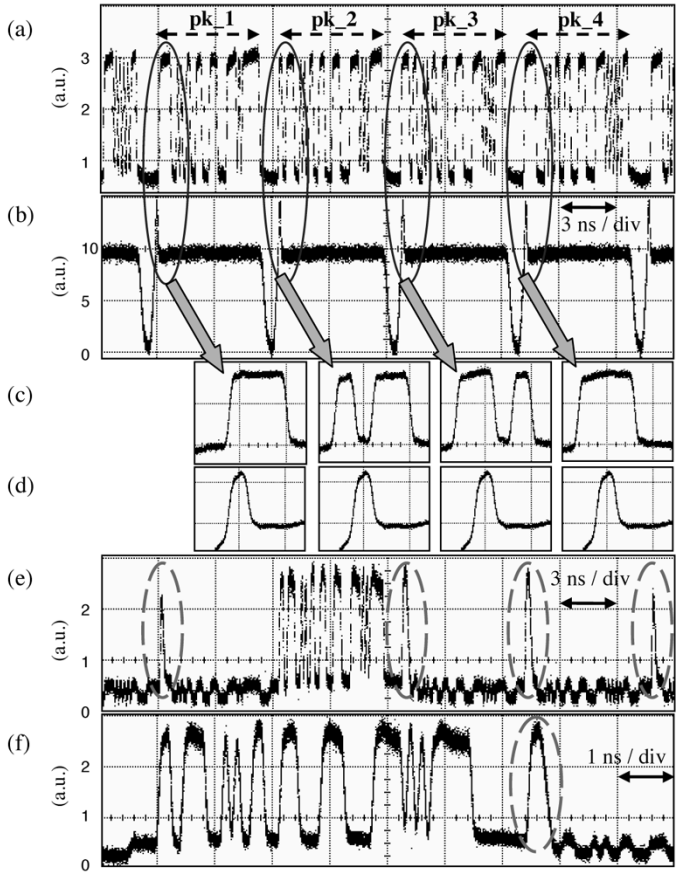

Fig. 4. Measured synchronized timing diagrams for (a) the input 10-Gb/s data for four consecutive packets and (b) the input control signal to the FP-LD. (c) The headers of for pk_1 to pk_4 with patterns "0111," "1011," "1101," and "1110," respectively, at the FP-LD input. (d) The control signal headers with pattern "0100" at the FP-LD input. Time scale 500 ps/div for both (c) and (d). (e) The switched output of the four data packets (time scale: 3 ns/div) and (f) the switched output of data packet pk_2 (time scale: 1 ns/div).

bistability is initiated only by the control signal when it injection-locks the FP-LD. The bias current of the FP-LD is 13.5 mA.

In the experiment, we encode four different data packets with different header bits which indicate four different output destinations. The data packet header is, therefore, 4 bits long corresponding to a 1×4 switch. The bit period at the header is 200 ps long which means the header rate is 5 Gb/s. The packet headers of the four different packets are arranged in the order of "'0111," "1011," "1101," and "1110" for pk_1 to pk_4, respectively. Thus, the data packets are arranged such that they are intended for output Ports 1 to 4 in consecutive order. The data packet payload is 48 bits long. The bit period at the payload is 100 ps long corresponding to a payload rate of 10 Gb/s. The guard period is 800 ps long. The payload length is chosen for convenience and in principle it can be hundreds of thousands of bits long. The guard period is limited by the rise time and fall time of the control signal and can be further reduced. The header of the control signal is "0100" which corresponds to the complement of the address of output Port 2 of the 1×4 switch.

Fig. 4(a) and (b) shows the synchronized timing diagrams of the data packets and the control signals at the input of the FP-LD. Fig. 4(c) and (d) shows the zoom-in synchronized timing diagrams of the data packet headers and the control signal headers for four consecutive packets. Note that the "1" bit in the control signal is aligned with the "0" bit in the data packet header for pk_2 only. Fig. 4(e) and (f) shows the switched output of the data packet at 3 and 1 ns/div, respectively. We observed that when the header of the data packet matches with that of the control signal, i.e., pk_2 only, the FP-LD transmits the data packets and otherwise blocks the packets. However, because of the finite response time of the FP-LD, part of the address headers of the blocked data packets, i.e., pk_1, pk_3, and pk_4, are able to pass through the FP-LD before injection-locking by the control signal header at λ_c can take place [shown by dashed circles in Fig. 4(e) and (f)]. In the experiment, the tolerance in wavelength and power for the control signal are about ± 0.05 nm and ± 1 dB and that for the data packets are about ± 0.02 nm and ± 3 dB, respectively. The extinction ratio of the output signal measured with an ac coupled receiver is $\sim$7.5 dB.

IV. Conclusion

We have demonstrated an all-optical packet switching with all-optical header processing using a single FP-LD. The header rate is at 5 Gb/s and the payload rate is at 10 Gb/s. The narrow injection-locking range of the FP-LD used ($<$0.3 nm) limits the maximum header processing and data rate to less than 40 Gb/s. The payload rate of the data will not be limited by the injection-locking range of FP-LD if the FP-LD is only used for header processing and control signal generation [5] while the switched control signal from the FP-LD output is used to switch the data packets using, for example, four-wave mixing or cross-gain modulation in a separate stage. Separating header processing and packet forwarding will also remove the residual header bits from the blocked data packets.

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