Nonvolatile multilevel memory effect by resistive switching in manganite thin films

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A planar multilevel memory structure is proposed and examined based on the resistive switching phenomenon in $La_{0.7}Sr_{0.3}MnO_3$ films with gold electrodes. Through the application of specific voltage pulses, such structures can be driven to well-defined intermediate resistance values. Samples were subjected to repeated switching cycles and prolonged reading processes to examine their durability during operations. Prescribed states of the samples could be retained after 10 000 switching cycles, and such states remained stable upon continuous probing. The proposed structure provides a simple scheme for the implementation of compact and nonvolatile multibit memory devices. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3043801]

I. INTRODUCTION

There is a continuous demand on increasing the data storage capacities of nonvolatile memories. Currently, such memory devices function on mechanisms such as magnetic hysteresis of domains or charge storage in capacitors. These structures will fail to work, as the feature dimensions continue to shrink (for example, due to superparamagnetism or charge leakages). Alternative nonvolatile memory schemes are therefore being actively sought after;[1] one of the candidates is the resistive switching phenomenon. Upon the application of a voltage pulse, the resistance of a sample can be drastically changed, sometimes by orders of magnitude.[2] The effect has been manifested in various material systems,[3–7] either in planar[7] or capacitorlike geometries,[8–10] as well as in semiconducting junctions.[11]

On the other hand, typical binary data storage mechanisms hold information in either one of the two possible states ("1" and "0"). A more radical approach of increasing the storage capacity is to pack more data into each single memory component, thus allowing the expansion of storage capacities without reducing the feature dimensions. For implementation of such a multistate memory element, it must possess some intermediate states which are stable enough to retain the information. Besides, such states have to be reproducible over repeated read/write processes.

Indeed there are studies that suggest the potential of resistive switching effect to settle at some metastable states. Watanabe *et al.*,[12] for example, applied current pulses across single crystals of Cr-doped $SrTiO_3$ (STO) and obtained clearly distinguishable resistance levels. Their measurements, however, have been repeated for less than 10 switching cycles. Besides, their results were obtained from single crystals of doped STO, making it hard to be employed for memory applications.

More promising approaches arise from thin film-based devices, which are more compatible with the current microelectronics technology. Shang *et al.*,[8] for example, presented *I-V* measurements with varying maximum ramping voltages in $La_{0.7}Ca_{0.3}MnO_3$-based capacitorlike structures. Hysteretic *I-V* behaviors were observed in all cases, and interestingly the current returned to zero along different paths. The results implied that different sample resistances could be achieved, depending on the voltages previously applied across the electrodes immediately before measurements. Such a multilevel switching behavior was indeed demonstrated in a recent work by the same group.[9] Similar effect has also been shown by Oligschlaeger *et al.*[10] in a capacitor structure, with $Ba_{0.7}Sr_{0.3}MnO_3$ as the spacer. Disappointingly, the switching among multiple levels has been demonstrated only for tens of times in both works, failing to address the issue concerning the reproducibility of multistate memory effect. Besides, these works are based on heterostructures with the functional epitaxial oxide films grown on either metal[8,9] or oxide[10] electrodes at elevated temperatures. Such conditions are not appropriate for industrial applications. Besides, differences in preparation conditions can lead to variations in interface structures, film crystallography, and electronic states in different works, complicating the interpretation of results.[13]

Here we demonstrate a multibit nonvolatile memory structure based on resistive switching effect in manganite thin films using a planar device geometry. By the application of suitable voltage pulses, $La_{0.7}Sr_{0.3}MnO_3$ (LSMO) films with photolithography-prepared Au electrodes can exhibit metastable resistive values that are reproducible for at least 10 000 cycles. Repeated probing of resistances at various states suggested the durability of the structure. Such features, together with its simplicity in fabrication and compatibility with current device technologies, highlight the potential of perovskite resistive switching elements for nonvolatile memory applications.

II. EXPERIMENNTAL DETAILS

LSMO films were deposited on single crystal $LaAlO_3$ (001) substrates by pulsed laser deposition (PLD).[14] In this work, the substrate temperature and oxygen pressure were

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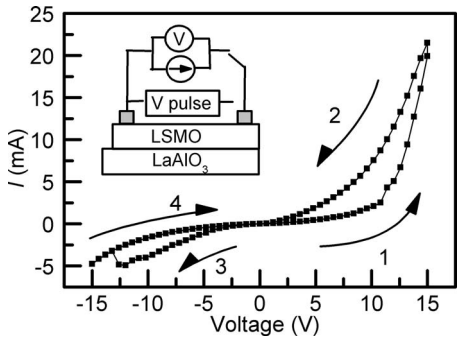

FIG. 1. *I-V* characteristics of a Au–LSMO–Au structure. Inset: schematic of the measurement geometry for read/write tests.

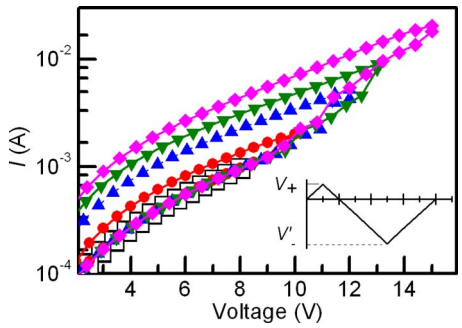

FIG. 2. (Color online) Semilog plot of minor-loop *I-V* curve in the positive voltage region. Plots were obtained by measuring the current across the sample between V_+ and V'_- (=−15 V) with the ramp profile, as illustrated in the inset. V_+ values used were 8 V (□), 10 V (●), 12 V (▲), 13 V (▼), and 15 V (♦).

750 °C and 300 mTorr. The laser repetition rate was 5 Hz. The thickness of LSMO films was ~300 nm. X-ray diffractometry indicated that such films were epitaxial. Subsequent to PLD deposition of oxides, circular Au metallic electrodes (diameter of 0.8 mm and thickness of 120 nm) were prepared on the film surfaces by lift-off technique. The minimum distance between electrodes was 20 μm.

Electrical measurements were performed at room temperature. Aluminum wires were ultrasonically bonded on the electrodes. A Keithley 2400 sourcemeter was used for the application of voltage signals with duration of 50 ms across the electrodes. Two-point resistances of the samples were measured using the current bias mode with a direct current of 100 μA. Given resistances of samples were generally smaller than 30 kΩ, the voltage generated was not expected to cause any effect on the switching behavior of the devices. The corresponding circuit diagram is shown in the inset of Fig. 1.

III. RESULTS AND DISCUSSION

A forming process was needed to prepare the samples for the experiment.[2] A negative voltage of −13 V was applied across the electrodes, which caused the resistance of sample to increase from ~300 Ω to the order of 20–30 kΩ. Figure 1 shows the *I-V* characteristics of the sample after forming. A clear hysteretic behavior is observed, similar to that reported in other systems.[8,12,15] As the voltage across the electrodes increases from zero (branch 1), the slope of the *I-V* plot is fairly gentle until ~10 V, at which the slope of the curve (i.e., differential conductance of the sample) suddenly increases. The voltage is subsequently ramped down to zero (branch 2). Note that the current across the sample retained a higher value compared to that of branch 1, suggesting a decrease in sample resistance. When the voltage drops below −12 V (branch 3), the size of current across the sample suddenly decreases. The current value then retains at a relatively small value (implying a higher resistance) when the voltage ramps back to zero (branch 4). For clarity, the same notations for various stages of *I-V* plots (branches 1–4) in Fig. 1 will be used throughout the paper.

From the hysteretic behavior in Fig. 1, it would be expected that "minor loops" of *I-V* plots can yield similar hysteretic behavior.[8] Such minor loops can be obtained by ramping the voltage between a fixed negative voltage V'_- and a certain positive voltage V_+ (a schematic of the ramp function is plotted in the inset of Fig. 2). Here, V'_- was set at −15 V for two reasons. Unrecoverable sample damages could occur for voltage magnitude larger than 15 V; besides, no differences in sample resistances were observed by driving voltages below −15 V. To ensure identical starting conditions for the samples during minor loop measurements, the samples were pulsed at −15 V before a *I-V* minor loop was extracted. Selected *I-V* curves with different V_+ values are shown in a semilog plot in Fig. 2. Here we focus only on the positive branches (i.e., branches 1 and 2) of the *I-V* minor loops. As long as V_+ does not exceed 8 V, the *I-V* plots are completely reversible, and branches 1 and 2 basically overlap on one another. Starting from V_+=10 V onward, hysteresis sets in at both positive and negative branches of the plot. It should be mentioned that branch 1 of all *I-V* minor loops basically follows the same path. This confirms that the samples were starting from the same conditions at the beginning of the experiment, which was brought about by the application of −15 V "reset" voltage.

On the other hand, deviations can be observed among branch 2 of the *I-V* curves as the applied voltage returns to zero. As mentioned before, this result implies that multiple resistance values can be obtained from the same sample, depending on the V_+ value previously applied to the sample. This is illustrated in Fig. 3(a), in which voltage pulses of specific values (as labeled on the graph) are applied across the electrodes, followed by resistance probing of the sample. A minimum resistance value is obtained after a +15 V pulse is applied. As V_+ decreases, the resistance of the sample *gradually* increases to a maximum of about 9 V; this high resistance state can also be obtained by directly "resetting" the sample with a −15 V pulse, as explained previously. We also examined the response of the sample by resetting with +15 V pulses, followed by the application of varying negative voltage signals, the results are shown in Fig. 3(b). The resistance change could only take place if the negative pulse is larger than −12 V. More importantly, the maximum resistance is reached as the voltage reaches −14 V. The narrow voltage window for resistance control is undesirable for manifesting the multiple resistive states.

In any case, the results in Fig. 3 demonstrate that the resistance levels of the samples can be determined by the

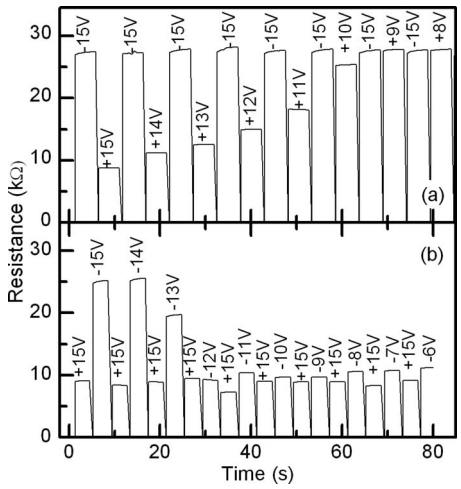

FIG. 3. Resistance of a device after the application of varying voltage pulses. Voltage pulses applied are as labeled in the figure. (a) Cycling between −15 V and varying positive voltages. (b) Cycling between +15 V and varying negative voltages.

magnitude of positive voltage pulses applied, after resetting with a large negative pulse. Indeed, we can arbitrarily determine the number of intermediate resistance states that can be obtained in such kind of resistive switching element, subjected to a number of limitations. Two of the crucial issues need to be addressed when deciding the number of possible states include the reproducibility of each single state (i.e., how likely the same resistance level can be obtained by the application of the same positive voltage pulse) and the stability of individual states upon repeated measurements.

To this end, we subjected a sample to a series of repeated pulses for 10 000 cycles with the following pulse pattern: $-15\ \text{V} \rightarrow +11\ \text{V} \rightarrow -15\ \text{V} \rightarrow +12\ \text{V}$. After the application of each pulse, the resistance of the sample was probed by switching to the measurement circuit in the inset of Fig. 1. In Fig. 4(a), we can see that various resistance states are well separated from each other. While we have just tested three separate states in this run, more resistive states can be designated by the application of suitable voltages. The fluctuation of resistances from the mean value is minimal, illustrating the (short-term) repeatability of the states. An undesirable feature, as observed from the figure, is the continuous rise in resistance with the continuous application of pulses. Clearly further investigations are necessary to improve the long-term stability of the devices.

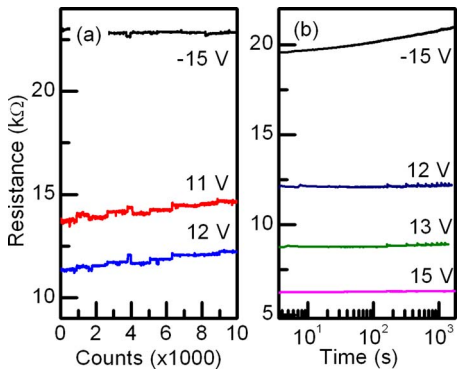

FIG. 4. (Color online) Performance of Au/LSMO/Au planar devices. (a) Device resistance upon repeated cycling of voltage sequence: $-15\ \text{V} \rightarrow +11\ \text{V} \rightarrow -15\ \text{V} \rightarrow +12\ \text{V}$. (b) Stability of resistance states in another sample after pulsing at specific voltages, as labeled in the figure.

Finally, we tested the durability of the samples upon prolonged probing of resistances, which is shown in Fig. 4(b). The resistances were seen to be fairly stable over the period (~30 min) of measurements. While there is a trend for the resistance of reset state (i.e., highest resistance condition) to increase with time, various resistance states are definitely well separated from one another. This, together with the results in Fig. 4(b), suggests the possibility of repeatable and stable memory state in a single device. To definitely prove the usefulness of the resistive switching effect as applied for multistate nonvolatile memories, they have to be subjected to standardized tests generally applied on memory devices.

A few points concerning the proposed multilevel resistive switching elements are worth mentioning. Once an intermediate resistive state is reached by the application of a positive pulse V, there are two possible ways to drive it away from the metastable state. A large negative reset pulse can be applied to drive the element back to the high resistive state. Alternatively, a positive voltage pulse that is larger than V can be used to further reduce the resistance of the structure. Various models have been proposed to explain the origin of resistive switching effect.[16–18] Szot *et al.*[16] observed the conducting paths along dislocations in single crystal $SrTiO_3$ samples, directly supporting the filamentation model. Qualitative explanation of our results can be made based on this model. Resistive state of a sample is determined by the number density of conducting filaments that is present in the sample. Application of higher voltages (i.e., electric field) provides sufficient force to produce more of such paths. Destruction of paths has to be done by the application of a negative reset voltage, which destroys the (metastable) conducting paths. Changes in sample resistance can also be brought about by the increase in defect density through the application of higher positive voltage, or by completely erasing all the paths before the new ones are generated.

In our proposed scheme, the negative voltage is acting simply as a reset mechanism. The main reason was the narrow range of voltages that can be applied to change the resistance between various resistive states, as demonstrated in Fig. 3. The asymmetry between the positive and negative voltages has been previously observed.[19] At first sight it seems puzzling that such an asymmetry exists in our sample geometries, in which all of the electrodes were prepared on the same LSMO film. On the other hand, the forming process did provide the asymmetric initial conditions (in the form of a potential difference) across the electrodes. Janousch *et al.*[19] conducted thermal imaging on resistive switching Cr-doped STO samples, which did show the differences between the anode and cathode.

IV. CONCLUSIONS

To summarize, we have proposed the use of thin film resistive switching elements for multistate nonvolatile memory structures based on a planar measurement geometry. The simplicity of the setup, both in terms of sample prepa-

rations and reading/writing processes, should prove a great advantage for adoption into the current microelectronics technology. Repeated switching (over 10 000 times) among different resistance levels has been clearly demonstrated, faring closely to some existing multiple read-write memory technologies. Given the generality of resistive switching effect as observed in various types of insulators and structures, we believe that this scheme of multibit nonvolatile memory can be further optimized by the choice of suitable material and refined device geometries.

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