# A Novel Square-Wave Converter with Bidirectional Power Flow

H.L. Chan[1], K.W.E. Cheng[2] and D. Sutanto[3]

The Hong Kong Polytechnic University, Hung Hom, Hong Kong. Fax: (852) 2330-1544
Email: (1) eehlchan@inet.polyu.edu.hk
(2) eecheng@polyu.edu.hk
(3) eesutant@polyu.edu.hk

**Abstract - A novel ZVS phase-shift controlled bidirectional DC-DC convertor is proposed. It possesses the conventional features of phase-shifted convertors, including constant switching frequency, zero-voltage switching (ZVS) and voltage controlling by phase-shift. However, the new convertor has been improved by developing a bi-directional power flow capability and applying synchronous rectification, hence the on-state voltage drop of the active devices are small. Therefore it is recommended for use in electric vehicle (EV). In this paper, the principle of circuit operation of the proposed convertor was described in detail with mathematical calculations, and the experimental results were also given to verify the concept.**

## I. INTRODUCTION

In this paper, a novel bidirectional DC-DC convertor is proposed [1], which is an excellent candidate for high voltage and high power applications [2]-[5]. The newly developed bi-directional feature is especially useful for regenerative braking in EV, where the mechanical energy is converted into electrical energy by traction motor and then fed back into the batteries.

The converter employs the phase shift technique for voltage control; utilizes parasitic capacitance of active switches and leakage inductance of transformer for resonant switching; does not require a large filter inductor and applies the synchronous rectification [6]-[7] for bidirectional power flow.

The bidirectional phase-shifted DC-DC convertor is comprised of an inverter bridge ($Q_1$-$Q_4$) and a convertor bridge ($M_1$-$M_4$), which are connected with a high frequency power transformer. The 50% duty-ratio gate signals applied to the convertor bridge are synchronized with those applied to the left–leg of inverter bridge. Figure 1 shows the topology of the proposed convertor.

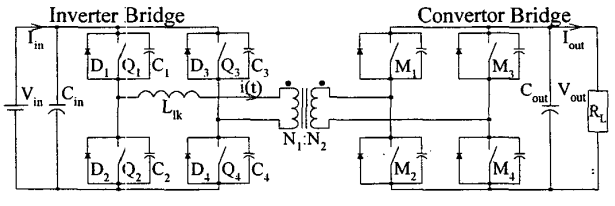


Figure 1: Bi–Directional Phase–Shift DC–DC Converter

All the active switches in both the inverter and convertor bridges are identical, each of them consists of a MOSFET, a body diode and a capacitor. The capacitors, $C_1$-$C_4$, represent the sum of stray capacitance of the MOSFET and an additional resonant capacitor. $L_{lk}$ is the total leakage inductance of the transformer's primary and secondary windings. $C_{in}$ and $C_{out}$ are the input and output filter capacitors.

## II. OPERATIONS OF THE CIRCUIT

The operations of the proposed converter are different when the converter operates under light and heavy load conditions. Figure 2 shows the waveforms of the converter under the condition of light load, where the primary current of transformer is only sufficient to switch on $Q_3$ ($Q_4$ at negative cycle) under zero voltage. On the other hand, $Q_2$ ($Q_1$ at negative cycle) is turned on in a manner of hard switching, because the light load results in small primary current, which will flow in a reverse direction through the body diode of $Q_1$ ($Q_2$ at negative cycle) after the energy stored in the leakage inductance of transformer is empty.

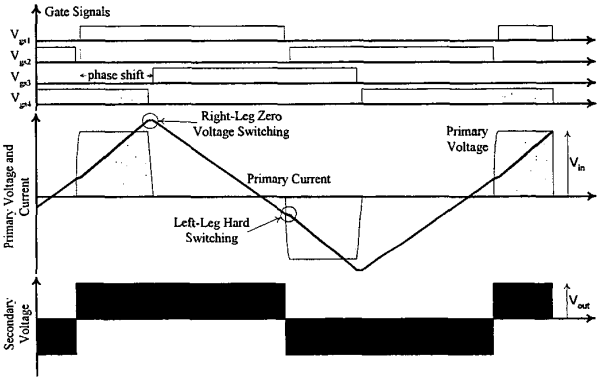


Figure 2: Circuit Operation under Light Load Condition

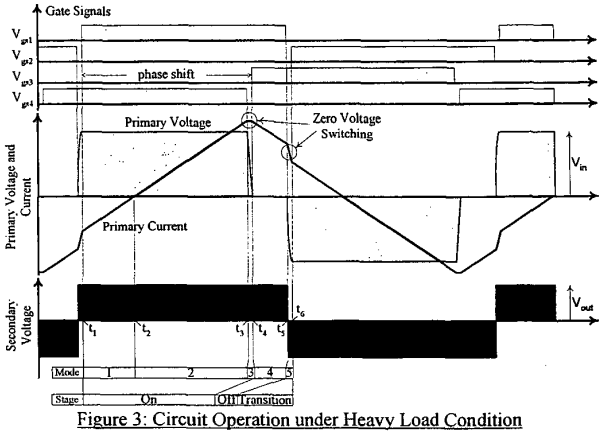


Figure 3: Circuit Operation under Heavy Load Condition

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Under the heavy load condition, the converter can thus operate under ZVS for all active switches as shown in Figure 3, which also illustrates the complete cycle of operation for the proposed converter. $V_{gs1}$ to $V_{gs4}$ are gate signals applied to the switches $Q_1$ to $Q_4$. In addition, $V_{gs1}$ is also used to drive $M_1$ and $M_4$, $V_{gs2}$ to drive $M_2$ and $M_3$, such that the converter bridge can operate in a manner of synchronous rectification. The synchronous rectification allows the converter to have low on-state loss and ease of control at the transistors $M_1$ to $M_4$.

The positive half cycle is the same as the negative half cycle except the signs of voltage and current are reversed, so only the positive half cycle of circuit operation is explained here. The principle of circuit operation can be divided into the following five modes as shown in Figure 4a-e.

**Mode 1**: $Q_1$ and $Q_4$ are on. Source voltage $V_{in}$ is applied across the primary winding of transformer, and the secondary winding of transformer is clamped at the level of output voltage $V_{out}$, because $M_1$ and $M_4$ are on. As energy has been stored in primary and secondary leakage inductances of transformer during the previous mode of operation, then it is returned to the source.

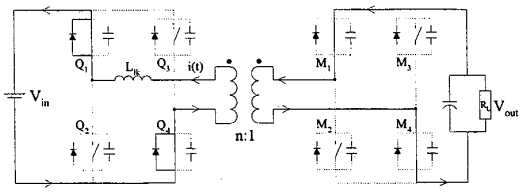


Figure 4a: Mode 1 of Operations

**Mode 2**: The difference between Mode 1 and Mode 2 is that the primary current is positive, or the source is charging up the leakage inductances of transformer with the same slope. In this mode of operation, the source is supplying energy to the load.

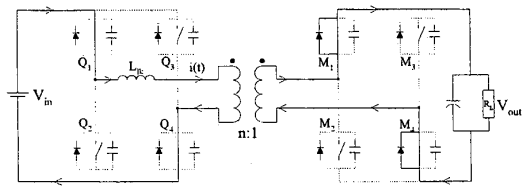


Figure 4b: Mode 2 of Operations

**Mode 3**: $Q_1$ remains on, but $Q_4$ is being turned off. Energy stored in leakage inductances is charging the parasitic capacitance of $Q_4$ (i.e. $C_4$) and discharging that of $Q_3$ (i.e. $C_3$). $D_3$ will conduct once the voltage across $C_3$ is zero. Subsequently, $Q_3$ is turned on under ZVS. It is clear that a dead time between turn-off of $Q_4$ and turn-on of $Q_3$ is requisite for $Q_3$ to achieve the ZVS.

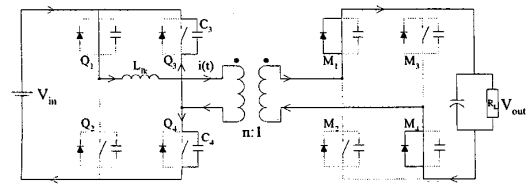


Figure 4c: Mode 3 of Operations

**Mode 4**: $Q_1$ and $Q_3$ are on. Energy in leakage inductances continues to deliver to the load, and the large output filter capacitor maintains the secondary side of transformer at voltage level of $V_{out}$.

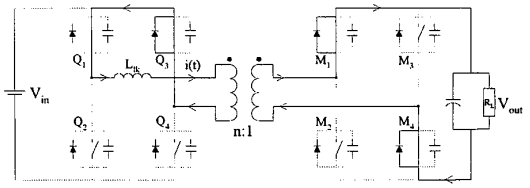


Figure 4d: Mode 4 of Operations

**Mode 5**: $Q_3$ remains on, but $Q_1$ is being turned off. $C_1$ is being charged up and $C_2$ is being discharged simultaneously by the energy stored in leakage inductances. Once voltage across $C_2$ reaches zero, $D_2$ conducts and $Q_2$ switches on under ZVS condition. Also a dead time between the turn-off of $Q_1$ and turn-on of $Q_2$ is required for ZVS of $Q_2$.

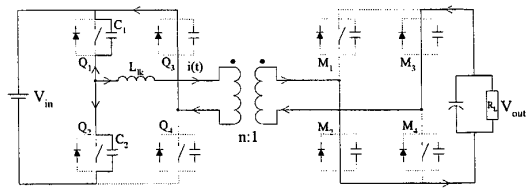


Figure 4e: Mode 5 of Operations

## III. MATHEMATICAL CALCULATIONS

In this section, we will calculate the requisite dead times for the operations of modes 3 and 5, and the DC characteristics of the converter as well. Some parameters are used, namely $D$ = phase shift, $n = N_1/N_2$ and $T$ = switching period. In addition, calculations were made in accordance with an assumption that the $C_{out}$ is sufficiently large to hold the $V_{out}$ at nearly constant.

**Left–Leg ZVS Transition**: $(t_5 < t \le t_6)$

It takes place in mode 5 operation, where $Q_1$ is being turned off and $Q_2$ is being turned on. To reset the duration of time $t_5 < t \le t_6$, we use $0 < t \le \delta_5 \frac{T}{2}$, and the equivalent circuit of this transition is shown in Figure 5.

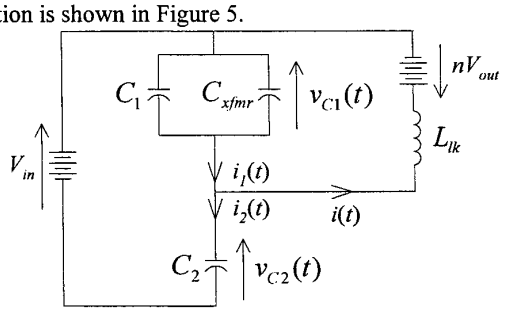


Figure 5: Left–Leg ZVS Transition

The initial and final states of circuit elements are given as:

$$v_{C1}(0) = 0, \qquad v_{C1}(\delta_5 \frac{T}{2}) = V_{in},$$

$$v_{C2}(0) = V_{in}, \qquad v_{C2}(\delta_5 \frac{T}{2}) = 0,$$

$$i(0) = i(t_5) = I_5, \qquad i(\delta_5 \frac{T}{2}) = i(t_6) = I_6.$$

The circuit equations can be obtained by KCL as follows:

$$V_{in} + nV_{out} + L_{lk}\frac{di(t)}{dt} = v_{C2}(t), \tag{1}$$

$$i_1(t) = (C_1 + C_{xfmr})\frac{dv_{C1}(t)}{dt}, \tag{2}$$

$$i_2(t) = C_2\frac{dv_{C2}(t)}{dt}. \tag{3}$$

Then, solving (1) to (3), and taking Laplace transforms with the initial values of $i(0^-)$ and $v_{C1}(0^-)$, we obtain

$$i(t) = -\frac{nV_{out}}{Z_{lef}t}\sin(\omega_{left}t) + I_5\cos(\omega_{left}t), \tag{4}$$

$$v_{C1}(t) = -nV_{out}[1-\cos(\omega_{left}t)] + I_5 Z_{left}\sin(\omega_{left}t), \tag{5}$$

where $\omega_{left} = \sqrt{\frac{1}{L_{lk}C_{left}}}$, $Z_{left} = \sqrt{\frac{L_{lk}}{C_{left}}}$ and $C_{left} = C_1 + C_2 + C_{xfmr}$.

For optimal design, simultaneously the voltages across $Q_1$ and $Q_2$ should be risen from 0V to $V_{in}$ and $V_{in}$ to 0V respectively after time $t = \delta_5 T/2$, which is the minimum dead time for left-leg ZVS transition. To evaluate $\delta_5 T/2$, we take the derivative of (5) with respect to $t$ and get:

$$\boxed{\delta_5\frac{T}{2} = \sqrt{L_{lk}C}\tan^{-1}\left(\frac{I_5 Z_{left}}{nV_{out}}\right)} \tag{6}$$

However, to ensure the current flowing in the leakage inductance of transformer is large enough to achieve the ZVS at left-leg, $v_{C1}(\delta_5 T/2)$ must be larger or equal to $V_{in}$. Then, we substitute (6) into (5) and evaluate $I_5$ that is the limit for the converter to achieve ZVS.

$$\boxed{\sqrt{\frac{V_{in}(V_{in}+2nV_{out})}{Z_{left}}} \le I_5}. \tag{7}$$

**Right–Leg ZVS Transition**: ($t_3 < t \le t_4$)

This transition occurs in mode 3 operation, where $Q_3$ is being turned on and $Q_4$ is being turned off. To reset the duration of time $t_3 < t \le t_4$, we use $0 < t \le \delta_3 T/2$, and Figure 6 shows the equivalent circuit of the operation.

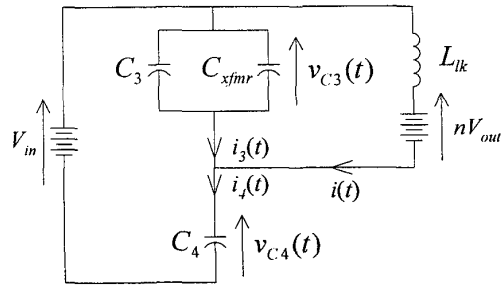


Figure 6: Equivalent Circuit of Right–Leg ZVS Transition

The initial and final states of circuit elements are given as:

$$v_{C3}(0) = V_{in}, \qquad v_{C3}(\delta_3 \frac{T}{2}) = 0,$$

$$v_{C4}(0) = 0, \qquad v_{C4}(\delta_3 \frac{T}{2}) = V_{in},$$

$$i(0) = i(t_3) = I_3, \qquad i(\delta_3 \frac{T}{2}) = i(t_3) = I_4.$$

The circuit equations can be obtained by KCL as follows:

$$V_{in} = L_{lk}\frac{di(t)}{dt} + nV_{out} + v_{C4}(t), \tag{8}$$

$$i_3(t) = (C_3 + C_{xfmr})\frac{dv_{C3}(t)}{dt}, \tag{9}$$

$$i_4(t) = C_4\frac{dv_{C4}(t)}{dt}. \tag{10}$$

Then, solving (8) to (10), and taking Laplace transforms with the initial values of $i(0^-)$ and $v_{C4}(0^-)$, we obtain

$$i(t) = \frac{V_{in}-nV_{out}}{Z_{right}}\sin(\omega_{right}t) + I_3\cos(\omega_{right}t), \tag{11}$$

$$v_{C4}(t) = (V_{in}-nV_{out})[1-\cos(\omega_{right}t)] + I_3 Z_{right}\sin(\omega_{right}t), \tag{12}$$

where $\omega_{right} = \sqrt{\frac{1}{L_{lk}C_{right}}}$, $Z_{right} = \sqrt{\frac{L_{lk}}{C_{right}}}$ and $C_{right} = C_3 + C_4 + C_{xfmr}$.

By comparing $v_{c4}(t)$ of (12) with $v_{c1}(t)$ of (5) and $i(t)$ of (11) with $i(t)$ of (4), we find that $\delta_3 T/2$ for $v_{c4}(t)$ resonating from 0V to $V_{in}$ is much shorter than $\delta_5 T/2$ for $v_{c1}(t)$ resonating from 0V to $V_{in}$ on the grounds of $(V_{in} - nV_{out}) > -nV_{out}$ and $I_3 > I_5$. In other words, the dead time $\delta_3 T/2$ for right–leg ZVS transition is much shorter than the dead time $\delta_5 T/2$ for left–leg ZVS transition.

Thus, (11) becomes

$$\boxed{I_4 \approx \lim_{\delta_3\frac{T}{2}\to 0} i\left(\delta_3\frac{T}{2}\right) = I_3}. \tag{13}$$

Since $I_3$ is always larger than $I_5$, and if the condition of (7) is fulfilled, then the ZVS at the right–leg will be definitely accomplished.

And (12) becomes

$$\Rightarrow \quad V_{in} \approx \lim_{\delta_3 \frac{T}{2} \to 0} v_{C4}\left(\delta_3 \frac{T}{2}\right) = \frac{I_3}{C_{right}}\left(\delta_3 \frac{T}{2}\right),$$

$$\therefore \quad \boxed{\delta_3 \frac{T}{2} = \frac{V_{in} C_{right}}{I_3}}. \tag{14}$$

Therefore, the minimum dead time for right–leg ZVS transition is $\frac{V_{in} C_{right}}{I_3}$.

**DC Characteristics**

To derive the DC characteristics of the converter, we re–arrange the circuit operations into three stages as follows:

**"On" Stage:** $(t_1 < t \le t_4)$ or $(t_4 - t_1 = D\frac{T}{2})$

Since modes 1 and 2 are identical when they are considered under circuit theory, and the primary current changes in mode 3 is small (i.e. $I_3 \approx I_4$ as indicated in (13)), so this stage includes modes 1, 2 and 3. In addition, we also neglect the dead time $\delta_3 \frac{T}{2}$ as it is insignificant when compared with $D$.

$$V_{in} - nV_{out} = L_{lk}\frac{di}{dt}$$

$$\Rightarrow \quad (V_{in} - nV_{out})\frac{DT}{2L_{lk}} = I_4 - I_1. \tag{15}$$

where $I_1 = i(t_1)$ and $I_4 = i(t_4)$.

**"Off" Stage:** $(t_4 < t \le t_5)$ or $t_5 - t_4 = (1 - D - \delta_5)\frac{T}{2}$

In this stage, the energy stored in leakage inductance of the transformer is freewheeling to drive the load, it operates in mode 4.

$$-nV_{out} = L_{lk}\frac{di}{dt}$$

$$\Rightarrow \quad -nV_{out}\frac{(1-D-\delta_5)T}{2L_{lk}} = I_5 - I_4. \tag{16}$$

where $I_5 = i(t_5)$.

**"Transition" Stage:** $(t_5 < t \le t_6)$ or $t_6 - t_5 = \delta_5\frac{T}{2}$

This stage is the changeover of the "Off" stage to the "On" stage, it is actually the mode 5 of operation.

$$-V_{in} - nV_{out} = L_{lk}\frac{di}{dt}$$

$$\Rightarrow \quad (V_{in} + nV_{out})\frac{\delta_5 T}{2L_{lk}} = I_1 + I_5. \tag{17}$$

where $I_6 = i(t_6) = -i(t_1) = -I_1$.

We solve (16) and (17),

$$\Rightarrow \quad \frac{V_{in}\delta_5 T + (1-D)nV_{out}T}{2L_{lk}} = I_1 + I_4. \tag{18}$$

The input energy $W_{in}$ to the converter during a half cycle is given by:

$$W_{in} = \int_0^{D\frac{T}{2}} i(t)\cdot V_{in}\cdot dt$$

$$\Rightarrow \quad W_{in} = (I_1 + I_4)V_{in}D\frac{T}{4}. \tag{19}$$

Then, substitute (18) into (19), and we get

$$W_{in} = \left(\frac{V_{in}\delta_5 T + (1-D)nV_{out}T}{2L_{lk}}\right)V_{in}D\frac{T}{4}.$$

And the output energy $W_{out}$ of the converter for a half cycle is obtained by:

$$W_{out} = \frac{T}{2}\cdot\frac{V_{out}^{\ 2}}{R_{Load}}.$$

Assumed that $W_{out} = W_{in}$,

$$\Rightarrow \quad \frac{T}{2}\cdot\frac{V_{out}^{\ 2}}{R_{Load}} = \left(\frac{V_{in}\delta_5 T + (1-D)nV_{out}T}{2L_{lk}}\right)V_{in}D\frac{T}{4},$$

$$\therefore \quad \boxed{\left(\frac{V_{out}}{V_{in}}\right)^2 - nkD(1-D)\left(\frac{V_{out}}{V_{in}}\right) - k\delta_5 D = 0}, \tag{20}$$

where $k = \frac{R_{Load}T}{4L_{lk}}$, and this is the voltage conversion ratio of the converter.

**Control Region**

Equation (20) indicates that $V_{out}$ is not directly proportional to the phase shift $D$, and it rather shows a second–order relationship between $V_{out}$ and $D$. In order to define a linear control region of phase shift for the converter, we then calculate a phase shift $D_{max}$ for the maximum output voltage.

Thus, differentiate $V_{out}$ by $D$ to obtain the maximum output voltage and get the $D_{max}$:

$$\boxed{D_{max} = \frac{nV_{out} + \delta_5 V_{in}}{2nV_{out}}}. \tag{21}$$

Therefore, the output voltage reaches its maximum when phase shift = $D_{max}$.

However, equation (7) sets a constraint for $I_5$ to exceed a minimum current in order for the converter to achieve ZVS, then we evaluate $I_5$ in term of phase shift.

First, we solve (15), (16) and (17) together, and get

$$\frac{(D+\delta_5)V_{in}T+(2\delta_5-1)nV_{out}T}{4L_{lk}}=I_5. \quad (22)$$

Then, put (22) into (7), and assumed that $D > \delta_5$ and $1 > 2\delta_5$, we get:

$$D_{\min} \geq \frac{4\sqrt{C_{left}L_{lk}}}{T}\sqrt{1+2\frac{nV_{out}}{V_{in}}}+\frac{nV_{out}}{V_{in}}. \quad (23)$$

This is the minimum phase shift for the converter to achieve ZVS.

By utilising the equations (20), (21) and (23), we can then design the proposed converter with a linear control region where the ZVS is ensured. Figure 7 demonstrates the typical DC characteristics and control region of the proposed converter.

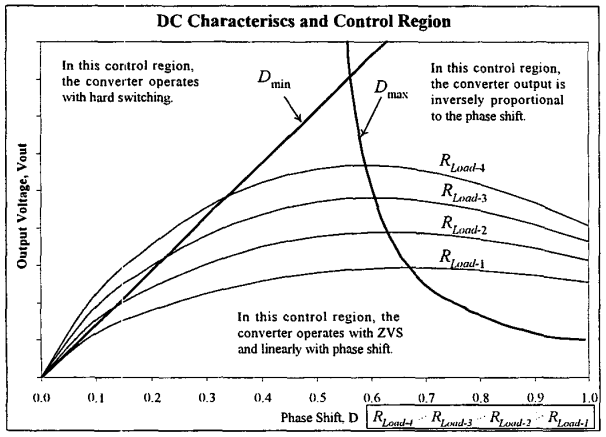


Figure 7: DC Characteristics and Control Region of the Proposed Converter

## IV. EXPERIMENTS

There were two experiments carried out to test the performance of the proposed convertor's efficiency and reverse mode of operation.

### Experiment A

A prototype of the proposed convertor was built up with the specifications: switching frequency of 100kHz, input voltage of 70V and output voltage of 30V. The circuit components included: all of MOSFETs ($Q_1$-$Q_4$ and $M_1$-$M_4$) are IRF530N, total leakage inductance ($L_{lk}$) of transformer's primary and secondary windings is 21.8μH, equivalent resonant capacitance ($C_1$-$C_4$) is 3.2nF, input and output capacitance ($C_{in}$ and $C_{out}$) are 5.4μF and 14.8μF respectively. Moreover, the power transformer was constructed using a bobbin of ETD49 and Ferrite core material of 3C85, its turn number of primary winding ($N_1$) and secondary winding ($N_2$) were 70 and 40 respectively.

Under the load range from 60W to 120W, the conversion efficiencies were measured and plotted in Figure 8. It is obvious that the overall efficiency of the proposed convertor is more than 91% over the specific load range.

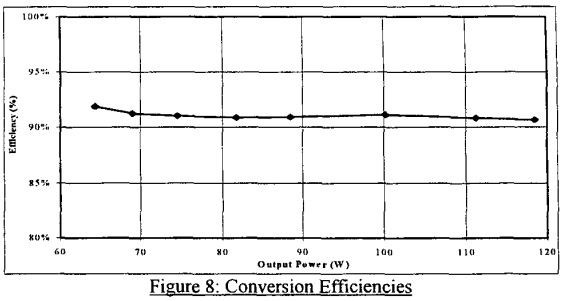


Figure 8: Conversion Efficiencies

The finding in Figure 9 and Figure 10 can be used to account for such high efficiency.

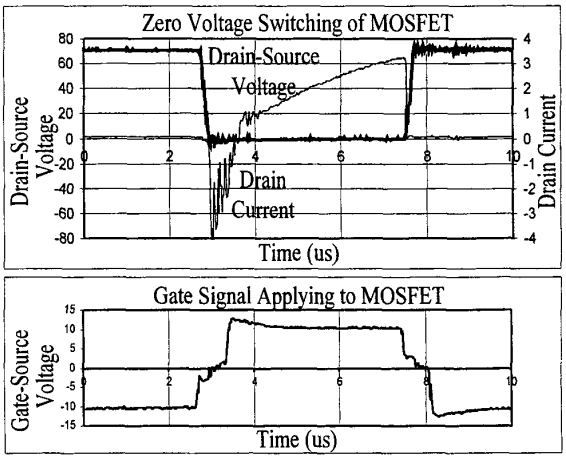


Figure 9: Zero-Voltage Switching of MOSFET $Q_4$

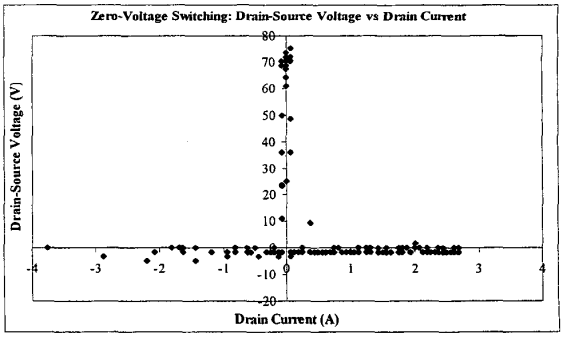


Figure 10: V-I of MOSFET $Q_4$

It was clearly shown that the drain-source voltage of $Q_4$ has been resonated to zero before the gate-source signal is applied. With the aim of this switching method, the switching losses of MOSFETs are minimized, and the overall efficiency of the convertor is maximized. The other MOSFET switching waveforms are similar.

### Experiment B

Another setup was used to test the performance of bidirectional power flow of the convertor.

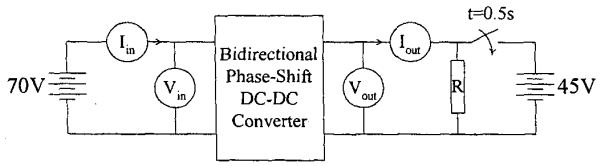


Figure 11: Testing Setup for Reverse Power Flow

As illustrated in Figure 11, the convertor first ran in forward mode with $V_{in}$ = 70V, $I_{in}$ = 1.08A, $V_{out}$ = 36V and $I_{out}$ = 1.95A. Then, at t = 0.5s, an external voltage source of 45V was applied momentarily to the output of the convertor to force reverse power flow. Consequently, the output current and input current flowed in reverse direction simultaneously with amplitude of 1.9A and 1.1A respectively, however, the input voltage almost kept constant at 70V either in forward and reverse operations. Figure 12 shows the changeover of operations.

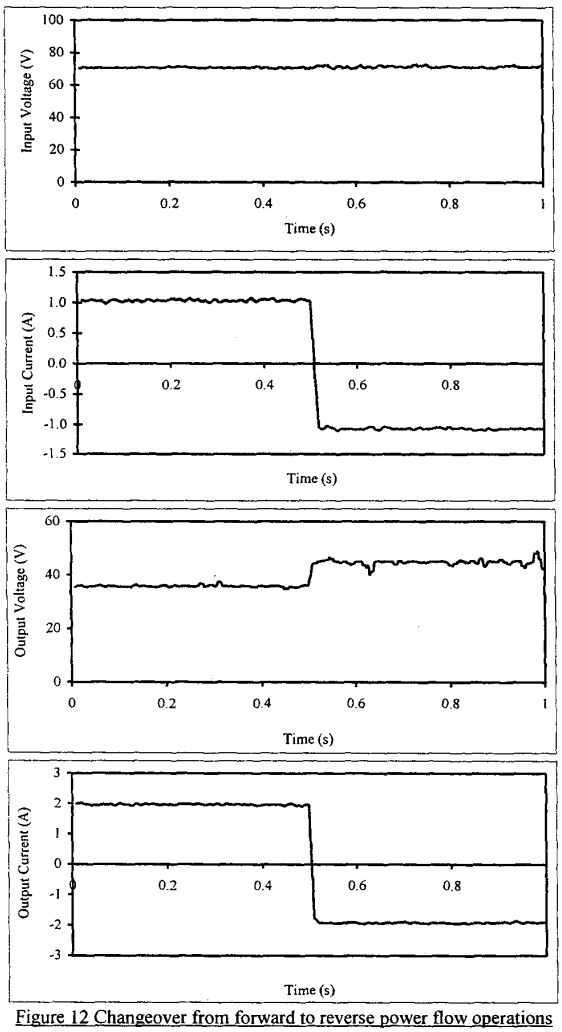


Figure 12 Changeover from forward to reverse power flow operations

## V. CONCLUSION

A novel bidirectional phase-shift controlled DC-DC convertor was proposed. The converter uses leakage inductance of the transformer and parasitic capacitance of active switches to perform resonant switching. All the active switching devices are switched at zero voltage switching. The proposed convertor, if employed in EV, is capable of not only transferring energy from EV batteries to powertrain for motoring, but also returning energy back into batteries in case of regenerative braking.

Moreover, by making use of a simple drive circuit for the convertor bridge, it can gain the benefit of synchronous rectification.

## ACKNOWLEDGEMENTS

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