An Autonomous Current Balancing Method for Interleaved DC/DC Converter in Wireless Power Transfer Systems

Zixuan Xu, *Student Member, IEEE,* Menglin L.N.Chen, *Senior Member, IEEE,* Kerui Li, *Member, IEEE,* Minghao Wang, *Senior Member, IEEE,* Xinyang Su, *Student Member, IEEE*, and Zhao Xu, *Senior Member*, *IEEE*

***Abstract*—Interleaved DC/DC converters are commonly used in high-power wireless power transfer (WPT) systems to manage the high charging currents and voltages. However, interleaved DC/DC converters in these systems suffer from current imbalances, causing inefficiencies and unreliability due to uneven thermal distribution and current stress. In this paper, an autonomous current balancing method is proposed for two-phase interleaved DC/DC converter-based WPT systems with a split input configuration. The method is mathematically proven to be generally applicable to WPT systems with interleaved DC/DC converters, enabling flexible deployment across applications with varying power levels, load conditions, and converter configurations. A small-signal model-based control strategy is developed to ensure fast dynamic responses and high robustness of the system against disturbances. The proposed method is validated through mathematical analysis, simulation comparisons, and laboratory experiments, confirming its effectiveness in both steady-state and dynamic operations of the WPT system.**

***Index Terms*—Wireless power transfer, interleaved DC/DC converter, two-stage rectifier, autonomous current balancing**

I. Introduction

In recent years, wireless power transfer (WPT) systems have proliferated rapidly. The WPT technology has been evolving for high-power applications, such as industrial automation [1], electric vehicle charging [2], and railway systems [3]. Conventionally, two-stage AC–DC rectifiers are commonly employed in WPT systems. They are typically composed of a diode bridge followed by a single-phase DC/DC converter. This topology can achieve high power conversion efficiency and provide a wide output voltage regulation range [4]-[8]. However, single-phase DC/DC converters are not suitable for high-power applications. They suffer from elevated voltage and current stress on semiconductor devices and reactive components, limiting the output capability and requiring a bulky output filter for handling high current ripples.

To address these issues, interleaved DC/DC converters are considered as a more feasible solution in WPT charging systems [3] [9]-[13]. By utilizing multiple converter modules with phase-shifted pulse-width modulation (PWM), interleaved DC/DC converters can minimize component stress while enhancing output current capability. Additionally, the size of the output filter is significantly reduced due to the increased frequency of the current ripple [14-21]. Despite these inherent advantages, current imbalances of interleaved converters will lead to asymmetries among different phases, consequently resulting in high thermal stress for switches due to the uneven current delivery. This accelerated heating shortens device lifetime and reduces reliability. Imbalances also create unequal voltage stress across switches. Traditional approaches to balancing phase currents generally rely on the control of individual phase current or voltage, requiring the deployment of extra current or voltage sensors [22]-[28] and escalating the costs. To reduce the component cost, recent research has focused on single-sensor and sensor-less current balancing methods with the introduction of current estimation techniques. In [29]-[30], the inductor currents are estimated by analyzing the correlation between the output voltage ripple and the phase current distribution. This simplifies the current balancing process by eliminating the need for current sensors. A sensor-less current balancing method is reported in [31], where phase currents are estimated indirectly by identifying the series resistance ratio (SRR) of each phase. This method can achieve current balance through duty cycle adjustment without additional current sensors. Furthermore, in [32]-[34], a single-sensor sampling strategy is applied, in which diode current measurements are used to estimate the average inductor current. Despite their advantage of sensor reduction, these approaches heavily rely on accurate parameter estimation and involve complex control implementations, making them infeasible for practical and low-cost microcontroller-based applications.

In light of these challenges, a fundamentally different method is proposed in this paper with the following key contributions.

1. The proposed method can achieve autonomous current balancing through the inherent coupling between the DC-link capacitors' voltage and inductors' current by the novel topology, thereby eliminating the need for dedicated balancing

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Zixuan Xu, Menglin L.N.Chen, Xinyang Su, and Zhao Xu are with the Department of Electrical and Electronic Engineering, The Hong Kong Polytechnic University, Hong Kong 999077, SAR, China (e-mail: zixuan.xu@connect.polyu.hk; menglin.chen@polyu.edu.hk; xinyang.su@connect.polyu.hk; eezhaoxu@polyu.edu.hk).

Kerui Li is with the the Department of Electrical Engineering, City University of Hong Kong, Hong Kong SAR, China (e-mail: kerui.li@cityu.edu.hk).

Minghao Wang is with the State Key Laboratory of Internet of Things for Smart City and Department of Electrical and Computer Engineering, University of Macau, Macau 999078, SAR, China (e-mail: mhwang@um.edu.mo).

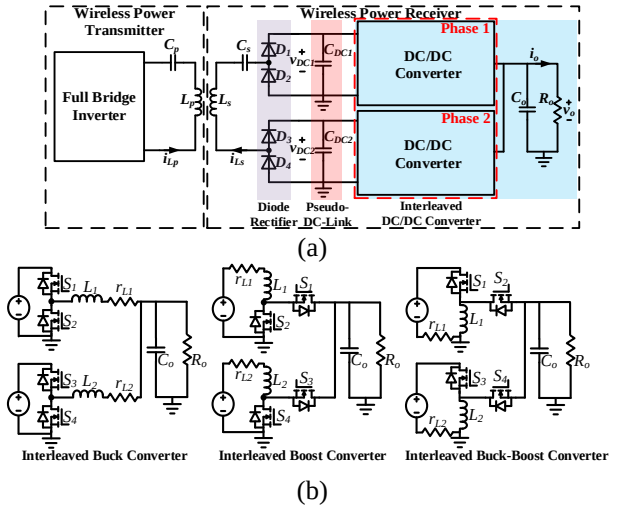

Fig. 1. (a) Circuit topology of the autonomous current balancing interleaved DC/DC converter-based WPT system. (b) Classical interleaved DC/DC converters.

sensors or complex balancing control schemes, and offering enhanced simplicity and robustness.

2. Different from most existing balancing methods focus on specific converter topologies. The proposed method is generally applicable to any interleaved DC/DC converter topologies used in WPT systems. This generality is analytically demonstrated and simulated, making the method highly versatile across different WPT applications.

3. To further improve system dynamic performance, a small-signal model-based PI control strategy with feedforward compensation is developed, which significantly enhances transient response and system robustness.

II. Autonomous Current Balancing Interleaved DC/DC Converter-based WPT System

A. Topology

Fig. 1(a) shows the circuit topology of the autonomous current balancing WPT system. The system consists of a power transmitter and a receiver. The transmitter is a full-bridge inverter generating a high-frequency AC current i_{Lp} that drives the resonant tank of compensation capacitor C_p and inductor L_p. The frequency of the i_{Lp} is designated as f_s. The receiver is a two-stage rectifier, including a diode rectifier, pseudo-DC-Link capacitors, and an interleaved DC/DC converter. The diode rectifier consists of four passive diodes D_1, D_2, D_3 and D_4. It converts AC power into DC and stores the energy on the pseudo-DC-Link capacitors C_{DC1} and C_{DC2}. The pseudo-DC-Link capacitors alternate in storing charge during the positive and negative half-cycles. When an imbalance occurs, a negative feedback mechanism corrects the imbalance through self-oscillation. The detailed balancing principle will be discussed in Section III. It is worth noting that, compared with the traditional DC bus structure, the pseudo-DC-link capacitor structure requires one more capacitor, and the total capacitance is doubled. Yet, this extra capacitor only slightly increases the volume and has negligible impact on the overall power density.

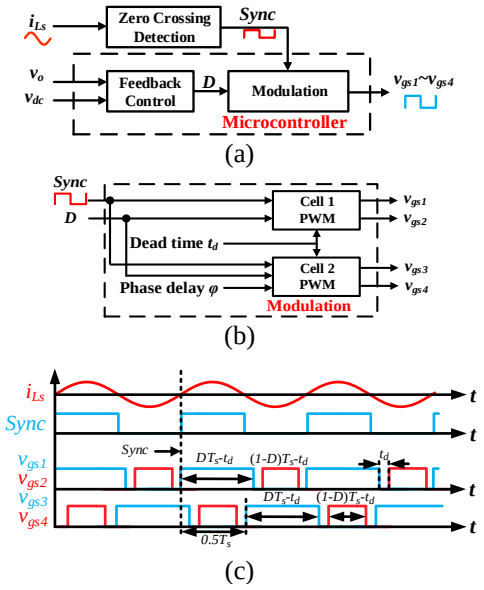

Fig. 2. Block diagram and key waveforms of the modulation scheme. (a) Synchronized modulation scheme with feedback control. (b) Detailed synchronized scheme. (c) Key waveforms of the modulation scheme.

The commonly used interleaved DC/DC converters are shown in Fig. 1(b). In this paper, an interleaved buck converter-based WPT system is analyzed as a general example. The proposed system consists of two complementary switch pairs, S_1, S_2 and S_3, S_4, two inductors L_1 and L_2 with equivalent series resistance r_{L1} and r_{L2}, an output capacitor C_o and a load R_o.

B. Modulation Scheme

To avoid the inherent beat frequency phenomenon in two-stage rectifiers in WPT system, a synchronized modulation scheme is employed in the proposed system [35]. The block diagram of the modulation scheme is shown in Fig. 2(a). Once the zero-crossing detection circuit detects that i_{Ls} turns to positive, a synchronization signal, $Sync$, is generated. Its rising edge are used to trigger the synchronized modulation scheme. Based on the detailed block diagram of the modulation scheme shown in Fig. 2(b), the phases of the drive signals are determined by the synchronous signal $Sync$, while the feedback control system establishes the duty ratios. Once the microcontroller receives the synchronous signal $Sync$, the drive signal V_{gs1} of S_1 is high, aligning its phase with $Sync$. The drive signal V_{gs2} of S_2 is complementary to V_{gs1}. The phase difference between the drive signal V_{gs3} of S_3 and V_{gs1} is set as 180° to achieve interleaved operation. The drive signal V_{gs4} of S_4 is complementary to V_{gs3}. The key waveforms are shown in Fig. 2(c).

The duty ratio of drive signals V_{gs1} and V_{gs3}, D, is given by the feedback control system to regulate the system output. Since V_{gs2} and V_{gs4} are complementary to V_{gs1} and V_{gs3}, their duty ratio is $1-D$. To avoid the simultaneous conduction of each complementary switches, a dead time t_d is introduced, so the duty ratios of each complementary drive signals are corrected

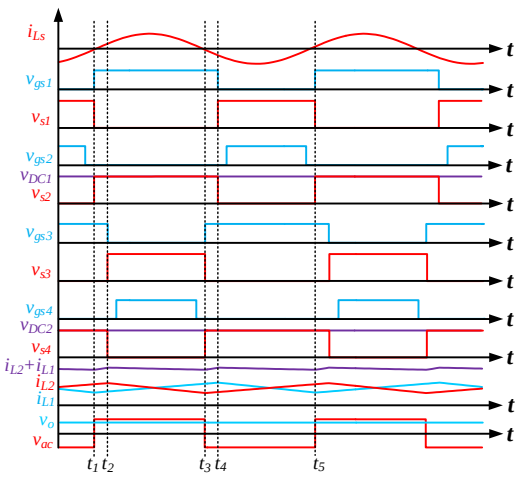

Fig. 3. Key waveforms of the proposed autonomous current balancing WPT system.

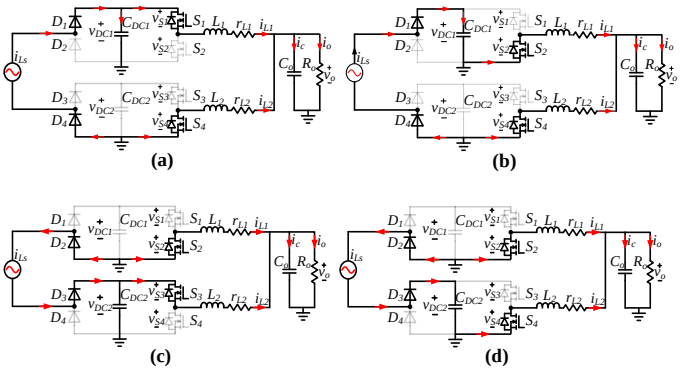

Fig. 4. Equivalent circuit under different operating states. (a) State I. (b) State II. (c) State III. (d) State IV.

to $D - t_d/T_s$ and $1 - D - t_d/T_s$, respectively.

C. Operation Principles and Steady-State Analysis

The equivalent circuit models of the proposed system under various operating states are provided in this section to illustrate its steady-state working principle. For simplified analysis, the transmitter and the receiver resonant cavities are equivalently expressed as an AC input current source i_{Ls}, and its amplitude is defined as I_{Ls} [36]. Hence, the AC input current source i_{Ls} can be expressed as

$$i_{Ls} = I_{Ls}\sin(2\pi f_s t). \tag{1}$$

The key waveforms of the system and the equivalent circuit models under various operating states are shown in Fig. 3 and 4, respectively.

For state I $[t_1 \le t < t_2]$, the equivalent circuit model is shown in Fig 4(a), and the corresponding waveforms of the system are shown in Fig. 3. At time t_1, i_{Ls} turns to positive, and the drive signal V_{gs1} turns high and S_1 is ON. Hence, the pseudo-DC-link capacitor C_{DC1} is being charged. Meanwhile, as i_{Ls} is in the positive cycle and switch S_3 is ON, the second pseudo-DC-link capacitor C_{DC2} is discharged by the output inductor L_2. The differential equations for pseudo-DC-link capacitors can be expressed as

$$\begin{cases} C_{DC1}\dfrac{dv_{DC1}}{dt} = i_{Ls} - i_{L1} \\ C_{DC2}\dfrac{dv_{DC2}}{dt} = -i_{L2} \end{cases} \tag{2}$$

During State I, the output inductors L_1 and L_2 are being charged by pseudo-DC-link capacitors C_{DC1} and C_{DC2} respectively. The differential equations for output inductors are

$$\begin{cases} L_1\dfrac{di_{L1}}{dt} = v_{DC1} - i_{L1}r_{L1} - v_o \\ L_2\dfrac{di_{L2}}{dt} = v_{DC2} - i_{L2}r_{L2} - v_o \end{cases} \tag{3}$$

The output capacitor C_o filters out the ripple of $i_{L1} + i_{L2}$ to get a smooth DC output current i_o, the differential equation for it can be written as

$$C_o\frac{dv_o}{dt} = i_{L1} + i_{L2} - \frac{v_o}{R} \tag{4}$$

For state II $[t_2 \le t < t_3]$: the equivalent circuit model is shown in Fig 4(b), and the corresponding waveforms of the system are shown in Fig. 3. At t_2, the driver signal V_{gs3} turns to low, S_3 is OFF, and no current flows through capacitor C_{DC2}. Meanwhile, C_{DC1} is charged by the input current source i_{Ls}. The differential equations for the two capacitors are

$$\begin{cases} C_{DC1}\dfrac{dv_{DC1}}{dt} = i_{Ls} - i_{L1} \\ C_{DC2}\dfrac{dv_{DC2}}{dt} = 0 \end{cases} \tag{5}$$

As S_3 is OFF, the inductor current i_{L2} freewheels through switch S_4. Meanwhile, the output inductor L_1 continues to be charged by capacitor C_{DC1}. The differential equation for inductor L_1 and L_2 can be expressed as

$$\begin{cases} L_1\dfrac{di_{L1}}{dt} = v_{DC1} - i_{L1}r_{L1} - v_o \\ L_2\dfrac{di_{L2}}{dt} = -i_{L2}r_{L2} - v_o \end{cases} \tag{6}$$

For state III $[t_3 \le t < t_4]$: the equivalent circuit model is shown in Fig. 4(c), and the corresponding system waveforms are shown in Fig. 3. During State III, i_{Ls} enters negative cycle, and drive signal V_{gs3} is high level, switch S_3 turns ON. Capacitor C_{DC2} is charged while C_{DC1} charges the inductor L_1. The differential equations for the two capacitors are

$$\begin{cases} C_{DC1}\dfrac{dv_{DC1}}{dt} = -i_{L1} \\ C_{DC2}\dfrac{dv_{DC2}}{dt} = -i_{Ls} - i_{L2} \end{cases} \tag{7}$$

The differential equations of L_1 and L_2 are

$$\begin{cases} L_1\dfrac{di_{L1}}{dt} = v_{DC1} - i_{L1}r_{L1} - v_o \\ L_2\dfrac{di_{L2}}{dt} = v_{DC2} - i_{L2}r_{L2} - v_o \end{cases} \tag{8}$$

For state IV $[t_4 \le t < t_5]$: the equivalent circuit model is shown in Fig. 4(d), and the corresponding waveforms of the system are shown in Fig. 3. At t_4, switch S_1 turns off, and no current flows through capacitor C_{DC1}, the inductor current i_{L1} freewheels through switch S_2. During State IV, the differential equations for capacitors C_{DC1} and C_{DC2} are

$$\begin{cases} C_{DC1}\dfrac{dv_{DC1}}{dt} = 0 \\ C_{DC2}\dfrac{dv_{DC2}}{dt} = -i_{Ls} - i_{L1} \end{cases} \tag{9}$$

The differential equations of L_1 and L_2 are

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = -i_{L1} r_{L1} - v_o \\ L_2 \frac{di_{L2}}{dt} = v_{DC2} - i_{L2} r_{L2} - v_o \end{cases} \tag{10}$$

D. Steady-State Model

In *Part C*, the duration of State I and State III is (D-0.5), while the duration of State II and State IV are (1-D). By applying the average switch model to the various operation states descripted in *Part C*, the steady-state model of the proposed system can be expressed as

$$\begin{cases} C_{DC1} \frac{dv_{DC1}}{dt} = \frac{I_{LS}}{\pi} - D i_{L1} \\ C_{DC2} \frac{dv_{DC2}}{dt} = \frac{I_{LS}}{\pi} - D i_{L2} \\ L_1 \frac{di_{L1}}{dt} = D v_{DC1} - i_{L1} r_{L1} - v_o \\ L_2 \frac{di_{L2}}{dt} = D v_{DC2} - i_{L2} r_{L2} - v_o \\ C_o \frac{dv_o}{dt} = i_{L1} + i_{L2} - \frac{v_o}{R_o} \end{cases} \tag{11}$$

When the system operates in steady-state, the differential terms in Equation (9) are all equal to zero, and the steady-state results can be expressed as

$$\begin{cases} \overline{i}_{L1} = \frac{I_{LS}}{D\pi} \\ \overline{i}_{L2} = \frac{I_{LS}}{D\pi} \\ \overline{v}_{DC1} = \frac{I_{LS} r_{L1} + 2 I_{LS} R_o}{\pi D^2} \\ \overline{v}_{DC2} = \frac{I_{LS} r_{L2} + 2 I_{LS} R_o}{\pi D^2} \\ \overline{v}_o = \frac{2 I_{LS} R_o}{\pi D} \end{cases} \tag{12}$$

III. Autonomous Current Balancing

In the previous section, the pseudo-DC-link capacitors structure was introduced. The mechanism of automatic current balancing enabled by the proposed method is analyzed in this section. The method is applied to three commonly used interleaved DC/DC converter-based WPT systems (buck, boost, and buck-boost) as examples. The validity of the autonomous current balancing mechanism is demonstrated through the negative feedback between the inductor current difference and the pseudo-DC-Link capacitors voltage difference. This mechanism is further validated through a mathematical model.

A. Autonomous Current Balancing Mechanism

The autonomous current balancing interleaved DC/DC converter-based WPT systems shown in Fig. 5 feature diode rectifiers and pseudo-DC-link capacitors structures. It is worth noting that this pseudo-DC-link structure can be applied to any WPT system with an interleaved DC/DC converter.

Assuming that all devices in the WPT system with interleaved buck converter are ideal, i.e., $C_{DC1} = C_{DC2} = C_{DC}$, $L_1 = L_2 = L$, and $r_{L1} = r_{L1} = r$. Then the differential equation for the system can be rewritten as

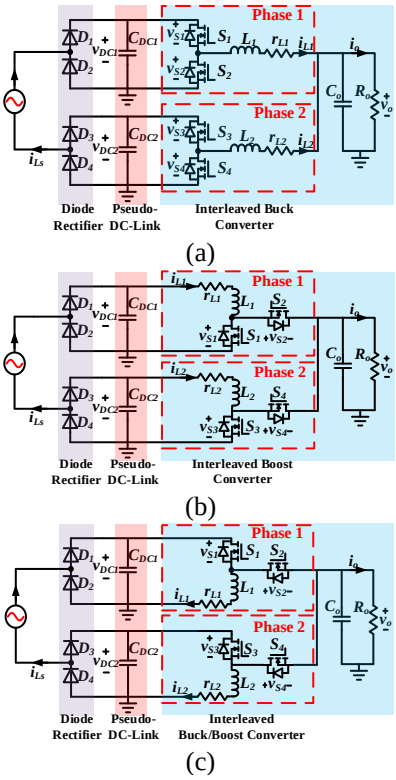

Fig. 5. Schematic of two-stage rectifier with different interleaved DC/DC converters. (a) Interleaved buck converter. (b) Interleaved boost converter. (c) Interleaved buck-boost converter.

$$\begin{cases} C_{DC} \frac{dv_{DC1}}{dt} = \frac{I_{LS}}{\pi} - D i_{L1} \\ C_{DC} \frac{dv_{DC2}}{dt} = \frac{I_{LS}}{\pi} - D i_{L2} \\ L \frac{di_{L1}}{dt} = D v_{DC1} - i_{L1} r_L - v_o \\ L \frac{di_{L2}}{dt} = D v_{DC2} - i_{L2} r_L - v_o \\ C_o \frac{dv_o}{dt} = i_{L1} + i_{L2} - \frac{v_o}{R_o} \end{cases} \tag{13}$$

Similarly, the differential equation for WPT system with an interleaved boost converter and buck-boost converter as equation (14) and (15), respectively

$$\begin{cases} C_{DC} \frac{dv_{DC1}}{dt} = \frac{I_{LS}}{\pi} - i_{L1} \\ C_{DC} \frac{dv_{DC2}}{dt} = \frac{I_{LS}}{\pi} - i_{L2} \\ L \frac{di_{L1}}{dt} = v_{DC1} - i_{L1} r_L + (1-D) v_o \\ L \frac{di_{L2}}{dt} = v_{DC2} - i_{L2} r_L + (1-D) v_o \\ C_o \frac{dv_o}{dt} = (D-1) i_{L1} + (D-1) i_{L2} - \frac{v_o}{R_o} \end{cases} \tag{14}$$

$$\begin{cases} C_{DC} \frac{dv_{DC1}}{dt} = \frac{I_{LS}}{\pi} - D i_{L1} \\ C_{DC} \frac{dv_{DC2}}{dt} = \frac{I_{LS}}{\pi} - D i_{L2} \\ L \frac{di_{L1}}{dt} = D v_{DC1} + (D-1) v_o - i_{L1} r_L \\ L \frac{di_{L2}}{dt} = D v_{DC2} + (D-1) v_o - i_{L2} r_L \\ C_o \frac{dv_o}{dt} = \frac{v_o}{R_o} - (1-D) i_{L1} - (1-D) i_{L2} \end{cases} \tag{15}$$

By rearranging differential equations in (11), the current difference ($i_{L1} - i_{L2}$) and voltage difference ($v_{DC1} - v_{DC2}$) in

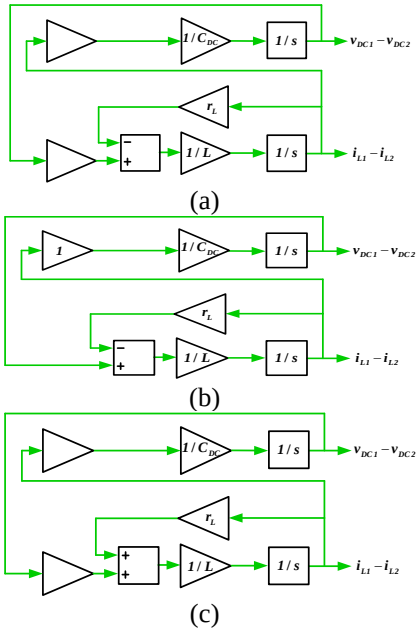

Fig. 6. Block diagram of the dynamics of voltage and current difference with different interleaved DC/DC converter. (a) Interleaved buck converter. (b) Interleaved boost converter. (c) Interleaved buck-boost converter.

the interleaved buck converter-based WPT system can be derived as follows

$$\begin{cases} C_{DC}\left(\frac{dv_{DC1}}{dt}-\frac{dv_{DC2}}{dt}\right)=-D(i_{L1}-i_{L2}) \\ L\left(\frac{di_{L1}}{dt}-\frac{di_{L2}}{dt}\right)=D(v_{DC1}-v_{DC2})-r_L(i_{L1}-i_{L2}) \end{cases} \quad (16)$$

As revealed by Equation (16), an imbalance between the inductor currents i_{L1} and i_{L2} triggers a negative feedback mechanism. When $i_{L1} > i_{L2}$, the voltage difference $v_{DC1} - v_{DC2}$ shifts in the direction， which leads to a reduction in v_{DC1}. This reduction results in negative feedback on i_{L1}, gradually decreasing i_{L1} to restore balance.

Similarly, the current and voltage difference in interleaved boost converter and buck-boost converter WPT system can be obtained by rearranging the differential equation (14) and (15) as

$$\begin{cases} C_{DC}\left(\frac{dv_{DC1}}{dt}-\frac{dv_{DC2}}{dt}\right)=-(i_{L1}-i_{L2}) \\ L\left(\frac{di_{L1}}{dt}-\frac{di_{L2}}{dt}\right)=(v_{DC1}-v_{DC2})-r_L(i_{L1}-i_{L2}) \end{cases} \quad (17)$$

$$\begin{cases} C_{DC}\left(\frac{dv_{DC1}}{dt}-\frac{dv_{DC2}}{dt}\right)=-D(i_{L1}-i_{L2}) \\ L\left(\frac{di_{L1}}{dt}-\frac{di_{L2}}{dt}\right)=D(v_{DC1}-v_{DC2})-r_L(i_{L1}-i_{L2}) \end{cases} \quad (18)$$

This autonomous balancing mechanism results from the inherent coupling between the DC-link capacitor voltages and inductor currents. It drives the system toward equilibrium by reducing the inductor current difference proportionally until balanced operation is restored. The block diagram of this coupled voltage-current dynamics mechanism is shown in Fig. 6, illustrating the interactive regulation process between Δi_L and Δv_{DC}.

B. Second-Order Oscillation Model

The following equation is obtained by reorganizing the dynamic formula for voltage and current differences in the interleaved buck converter-based WPT system

$$\begin{cases} C_{DC}L\frac{d^2(i_{L1}-i_{L2})}{dt^2}+C_{DC}r_L\frac{d(i_{L1}-i_{L2})}{dt}+D^2(i_{L1}-i_{L2})=0 \\ C_{DC}L\frac{d^2(v_{DC1}-v_{DC2})}{dt^2}+C_{DC}r_L\frac{d(v_{DC1}-v_{DC2})}{dt} \\ +D^2(v_{DC1}-v_{DC2})=0 \end{cases} \quad (19)$$

The autonomous voltage and current balancing process in the system can be represented as a second-order oscillation model shown in Equation (19). By applying the Routh-Hurwitz criterion, it is confirmed that all poles lie in the left-half plane, ensuring asymptotic stability. Essentially, any disturbance in the inductor currents or DC-link voltages is passively attenuated by the inherent negative feedback of the pseudo-DC-link capacitor structure.

The simulation and model analysis of the current and voltage autonomous balancing process are shown in Fig. 7. Under the defined operating conditions ($f_s = 200\text{kHz}$, $D = 0.7$, $I_{Ls} = 3\text{A}$, $C_{DC} = 10\mu\text{F}$, $C_o = 10\mu\text{F}$, $L = 50\mu\text{H}$, $r_L = 0.1\Omega$ and $R_o = 12\Omega$), there is close agreement between the simulated waveforms and model predictions. The close agreement between the simulated waveforms and model predictions demonstrates the validity of the second-order oscillation model

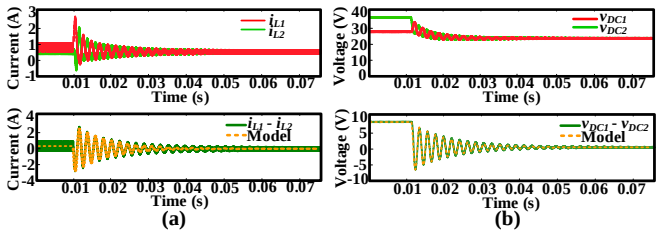

Fig. 7. Simulation and model-calculated waveforms of interleaved buck converter-based system. (a) Inductor Currents. (b) Pseudo DC-link capacitors voltages.

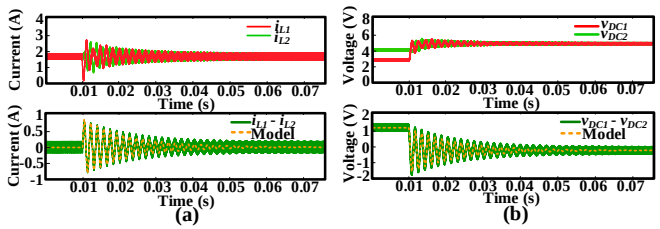

Fig. 8. Simulation and model-calculated waveforms of the interleaved boost converter-based system. (a) Inductor Currents. (b) Pseudo DC-link capacitors voltages.

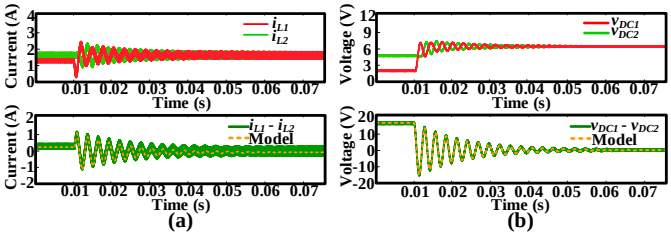

Fig. 9. Simulation and model-calculated waveforms of interleaved buck-boost converter-based system's current and voltage autonomous balancing (a) Inductor Current. (b) Pseudo DC-link capacitors voltage.

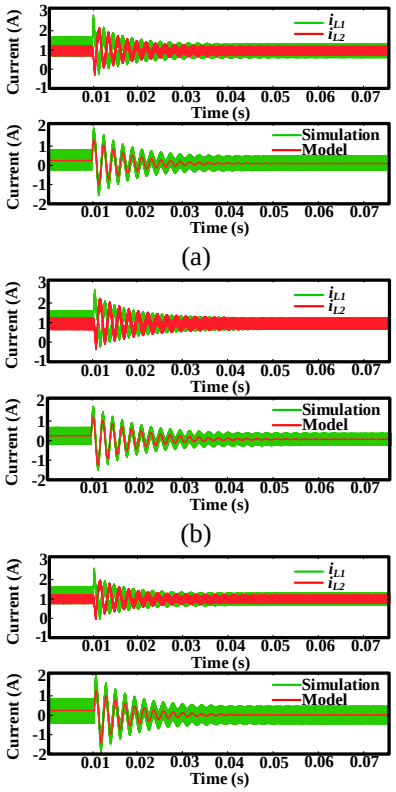

Fig. 10. The simulated and model-calculated waveforms of inductor currents balancing process under parameters mismatch conditions ($C_{DC1} < C_{DC2}$ and $L_1 < L_2$) (a) $L_1 = 33\mu H$, $L_2 = 50\mu H$. (b) $C_{DC1} = 8\mu F$, $C_{DC2} = 10\mu F$. (c) $L_1 = 33\mu H$, $L_2 = 50\mu H$ and $C_{DC1} = 8\mu F$, $C_{DC2} = 10\mu F$.

derived. It also confirms the effective autonomous current-sharing capability of the proposed methodology.

Similarly, by reorganizing the current and voltage difference equations for the interleaved boost converter and buck-boost converter-based WPT system, the second-order oscillation models for each system can be derived as follows:

$$\begin{cases} C_{DC}L\frac{d^2(i_{L1}-i_{L2})}{dt^2} + C_{DC}r_L\frac{d(i_{L1}-i_{L2})}{dt} + (i_{L1}-i_{L2}) = 0 \\ C_{DC}L\frac{d^2(v_{DC1}-v_{DC2})}{dt^2} + C_{DC}r_L\frac{d(v_{DC1}-v_{DC2})}{dt} \\ +(v_{DC1}-v_{DC2}) = 0 \end{cases} \quad (20)$$

$$\begin{cases} C_{DC}L\frac{d^2(i_{L1}-i_{L2})}{dt^2} + C_{DC}r_L\frac{d(i_{L1}-i_{L2})}{dt} + D^2(i_{L1}-i_{L2}) = 0 \\ C_{DC}L\frac{d^2(v_{DC1}-v_{DC2})}{dt^2} + C_{DC}r_L\frac{d(v_{DC1}-v_{DC2})}{dt} \\ +D^2(v_{DC1}-v_{DC2}) = 0 \end{cases} \quad (21)$$

The simulation and model analysis of the current and voltage autonomous balancing processes for these two systems are shown in Fig. 8 and Fig. 9, respectively. The simulation results and model analysis demonstrate the universality of the proposed method for the interleaved DC/DC converter in WPT system.

C. Influence on Parameter Mismatch

In practical circuits, the parameters asymmetry between each phase is common. Taking interleaved buck converter-based WPT system as an example, when the pseudo-DC-Link capacitance and the output inductance are mismatched (e.g. $C_{dc1} < C_{dc2}$ and $L_1 < L_2$), the differential equation for the system can be rewritten as

$$\begin{cases} C_{DC1}\frac{dv_{DC1}}{dt} = \frac{I_{LS}}{\pi} - Di_{L1} \\ C_{DC2}\frac{dv_{DC2}}{dt} = \frac{I_{LS}}{\pi} - Di_{L2} \\ L_1\frac{di_{L1}}{dt} = Dv_{DC1} - i_{L1}r_L - v_o \\ L_2\frac{di_{L2}}{dt} = Dv_{DC2} - i_{L2}r_L - v_o \\ C_o\frac{dv_o}{dt} = i_{L1} + i_{L2} - \frac{v_o}{R_o} \end{cases} \quad (22)$$

By solving the differential equation, the steady-state solution can be obtained as follows

$$\begin{cases} \bar{i}_{L1} = \bar{i}_{L2} = \frac{I_{LS}}{\pi D} \\ \bar{v}_{DC1} = \bar{v}_{DC2} = \frac{I_{LS}r_L + 2I_{LS}R_o}{\pi D^2} \\ v_o = \frac{2I_{LS}R_o}{\pi D} \end{cases} \quad (23)$$

Equation (23) shows that, in the steady state, the average value of the inductor currents remain balanced. When there is a difference in inductor currents, the dynamic expression of the balancing process can be expressed as

$$\Delta i_L(s) = i_{L1}(s) - i_{L2}(s) \quad (24)$$

where $i_{L1}(s)$ and $i_{L2}(s)$ are the zero-input response of the system with initial voltage and current difference. The detailed derivation and results of $\Delta i_L(s)$ are provided in *Appendix II*. Under parameter mismatch conditions, the autonomous current balancing process no longer follows a second-order oscillation model. Nevertheless, all coefficients in the characteristic equation remain positive. By applying the Routh–Hurwitz criterion, it is confirmed that all system poles lie in the left half-plane, ensuring asymptotic convergence.

To verify the aforementioned analysis, the current-balancing process is simulated under three parameter-mismatch scenarios. Namely, i) Inductance mismatch ($L_1 = 33\mu H$, $L_2 = 50\mu H$); ii) Capacitance mismatch ($C_{DC1} = 8\mu F$, $C_{DC2} = 10\mu F$); iii) Simultaneous inductance and capacitance mismatch. The simulated and model-calculated waveforms of the inductor currents balancing process are shown in Fig. 10. The simulated and model-calculated waveforms of the inductor currents balancing process are shown in Fig. 10. The two sets of waveforms agree closely in amplitude, phase, and settling behavior. This agreement verifies the model and validates the derived dynamic expression of the balancing process. These facts demonstrate that the proposed autonomous current-balancing method remains effective under parameter mismatch.

IV. Small Signal Model and Feedback Control Design

To improve the stability and reliability of the autonomous current-balancing WPT system, the small-signal model of the interleaved buck converter-based WPT system is analyzed in this section. A detailed feedback control strategy is then presented.

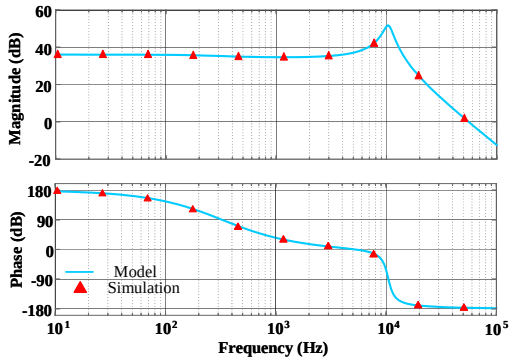

Fig. 11. Model-calculated and simulated Bode plots of small-signal response of output voltage $\hat{v}_o$ to duty cycle $\hat{d}$.

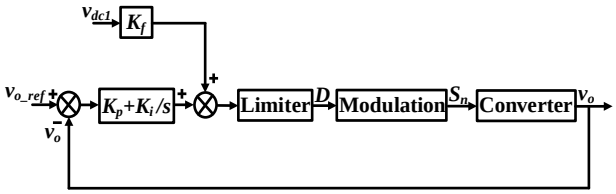

Fig. 12. Block diagram of proposed control strategy.

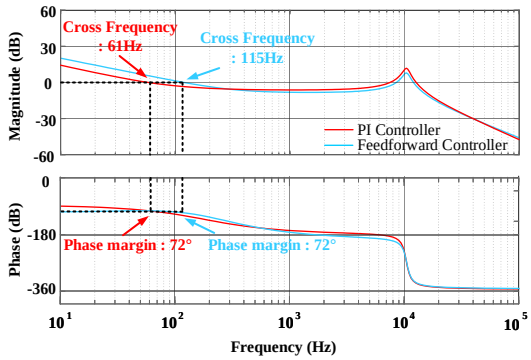

Fig. 13. Bode Plots of loop gains with proposed control method and PI-only method.

A. Small Signal Model

By linearizing the steady-state model of the proposed system, a small-signal model of the converter is derived. This model provides the foundation for analyzing system stability and designing a control strategy. The model and simulated analysis results of the output voltage response to duty ratio perturbations are compared in Fig. 11. The simulation parameters were set as follows: $f_s = 200\text{kHz}$, $D = 0.6$, $I_{Ls} = 3\text{A}$, $C_{DC} = 10\mu\text{F}$, $C_o = 10\mu\text{F}$, $L = 50\mu\text{H}$, $r_L = 0.1\Omega$ and $R_o = 12\Omega$. The response predicted by the small-signal model closely matches the simulation results, as seen in Fig. 11. This confirms the accuracy and reliability of the derived model, thereby demonstrating its suitability for further analysis and controller design.

B. Feedback Control Strategy

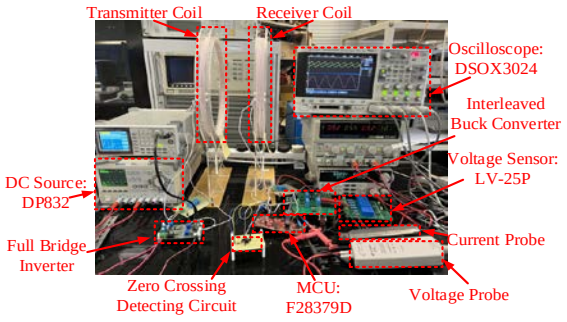

Fig. 14. Photograph of the experimental setup and prototype.

To regulate and achieve a stable output voltage, a Proportional-Integral (PI) controller is employed. Furthermore, to improve the system's transient response and reduce steady-state errors, a feedforward control strategy is introduced. The feedforward control utilizes the pseudo-DC-link capacitor voltage v_{DC1}, to anticipate disturbances and provide preemptive adjustments, thereby accelerating the system's response to changes in load or input conditions. The block diagram of PI with feedforward controller is shown in Fig. 12. In this diagram, v_{ref} is the reference of output voltage, v_o is the sampled value of output voltage, D is the duty ratio signal, k_f is the feedforward gain, k_p is the proportional gain, and k_i is the integrator gain. To ensure the fast response and sufficient stability margin of the system, the cross frequency and phase margin are set to 115Hz and 72°, respectively. The controller parameters of the system are determined by using the Ziegler–Nichols tuning method. For our proposed PI and feedforward control method, the gains are set as $k_f = 0.024$, $k_p = 0.012$, and $k_i = 12$. For comparison, a PI-only controller with identical phase margin is also tested. The crossing frequency is only 61Hz with the control parameters $k_p = 0.0108$, and $k_i = 8$. Fig. 13 shows the Bode Plots of loop gains with proposed control method and PI-only method. These results indicate that incorporating feedforward control can significantly enhance the transient response while maintaining the stability margin.

TABLE I.
SYSTEM SPECIFICATIONS OF THE EXPERIMENT SETUP

Description	Parameter	Value
Output Inductors	L_1, L_2	50μH
Inductor Equivalent Resistors	r_{L1}, r_{L2}	0.1Ω
Output Capacitors	C_o	10μF
Pseudo-DC-Link Capacitors	C_{DC1}, C_{DC2}	10μF
Output Resistance	R_o	12Ω
Switching frequency	f_s	200kHz

V. EXPERIMENTAL VERIFICATION

A prototype of the interleaved buck converter-based two-stage rectifier WPT system is built as a test bench. The hardware testing platform is shown in Fig. 14. The system's specifications are shown in Table I. The experimental waveforms are recorded by using the DSOX3024. LV-25P is

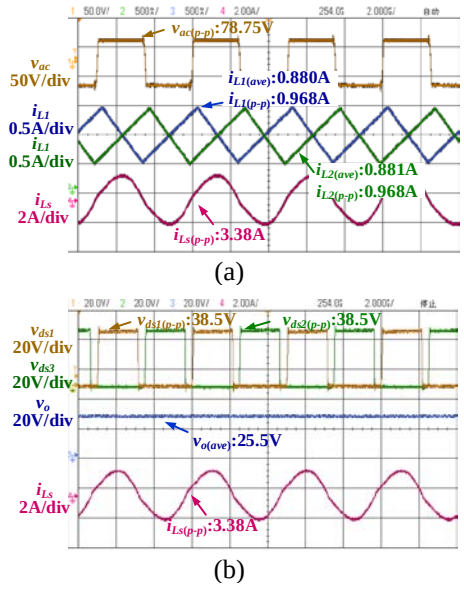

Fig. 15. Steady-state waveforms of the proposed system. (a) Waveforms of v_{ac}, i_{L1}, i_{L2}, and i_{Ls}. (b) Waveforms of v_{ds1}, v_{ds3}, v_o, and i_{Ls}.

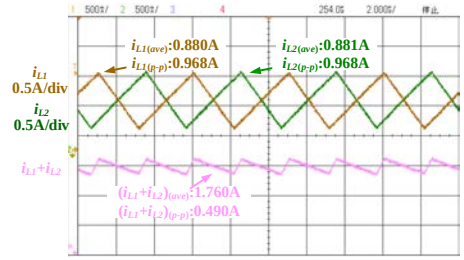

Fig. 16. Steady-state waveforms of two-phase inductor current i_{L1}, i_{L2} and calculated value of $i_{L1}+i_{L2}$.

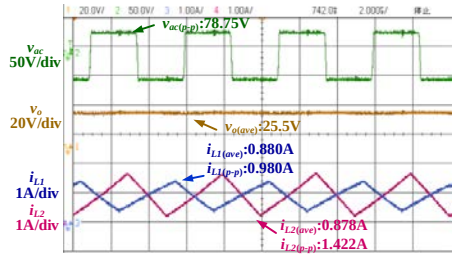

Fig. 17. Steady-state waveforms of proposed system with parameters mismatch.

used for the output voltage and pseudo-DC-Link capacitors voltage measurement. The receiver of the WPT system is controlled by a commercialized digital signal processor TMS320F28379D. The gate driver ADuM3223 is chosen to drive the power MOSFETs IPB057.

A. Verification of Steady-State Performance

The experimental results of the proposed system while operating under nominal conditions are shown in Fig. 15. The input voltage of two-stage rectifier v_{ac}, inductor currents i_{L1}, i_{L2} and input current i_{Ls} are recorded as shown in Fig. 15(a). It can be observed that the peak-to-peak value of input voltage v_{ac}

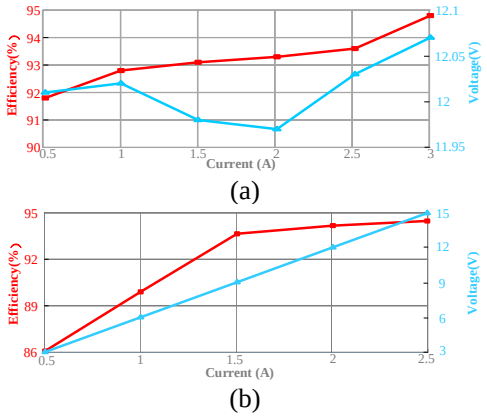

Fig. 18. (a) Measured efficiency of rectifier with constant output voltage. (b) Measured output power with constant load $R_o = 12\Omega$.

is 78.75V while the peak-to-peak value of input current i_{Ls} is 3.38A. The average value and ripple of inductor current i_{L1} is 0.880A and 0.968A, respectively. The average value and ripple of inductor current i_{L2} is 0.881A and 0.968A, respectively. It can be seen that the two-phase inductor currents i_{L1} and i_{L2} is quite close, suggesting that the autonomous current balancing has been successfully achieved under steady-state conditions. Further, the switch voltage v_{ds1} and v_{ds2} of switches S_1 and S_2, output voltage , and input current i_{Ls} are recorded as shown in Fig. 15(b). The peak-to-peak voltage across the switches is 38.5V while the system output voltage stabilizes at 25.5V.

Fig. 16 presents the two-phase inductor currents i_{L1}, i_{L2} along with the calculated sum of the currents, $i_{L1}+i_{L2}$. The dc average values of i_{L1} and i_{L2} are 0.880A and 0.881A respectively, while the current ripple values are 0.968A. The calculated sum of $i_{L1}+i_{L2}$ has a DC average value of 1.760A with current ripple value equal to 0.490A. This indicates that the total current ripple has been effectively reduced by 49% compared to the individual inductor currents, demonstrating a significant improvement in current stability.

To demonstrate robustness under parameter mismatch, Fig. 17 presents the steady-state behavior of the proposed system with mismatched parameters ($L_1 = 33\mu H$, $L_2 = 50\mu H$, $C_{DC1} = 10\mu F$, $C_{DC2} = 12\mu F$). The peak-to-peak value of the input voltage $v_{ac(p-p)}$ is 78.5V, and the average output voltage $v_{o(ave)}$ is 25.5V. These results are identical to those in Fig. 15. The average values of inductor currents $i_{L1(ave)}$ 0.880A and $i_{L2(ave)}$ 0.878A remain equal, confirming that the pseudo-DC-link topology still enforces accurate current sharing under mismatch conditions.

Steady-state performance at various operating conditions is evaluated, and the efficiency of the two-stage rectifier is measured and plotted in Fig. 18. The output voltage is regulated at 12V, and the output current I_o is varied from 0.5A to 3A (see Fig. 18(a)). The average efficiency over this range is 93.3%, and the maximum efficiency is 94.8% when the output current is 3A. Fig. 18(b) illustrates the measured efficiency with constant load $R_o = 12\Omega$, and the output voltage varies from 3V to 15V. The maximum efficiency is 94.6% when the output

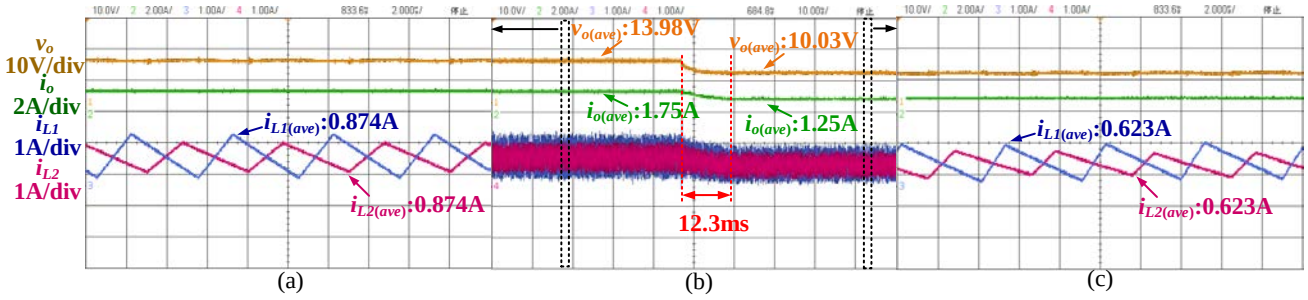

Fig. 22. Waveforms of the system in parameter mismatch condition with voltage changing from 14V to 10V. (a) zoom-in waveforms before step change. (b) step change process. (c) zoom-in waveforms after step change.

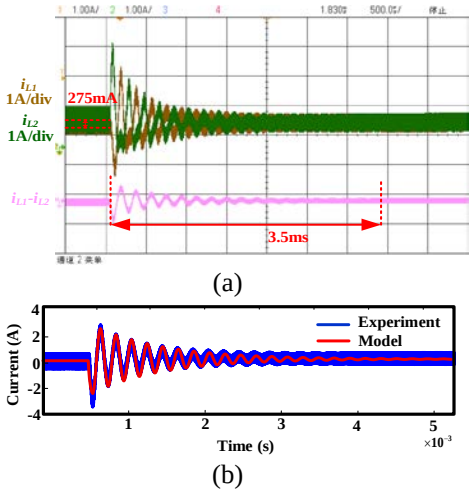

Fig. 19. Experimental and model-calculated results of autonomous current balancing process. (a) Experimental waveforms. (b) Experimental and model results of inductor currents difference.

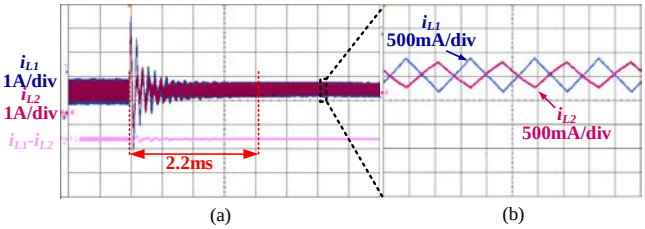

Fig. 20. Autonomous current balancing process under parameter imbalance. (a) Experiment waveforms of inductor currents. (b) Zoomed-in waveforms.

voltage is 15V. These results prove the two-stage rectifier maintain high efficiency across a wide range of operating points.

These experimental results confirm that the proposed WPT system, based on the interleaved DC/DC converter configuration, achieves a substantial reduction in current ripple while maintaining high output current capability. The system meets the contemporary demands for high current output, highlighting the effectiveness of the proposed autonomous current balancing method.

B. Verification of Autonomous Current Balancing

The waveforms of the autonomous current balancing process are shown in Fig. 19. Initially, the difference between the DC average values of two-phase inductor current i_{L1} and i_{L2} is 275mA. The waveform of the calculated current difference

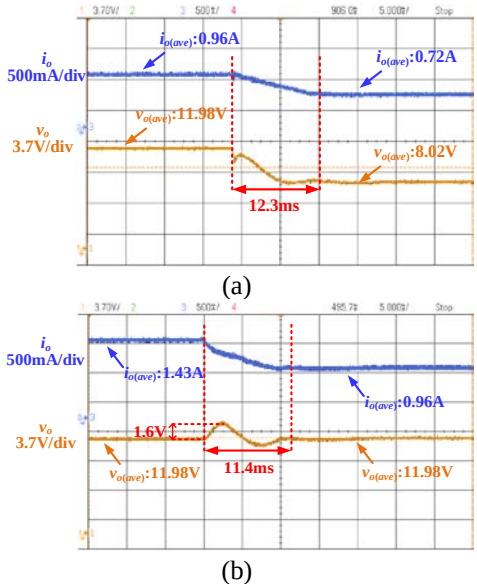

Fig. 21. Waveforms of the system operating with step change. (a) output voltage changes from 12V to 8V. (b) load changes from 12Ω to 8Ω.

$i_{L1} - i_{L2}$, shows that the current imbalance converges to zero after 3.5ms, as shown in Fig 19(a). Fig. 19(b) depicts the waveforms of the modeled and experimental results of inductor currents difference. The results from the experiment (blue trace) coincide with the model (red trace) throughout the transient and steady-state operations, quantitatively validating the accuracy of the model. These validate that the proposed pseudo-DC-Link method effectively achieves autonomous current balancing in the interleaved DC/DC converter-based WPT system.

To evaluate the autonomous current balancing performance under parameter mismatch conditions, the experiment is conducted. Fig. 20(a) illustrates the waveforms of inductor currents during the current balancing process. The current difference Δi_L is driven to zero within 2.2 ms. The zoomed-in waveforms shown in Fig. 20(b) confirm that after the balancing process, the average inductor currents are still the same, and the system operates in the steady-state region. These results prove that, even under significant inductor and capacitor tolerances, the proposed autonomous balancing method rapidly enforces equal current sharing without any active sensing or control compensation.

C. Verification of Dynamic Performance

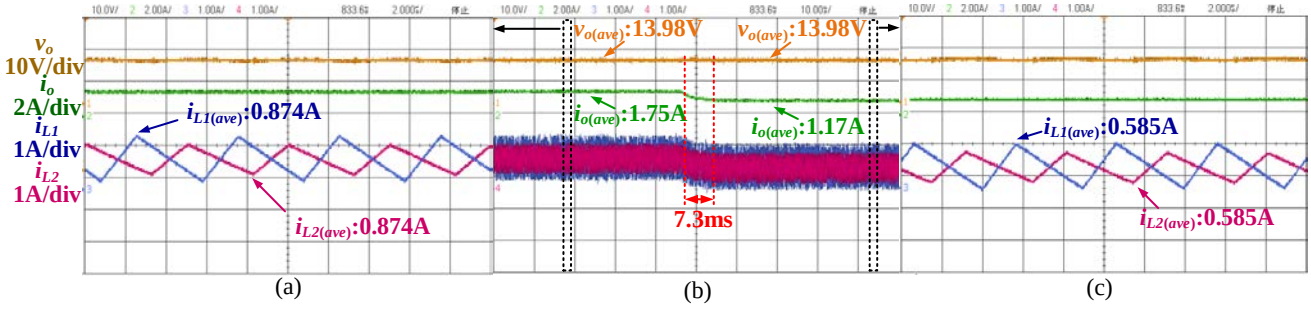

Fig. 23. Waveforms of the system in parameter mismatch condition with load changing from 8Ω to 12Ω. (a) zoom-in waveforms before step change. (b) step change process. (c) zoom-in waveforms after step change.

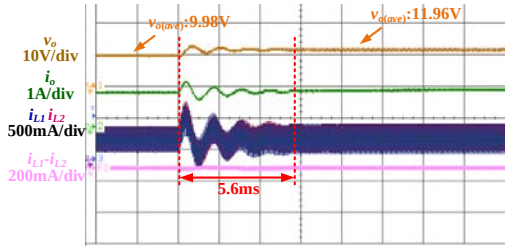

Fig. 24. Experiment waveforms of the system when output voltage steps from 10V to 12V.

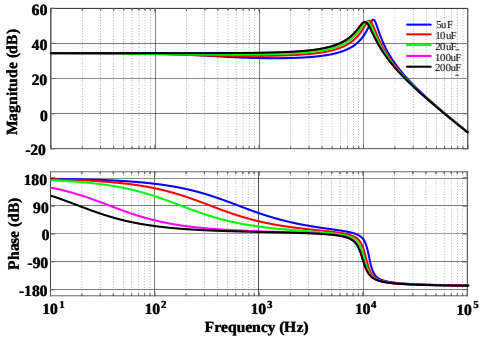

Fig. 25. Bode Plots of small-signal response of output voltage $\hat{v}_o$ to duty cycle $\hat{d}$ with different C_{DC}.

Dynamic responses to reference and load steps are presented in Fig. 21(a) and Fig. 21(b). The implemented parameters of the feedforward control scheme are set to $k_p = 0.032$, $k_i = 10.8$, and $k_f = 0.02$. Fig. 21(a) depicts the waveforms of the rectifier operating in response to the reference voltage step from 12 to 8V. After a settling time of 12.3ms, the output voltage is regulated from 11.98V to 8.02A. In the meantime, the output current is changed from 0.96A to 0.72A.

Fig. 21(b) shows load stepping from 8Ω to 12Ω. The controller maintains the output voltage at 12V while the output current steps from 1.43A down to 0.96A and the settling time is 11.4ms. During the transients, the output voltage overshoot is 1.6V. These dynamic results confirm the effectiveness of the proposed feedback control scheme.

Fig. 22(b) shows the waveforms when the reference voltage steps from 14 to 10V under component mismatch condition ($L_1 = 33\mu H$, $L_2 = 50\mu H$, $C_{DC1} = 10\mu F$, $C_{DC2} = 12\mu F$) with constant load 8Ω. After a settling time of 12.3ms, the output voltage is regulated to 10.03V and the output current changes from 13.98A to 1.03A. Figs. 22(a) and 22(c) provide zoom-in waveforms before and after the step change. In both cases, the average inductor currents remain identical. Fig. 23(b) presents the response when the load step from 8Ω to 12Ω, with the voltage reference fixed at 14V. The output voltage remains at 13.98V with a settling time of 7.3 ms, while the output current drops from 1.75A to 1.17A. Figs. 23(a) and 23(c) are the zoom-in figures of the inductor currents before and after the step change. Again, the average values remain equal. These results demonstrate that during both step changes, the two-phase currents stay balanced even under significant parameter mismatch.

Fig. 24 illustrates the experiment waveforms that the system output voltage steps from 10 V to 12 V. The output voltage v_o shifts from 9.98V up to 11.96V. Both inductor currents i_{L1} and i_{L2} exhibit second-order oscillatory behavior and maintain close tracking all the time. The instantaneous current difference $\Delta i = i_{L1} - i_{L2}$ remains within ±0.2A during the entire transition, and this difference converges to 0 A in 5.6ms. These results validate that the pseudo-DC-Link structure can effectively enforce precise current sharing under step changes without the assistance of any active current sensing or compensation circuitry.

VI. Conclusion

In this paper, an autonomous current balancing method for interleaved DC/DC converter based WPT system is proposed. By substituting the conventional DC bus capacitor with a pseudo-DC-Link capacitors structure, the proposed approach achieves autonomous current balancing without additional sensors. Theoretical analysis demonstrates that the principle enabling autonomous current balancing is valid. Specifically, it worths mentioning that the proposed approach can be generally applied to any WPT system that uses interleaved DC/DC converters. Based on the system's small-signal model, a control strategy is devised to ensure rapid disturbance response and high robustness. The experiment results validate that the proposed method allows interleaved DC/DC converter-based WPT systems to achieve high current output capability while avoiding current imbalances caused by parameter asymmetries. Furthermore, no extra sensors are required to be added, significantly reducing system costs and offering great potential

for practical applications.

APPENDIX I
GUIDANCE ON HOW TO SELECT PSEUDO-DC-LINK CAPACITOR

The selection of the capacitance value is a trade-off between the steady-state performance and the dynamic performance of the system. To provide clear guidance on selecting the pseudo-DC-Link capacitance, we derive upper and lower bounds from classical power-electronics theory:

1. Minimum capacitance (ripple constraint): Due to the system stability requirements, the ripple coefficient of the bus capacitor is less than 3% [37], i.e.

$$\frac{\Delta v_{DC1}}{\bar{v}_{DC1}} = 3\% \rightarrow C_{DC} \geq \frac{T_S \times \int_0^{0.5} i_{Ls} - i_{L1} dt}{0.03 \times \frac{I_{LS} r_{L1} + 2 I_{LS} R_O}{\pi D^2}} \approx 3.5\mu\text{F} \quad (25)$$

2. Dynamic performance: From the dynamic perspective, the value of pseudo-DC-Link capacitors also affects small-signal behaviors. In order to better understand the effect of C_{DC} variation, the Bode plots are depicted in Fig. 25 for different C_{DC}. As C_{DC} increases from 5μF to 200μF, the system requires a lower crossover frequency to maintain the same phase margin, resulting in slower response times with larger bus capacitance. To ensure that the system has a bandwidth with 115Hz, the pseudo-DC-Link capacitor value is selected to be 10μF.

APPENDIX II
DERIVATION OF THE DYNAMIC EXPRESSION OF THE BALANCING PROCESS

The dynamic behavior of the balancing process under parameter mismatch conditions no longer conforms to a second-order form. By using the state-space formulation derived in *Section II*, the system state vector is defined as

$$x = [v_{DC1}, v_{DC2}, i_{L1}, i_{L2}, v_o]^T \quad (26)$$

When the system parameters are mismatched, the state matrix A is expressed as

$$A = \begin{bmatrix} 0 & 0 & -\frac{D}{C_{DC1}} & 0 & 0 \\ 0 & 0 & 0 & -\frac{D}{C_{DC2}} & 0 \\ \frac{D}{L_1} & 0 & -\frac{r_L}{L_1} & 0 & -\frac{1}{L_1} \\ 0 & \frac{D}{L_2} & 0 & -\frac{r_L}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_o} & \frac{1}{C_o} & -\frac{1}{R_o C_o} \end{bmatrix} \quad (27)$$

The zero-input dynamic response of the system variables during the balancing process is governed by

$$\dot{x} = Ax + x(0) \quad (28)$$

where $x(0)$ represents the initial voltage and current of the system. The Laplace-domain representation is

$$x(s) = (s - A)^{-1} \times x(0) \quad (29)$$

By substituting the system parameters into the matrix A, the explicit expression of the balancing process can be obtained as

$$\Delta i_L(s) = i_{L1}(s) - i_{L2}(s)$$
$$= [(C_{CD1}C_{CD2}C_O I_{L1}(0)L_1L_2R_o - C_{CD1}C_{CD2}C_O I_{L2}(0)L_1L_2R_o)$$
$$s^4 + (C_{CD1}C_{CD2}I_{L1}(0)L_1L_2 - C_{CD1}C_{CD2}I_{L2}(0)L_1L_2 + C_{DC1}C_{DC2}$$
$$C_O L_1 R_o v_o(0) - C_{CD1}C_{CD2}C_O L_2 R_o v_o(0) + C_{CD1}C_{CD2}C_O I_{L1}(0)$$
$$L_1 R_o r_L - C_{CD1}C_{CD2}C_O I_{L2}(0)L_2 R_o r_L + C_{CD1}C_{CD2}C_O L_1 v_{DC2}(0)$$
$$R_o D + C_{CD1}C_{CD2}C_O L_2 v_{DC1}(0)R_o D)\, s^3 + (C_{CD1}C_{CD2}v_{DC1}(0)D$$
$$L_2 - C_{CD1}C_{CD2}v_{DC2}(0)DL_1 + 2C_{CD1}C_{CD2}I_{L1}(0)L_1R_o - 2C_{CD1}$$
$$C_{CD2}I_{L2}(0)L_2R_o + C_{CD1}C_{CD2}I_{L1}(0)L_1r_L - C_{CD1}C_{CD2}I_{L2}(0)L_2r_L$$
$$+C_{CD1}C_oI_{L1}(0)L_1R_oD^2 - C_{CD2}C_oI_{L2}(0)L_2R_oD^2 + C_{CD1}C_{CD2}$$
$$C_oR_ov_{DC1}(0)r_LD - C_{CD1}C_{CD2}C_oR_ov_{DC2}(0)r_LD)s^2 + (C_{CD1}L_1$$
$$I_{L1}(0)D^2 - C_{CD2}L_2I_{L2}(0)D^2 + 2C_{CD1}C_{CD2}R_Ov_{DC1}(0)D - 2$$
$$C_{CD1}C_{CD2}R_Ov_{DC2}(0)D + C_{CD1}C_{CD2}r_Lv_{DC1}(0)D - C_{CD1}C_{CD2}r_L$$
$$v_{DC2}(0)D + C_{CD1}C_oR_ov_{DC1}(0)D^3 - C_{CD2}C_oR_ov_{DC2}(0)D^3 -$$
$$C_{CD1}C_oR_ov_o(0)D^2 + C_{CD2}C_oR_ov_o(0)D^2)s + (C_{CD1}v_{CD1}(0)D^3$$
$$-C_{CD2}v_{CD2}(0)D^3)]/[(C_{CD1}C_{CD2}L_1L_2C_OR_o)s^5 + (C_{CD1}C_{CD2}L_1$$
$$L_2 + C_{CD1}C_{CD2}C_OL_1R_or_L + C_{CD1}C_{CD2}C_OL_2R_or_L)s^4 + (C_{CD1}$$
$$C_{CD2}L_1R_o + C_{CD1}C_{CD2}L_2R_o + C_{CD1}C_{CD2}L_1r_L + C_{CD1}C_{CD2}L_2r_L$$
$$+C_{CD1}C_{CD2}C_oR_or_L^2 + C_{CD1}C_oL_1R_oD^2 + C_{CD2}C_oL_2R_oD^2)s^3$$
$$+(C_{CD1}L_1D^2 + C_{CD2}L_2D^2 + C_{CD1}C_{CD2}r_L^2 + 2C_{CD1}C_{CD2}R_or_L$$
$$+C_{CD1}C_oR_or_LD^2 + C_{CD2}C_oR_or_LD^2)s^2 + (C_{CD1}R_oD^2 + C_{CD2}$$
$$R_oD^2 + C_oR_oD^4 + C_{CD1}r_LD^2 + C_{CD2}r_LD^2)s + D^4]. \quad (30)$$

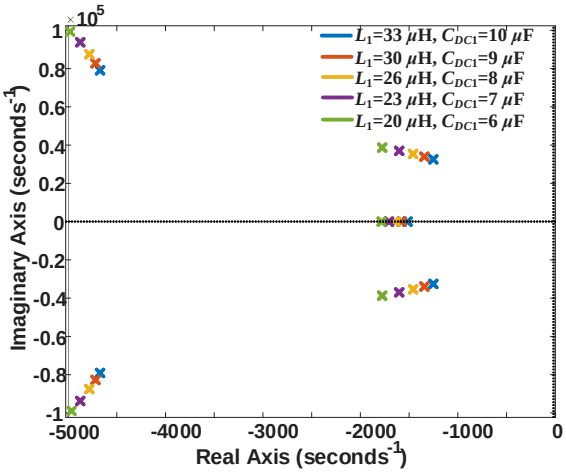

Fig. 26. Poles plots of the balancing process transfer function as L_1 and C_1 changes.

Fig. 26 shows the pole locations of the fifth-order balancing dynamics $\Delta i_L(s)$ as L_1 and C_{DC1} changes. As L_1 and C_{DC1} decrease, the poles shift marginally left. All poles remain in the open left-half plane for every case, confirming asymptotic stability of balancing transfer function.

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Zixuan Xu received the B. S. degrees in electrical engineering from Harbin Institute of Technology, Shenzhen, China, in 2022. He is currently working toward the Ph.D degree in electrical and electronic engineering with Hong Kong Polytechnic University, Hong Kong, SAR, China.
His current research interests include topology, modeling, and control of power electronics converters.

Menglin L.N.Chen(Senior Member, IEEE)received the B.S.degree from the Huazhong University of Science and Technology, Wuhan,China, the B.Eng.degree from the University of Birmingham, Birmingham, U.K., both in 2012, and the M.S. and Ph.D. degrees from The University of Hong Kong, Hong Kong, in 2013 and 2018, respectively.

From May 2017 to October 2017. She was an Academic Visitor with the School of Electronic Engineering and Computer Science, QueenMary University of London, London, U.K. From 2018 to 2022, she was a Post-Doctoral Fellow at The University of Hong Kong. She is curently a Research Assistant Professor with the Department of Electrical and Electronic Engineering, The Hong Kong Polytechnic University, Hong Kong. Her research interests include advanced electromagnetics-based interdisciplinary research, including novel metamaterial/metasurface design, microwave photonics, topological photonic crystals, and their applications in microwave/millimeter-wave engineering.

Kerui Li (Member, IEEE) received the B.Eng. degree from the South China University of Technology in 2013, the M.Eng. degree from the Sun Yat-sen University in 2016, and the Ph.D. degree from The University of Hong Kong in 2021. Since 2025, he has been with the City University of Hong Kong, where he is currently an Assistant Professor in the Department of Electrical Engineering. Prior to that, he served as a Research Fellow at Nanyang Technological

University and as a Research Assistant Professor at both The Hong Kong Polytechnic University and the University of Hong Kong.
Dr. Li's professional services and research have been recognized with several prestigious awards, including the IEEE Transactions on Power Electronics Outstanding Reviewer Award (2025), two IEEE Transactions on Power Electronics Prize Paper Awards (second place in 2024 and first place in 2023), the IEEE Power Electronics Society Ph.D. Thesis Talk Award (2022), and the University of Hong Kong Power Engineering Prize (2020).

Minghao Wang (Senior Member, IEEE) received the B.Eng. (Hons.) degree in electrical and electronic engin eering from the Huazhong University of Science and Technology, Wuhan, China, and the University of Birmingham, Birmingham, U.K. in 2012, and the M.Sc. and the Ph.D. degree, both in electrical and electronic engineering, from The University of Hong Kong, Hong Kong, in 2013 and 2017, respectively. Currently, he is a Research Assistant Professor in the Department of Electrical Engineering, the Hong Kong Polytechnic University. His search interests include power systems and power electronics.

Xinyang Su received the B. S. and M. S. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2020 and 2023. He is currently working toward the Ph.D degree in electrical and electronic engineering with Hong Kong Polytechnic University, Hong Kong, SAR, China.

His current research interests include modeling and control of power electronic converters, and stability analysis of DC and AC power systems.

Zhao Xu (Senior Member, IEEE) received the B.Eng. degree from Zhejiang University in 1996, the M.Eng. degree from the National University of Singapore in 2002, and the Ph.D. degree from The University of Queensland in 2006.
He is currently a Professor with the Department of Electrical and Electronic Engineering and Shenzhen Research Institute, the Hong Kong Polytechnic University. He is also a Foreign Associate Staff with the Centre for Electric Technology, Technical University of Denmark. His research interests include demand side, grid integration of wind and solar power, and AI applications. He is the Chairman of IEEE PES/IES/PELS/IAS Joint Chapter in Hong Kong Section. He has served/is serving as an Editor for a number of IEEE TRANSACTIONS and IET journals.