Model-Guided Modulation for AC-DC DAB Converter Considering AC-Side Capacitor Voltage Ripple

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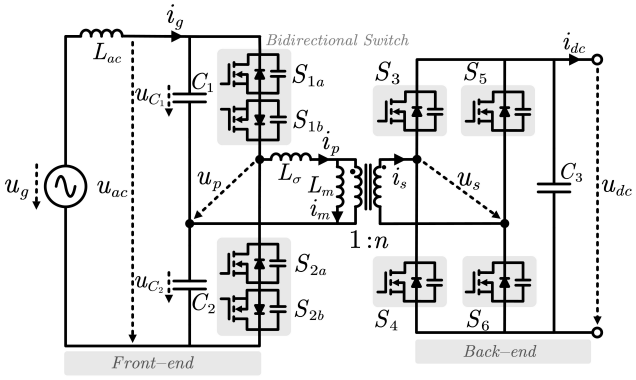
***Abstract*—The matrix-type ac-dc dual-active-bridge (DAB) converter is a promising topology for single-stage ac-dc power conversion, recognized for its high power density, reliability, and efficiency. This converter uses small capacitance for the ac-side filter, typically in the range of a few microfarads or a dozen microfarads, to achieve a high power-factor (PF) and optimize both power density and cost. However, the relatively small ac-side capacitance can cause noticeable capacitor voltage ripple during the switching cycle. This article presents a time-domain steady-state model to accurately characterize the steady-state behavior of the converter. The analysis reveals that the ac-side capacitor voltage ripple can substantially impact the performance of the converter, particularly by causing the front-end cycloconverter to lose zero voltage switching (ZVS), thereby reducing efficiency and worsening electromagnetic interference (EMI) issues. The steady-state model is then used in an optimized modulation strategy to determine the optimal control variables to ensure ZVS operation, realize power factor correction (PFC), and enhance efficiency. Simulation and experimental results demonstrate the theoretical analysis and validate the findings. Specifically, using the proposed modulation method, compared to the modulation method that does not account for the ac-side capacitor voltage ripple, the efficiency at light-load and heavy-load conditions can be improved by over 11.21% and 2.66%, respectively.**

***Index Terms*—Single-stage ac-dc converter, dual-active-bridge (DAB), steady-state model, capacitor voltage ripple, efficiency-optimized modulation.**

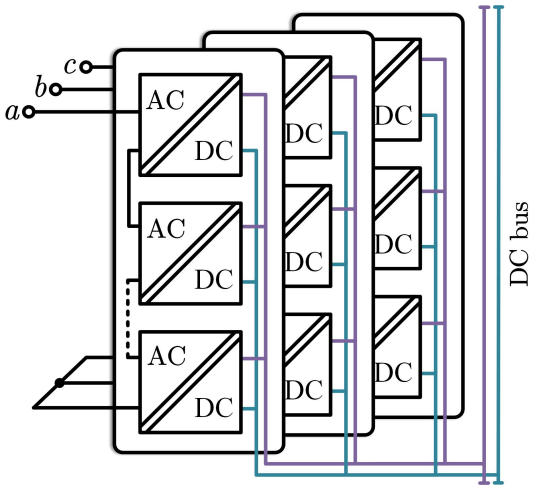
I. Introduction

The isolated single-phase ac-dc converters are widely utilized in modern power conversion systems, including electric vehicle charging systems, photovoltaic (PV) systems, and battery energy storage systems [1]–[6]. Based on the number of energy conversion stages, these converters can be categorized into single-stage and two-stage configurations. Typically, two-stage solutions consist of a front-stage power factor correction (PFC) unit and a back-stage isolated dc-dc converter, often linked by an electrolytic capacitor. Compared to two-stage schemes, single-stage ac-dc converters offer advantages in efficiency, reliability, power density, and cost [1].

Among the various types of isolated single-stage ac-dc converters, the matrix-type dual-active-bridge (DAB) converters have recently attracted extensive attention [7]–[15]. The circuit configuration of the matrix-type DAB converter discussed in this article is shown in Fig. 1 (a). This converter is named according to its front-end structure, which features a matrix configuration with bidirectional switches. It can also be referred to as a cycloconverter-type DAB converter because



(a)



(b)

Fig. 1. Circuit configurations of the single-stage ac-dc DAB converter and solid-state transformer (SST). (a) DAB converter. (b) SST.

the front-end circuit directly chops the fundamental-frequency grid voltage into switching-frequency ac pulse voltage. Unlike the approach in [7] and [8], which uses a full-bridge structure at the front end, employing a half-bridge configuration at the front end requires fewer switching devices. This reduces the cost of the converter and the complexity of the control algorithms, while maintaining a simpler structure. To interface with medium voltage level grids and achieve high-power electric energy conversion, multiple submodules based on the matrix-type ac-dc DAB converter can be connected in an input-

series and output-parallel configuration, as shown in Fig. 1 (b), to develop a solid-state transformer (SST) [9].

Comprehensive analyses and design methodologies for this single-stage ac-dc DAB converter have been thoroughly explored in existing literature. Reference [10] initially proposed a combined phase-shift and frequency modulation method, where optimal phase-shift angles and switching frequencies are obtained through offline optimization algorithms. Reference [11] introduced an analytical modulation method aimed at achieving zero-voltage-switching (ZVS) operation and minimizing the peak current of the transformer. A simplified modulation method using a single modulation mode is further presented in [12] to streamline the design and control of the converter. The cause of grid current distortion is explained in [13], along with its closed-loop control strategy. References [14] and [15] provide comprehensive analyses of the operating modes and multi-objective design principles of the converter.

Although the research presented in the existing literature has well covered the modulation, design, and modeling of the converter, one critical issue has not been addressed. As shown in Fig. 1 (a), the ac-side inductor L_{ac} and capacitors C_1 and C_2 form a filter to suppress the switching-frequency harmonic current injected into the grid. Besides forming the filter, C_1 and C_2 also support the ac-side input voltage (u_{ac}) of the converter. Existing studies generally rely on a simplified steady-state model that assumes the ac-side capacitor voltages, u_{C_1} and u_{C_2}, remain constant during each switching cycle. This assumption underpins the modeling, modulation, and design of the converter. However, this assumption can be invalid because the ac-side capacitance of the converter is relatively small, usually in the range of a few microfarads or a dozen microfarads, to reduce reactive power introduced by the capacitors [9]–[15] and to optimize the power density and cost of the converter. The capacitor voltage ripple can be more noticeable when the switching frequency is not far from the resonant frequency of the $L_\sigma C_1$ and $L_\sigma C_2$ circuits [10] (where L_σ is the equivalent inductance formed by the leakage inductance of the transformer and an auxiliary inductance). Consequently, the voltage ripple across the ac-side capacitors requires attention.

To investigate the impact of the ac-side capacitor voltage ripple on the converter, this article proposes a time-domain steady-state model. Analysis based on this model reveals that the capacitor voltage ripple can significantly affect the performance of the converter, an issue that has not been previously addressed in the literature. It is found that ZVS on the front-end circuit can fail if the modulation strategy is designed based on a simplified steady-state model that ignores the effects of the capacitor voltage ripple within one switching cycle. Losing ZVS operation can worse electromagnetic interference (EMI) issues and reduce the efficiency of the converter. The capacitor voltage ripple can also influence the characteristics of the transmission power and the root mean square (RMS) values of the transformer primary and secondary currents, thereby further affecting the overall efficiency of the converter.

Following the analysis of ac-side capacitor voltage ripple, this article further proposes an optimized modulation method to mitigate its negative effects. This approach begins by establishing a power loss model of the converter. Then, using the proposed steady-state model and a genetic algorithm (GA), the optimal control variables are determined to achieve unity power-factor (PF), ensure ZVS in the front-end circuit, and optimize the power conversion efficiency of the converter. Experimental results show that, compared to an existing modulation method that does not consider capacitor voltage ripple, the proposed method improves the efficiency of the converter by over 11.21% under light-load conditions and 2.66% under heavy-load conditions.

The rest of this article is organized as follows. Section II explains the circuit configuration and operating principle of the converter. Section III compares the simplified steady-state model and the proposed steady-state model, without and with considering the ac-side capacitor voltage ripple. The effect of the capacitor voltage ripple on the performance of the converter is revealed in Section IV. Section V presents the implementation of the optimized modulation method, and Section VI shows the experimental results that validate the theoretical analysis and findings. Finally, Section VII concludes this article.

II. Circuit Configuration and Operating Principle

A. Circuit Configuration

Fig. 1 (a) illustrates the circuit configuration of the single-stage ac-dc DAB converter. A cycloconverter with bidirectional switches is employed at the front end, while a full-bridge circuit is used at the back end. u_g and i_g represent the grid voltage and current, respectively, whereas u_{dc} and i_{dc} denote the dc-side voltage and current. Components L_{ac}, C_1, and C_2 function as a filter to suppress the switched currents injected into the grid, as mentioned above. C_3 is used for holding constant dc bus voltage and also provides a low impedance path for the high-frequency harmonic currents.

The isolation transformer establishes a power transmission channel, linking the cycloconverter and full bridge circuit with a turn ratio of $1 : n$. L_m is the magnetizing inductance. The primary and secondary voltages of the transformer are denoted as u_p and u_s, respectively. Similarly, the primary and secondary currents are represented by i_p and i_s, respectively.

B. Operating Principle

Fig. 2 illustrates the operating waveforms of the converter during one switching cycle, with all switching signals set to a 50% duty ratio. (S_{1a}, S_{2a}), (S_{1b}, S_{2b}), (S_3, S_4) and (S_5, S_6) are four pairs of complementary switches. Therefore, only the waveforms of S_{1a}, S_{1b}, S_3 and S_5 are shown in Fig. 2. The deadtime $T_i = d_i T_s$ is introduced to prevent short circuit in a half-bridge circuit.

During one half-cycle of the grid voltage, only two switches at the front end operate at high frequency. When u_g is positive, S_{1a} and S_{2a} switch at high frequency, while S_{1b} and S_{2b} remain ON. Conversely, when u_g is negative, S_{1b} and S_{2b} switch at high frequency, whereas S_{1a} and S_{2a} remain ON.

Two control variables, D_1 and D_2, are defined as the ratios of the switching cycle T_s. $D_1 T_s$ indicates the length of the back-end clamping interval, while $D_2 T_s$ represents the phase

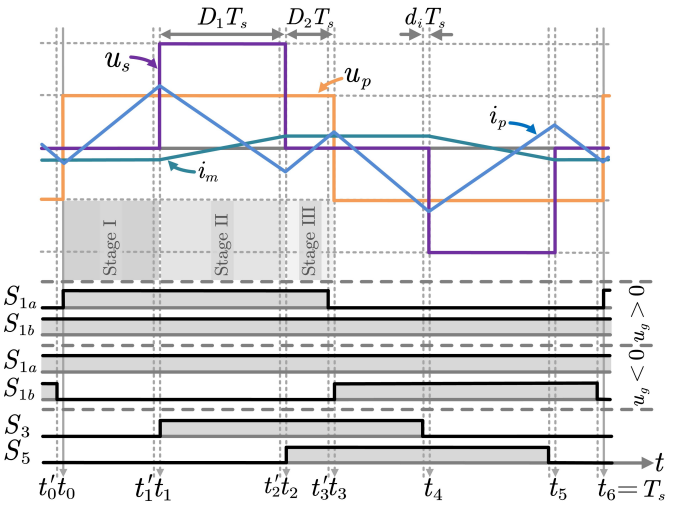


Fig. 2. Operating waveforms of the converter.

shift between the falling edges of u_p and u_s. Actually, four modulation modes can be derived based on different sequences of the rising and falling edges of u_p and u_s [14]. However, only the modulation mode shown in Fig. 2 is used in this article, as it results in smaller peak and RMS values of the transformer current [14]. Moreover, the converter design can be simplified by utilizing only one modulation mode [12]. This article aims to reveal the impact of the ac-side capacitor voltage ripple on converter performance and propose an optimized modulation strategy to enhance efficiency. While this article discusses only one modulation mode, the steady-state analysis model and optimized modulation idea proposed in the subsequent sections can be readily extended to other modulation modes, which are not detailed in this article. Additionally, although the converter is capable of bidirectional power transfer, this article focuses solely on the ac-to-dc operation. All the analysis presented in this article is applicable to dc-to-ac operation as well.

For the converter, when S_{1a} and S_{1b} are turned on, the primary side of the transformer with L_σ connects to C_1, resulting in u_p equaling u_{C_1}. Conversely, when S_{2a} and S_{2b} are turned on, the primary side of the transformer with L_σ connects to C_2, causing u_p to equal u_{C_2}. In Fig. 2, u_p is depicted as square-wave without ripples, based on the assumption that the ac-side capacitor voltages remain constant within one switching cycle. This assumption is valid for the dc-side voltage supported by a large capacitance. However, this assumption can be invalid for the ac-side due to the relatively small capacitance value. As analyzed in the next two sections, the ac-side capacitors actually exhibit noticeable voltage ripple, which can impact the performance of the converter.

III. Steady-State Modeling

In this section, a time-domain analysis model that accounts for the ac-side capacitor voltage ripple is developed to analyze the steady-state characteristics of the ac-dc DAB converter. Comparisons are then made between the proposed model and the model used in references [9]–[15]. The results demonstrate that the proposed model can accurately depict the steady-state performance of the converter. In contrast, the model used in the existing literature, which does not consider the ac-side capacitor voltage ripple, loses accuracy. Section IV will further explain the impact of the ac-side capacitor voltage ripple on converter operation, based on the steady-state models presented in this section.

A. Simplified Model

The waveforms illustrated in Fig. 2 can be divided into two half cycles: t_0 to t_3 and t_3 to t_6. The first half cycle, from t_0 to t_3, is further subdivided into three modulation stages, labeled I to III, according to the changes of the switching states. Due to the symmetry of the modulation method, analyzing the first half-cycle is enough to determine the waveforms for the second half-cycle. Therefore, the following analysis provides only the voltage and current expressions for the first half-cycle.

The existing references [9]–[15] assume that the ac-side capacitor voltage remains constant throughout one switching cycle. With this assumption, u_p exhibits a two-level voltage pattern, and the transformer primary current forms a straight line in each modulation stage, as shown in Fig. 2. The values of the transformer primary current at time instants t_0, t_1, t_2, and t_3 are given by

$$\begin{cases} i_p(t_0) = \dfrac{1}{8nf_sL_\sigma}(4u_{dc}D_1 - n|u_{ac}|) \\ i_p(t_1) = \dfrac{u_{dc}D_1}{2nf_sL_\sigma} + \dfrac{|u_{ac}|}{2f_sL_\sigma}(\dfrac{1}{4} - D_1 - D_2) \\ i_p(t_2) = -\dfrac{u_{dc}D_1}{2nf_sL_\sigma} + \dfrac{|u_{ac}|}{2f_sL_\sigma}(\dfrac{1}{4} - D_2) \\ i_p(t_3) = -\dfrac{1}{8nf_sL_\sigma}(4u_{dc}D_1 - n|u_{ac}|) \end{cases} \tag{1}$$

where u_{ac} and u_{dc} are assumed to be constant values within one switching cycle. u_{ac} approximates the grid voltage u_g.

The average transmission power of the converter during one switching cycle can be calculated using equation (2) [12], assuming power losses are negligible.

$$P = \int_{t_0}^{t_6} \frac{u_p(t)i_p(t)}{T_s}dt = \frac{|u_{ac}|\,u_{dc}D_1(1 - 2D_1 - 4D_2)}{4nf_sL_\sigma} \tag{2}$$

B. Proposed Model Considering the Capacitor Voltage Ripple

To accurately analyze the steady-state performance of the converter, this subsection proposes a steady-state model that accounts for the ac-side capacitor voltage ripple. Before developing the time-domain steady-state model, several assumptions are made:

1) C_1 and C_2 have the same capacitance and are both denoted as C.
2) The parasitic parameters of the converter and voltage drops of the switches are ignored, and the power losses in the converter are also neglected.
3) The switching dynamics are not considered.
4) The ripple components of the grid current are neglected in the dynamics of the capacitors, assuming the grid current remains constant within one switching cycle.

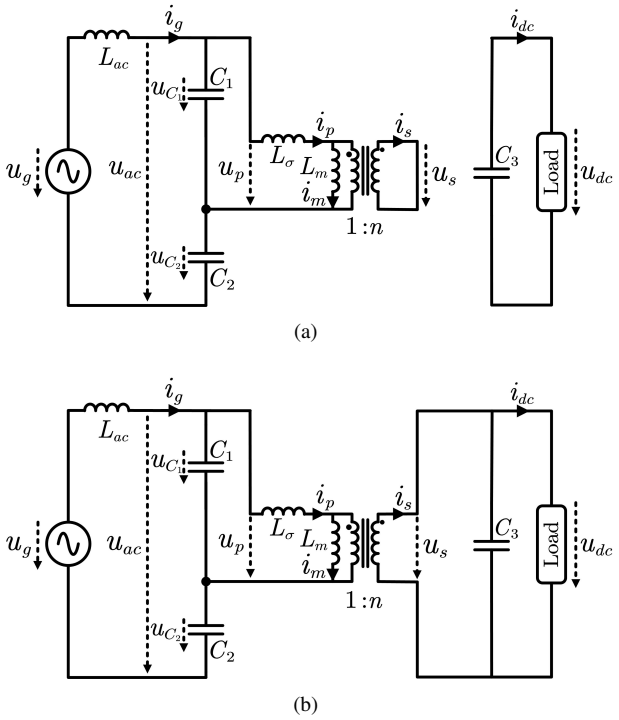


Fig. 3. Equivalent circuit of the converter in modulation stages I–III. (a) The equivalent circuit in stages I and III. (b) The equivalent circuit in stage II.

Consequently, the grid current is denoted as i_g instead of $i_g(t)$ in the following equations. Similarly, the grid voltage and dc-side voltage are denoted as u_g and u_{dc}, respectively, rather than $u_g\,(t)$ and $u_{dc}\,(t)$.

The equivalent circuits of the converter for each modulation stage are illustrated in Fig. 3. The equivalent circuit in modulation stages I and III is shown in Fig. 3 (a), while that for stage II is shown in Fig. 3 (b). The dynamic equations of the capacitors C_1 and C_2 remain unchanged during the first half cycle, and they are expressed as

$$C\frac{du_{C_1}(t)}{dt} = i_g - i_p(t) \tag{3}$$

$$C\frac{du_{C_2}(t)}{dt} = i_g \tag{4}$$

The dynamic equations of the transformer primary current depicted in Fig. 3 (a) and Fig. 3 (b) are respectively given by

$$L_\sigma\frac{di_p(t)}{dt} = u_{C_1}(t) \tag{5}$$

$$L_\sigma\frac{di_p(t)}{dt} = u_{C_1}(t) - \frac{u_{dc}}{n} \tag{6}$$

According to (3), (5) and (6), the expressions of $i_p(t)$ and $u_{C_1}(t)$ during modulation stages I III can be calculated as shown in (A1) and (A2) in the Appendix.

D_1 and D_2 are the two control variables for the modulation mode illustrated in Fig. 2. The objective here is to obtain the current and voltage waveforms of the converter based on given converter parameters and control variables D_1 and D_2. The first step involves calculating eight unknown variables in (A1) and (A2): $i_p\,(t_0)$, $i_p\,(t_1)$, $i_p\,(t_2)$, $i_p\,(t_3)$, $u_{C_1}\,(t_0)$, $u_{C_1}\,(t_1)$, $u_{C_1}\,(t_2)$ and $u_{C_1}\,(t_3)$. These values are essential not only because they allow for the calculation of $i_p(t)$ and $u_{C_1}(t)$ once D_1 and D_2 are specified, but also because they are crucial for evaluating the power losses of the converter.

To determine the eight unknown variables, two additional equations are needed, which are given as

$$i_p(t_0) = -i_p(t_3) \tag{7}$$

$$\int_{t_0}^{t_3} u_{ac}(t) = \int_{t_0}^{t_3} [u_{C_1}(t) + u_{C_2}(t)]dt = \frac{u_g T_s}{2} \tag{8}$$

Equation (7) indicates the modulation symmetry and the voltage-second balance of the inductor L_σ. Equation (8) implies that the average value of u_{ac} over half a switching cycle equals the grid voltage. According to (4), the expression of the capacitor voltage u_{C_2} can be given by

$$u_{C_2}(t) = \frac{i_g \triangle t}{C} + u_{C_2}(t_0) \tag{9}$$

where $\triangle t = t - t_0$.

According to the equivalent circuits shown in Fig. 3, the grid current i_g directly flows through capacitor C_2 in the first half cycle. Actually, it will directly flow through capacitor C_1 in the second half cycle, according to the modulation mode illustrated in Fig. 2. Essentially, capacitors C_1 and C_2 just exchange their waveforms in the two half switching cycles. Consequently, the following equations hold.

$$\begin{cases} u_{C_1}(t_0) = u_{C_2}(t_3) \\ u_{C_1}(t_3) = u_{C_2}(t_0) \end{cases} \tag{10}$$

Substituting (5), (6), (9) and (10) into (8) yields

$$L_\sigma[i_p(t_3) - i_p(t_0)] + \frac{u_{dc}}{n}(t_2 - t_1) + \frac{T_s u_{C_1}(t_3)}{2} + \frac{T_s^2 i_g}{8C} = \frac{T_s u_g}{2} \tag{11}$$

So far, eight equations have been derived: (7), (11), and the six equations obtained by substituting $t = t_0$, t_1, and t_2 into (A1) and (A2). These can be used to form an equation set to calculate the eight unknown variables mentioned above. For specific values of D_1 and D_2, the time instants t_0, t_1, t_2 and t_3 in the equation set can be easily determined, namely: $t_1 = t_0 + (0.5 - D_1 - D_2)T_s$, $t_2 = t_0 + (0.5 - D_2)T_s$, and $t_3 = t_0 + 0.5T_s$. However, the grid current i_g remains an unknown variable. Therefore, one more step further, i_g can be calculated as

$$i_g = \frac{P}{u_g} = \frac{2}{T_s u_g}\int_{t_0}^{t_3} \frac{u_{dc}(t) i_p(t)}{n} dt \tag{12}$$

where P is the average transmission power of the converter in one switching cycle. Substituting (A1), (A3) and (A4) into (12) yields (A5) as given in the Appendix. By substituting (A5) into (11), (A1) and (A2), a final matrix equation is obtained as shown in (A10). Finally, the eight unknown variables $i_p\,(t_0)$, $i_p\,(t_1)$, $i_p\,(t_2)$, $i_p\,(t_3)$, $u_{C_1}\,(t_0)$, $u_{C_1}\,(t_1)$, $u_{C_1}\,(t_2)$, and $u_{C_1}\,(t_3)$ can be calculated according to (A10) for given converter parameters and control variables D_1 and D_2. By substituting these current and voltage values into (A1) and (A2), the steady-state waveforms of $i_p(t)$ and $u_{C_1}(t)$ can be obtained.

TABLE I
PARAMETERS OF THE AC-DC DAB CONVERTER

Symbol	Description	Value
U_{grms}	RMS value of the grid voltage	110 V
f_0	Grid voltage frequency	50 Hz
T_0	Grid voltage cycle	20 ms
u_{dc}	DC-side voltage	200 V
P_{rtd}	Rated active power	500 W
n	Transformer trun ratio	2
L_σ	Commutation inductor	14.1 μH
L_m	Transformer magnetizing inductance	700 μH
L_{ac}	AC-side inductor	200 μH
C_1, C_2	AC-side capacitors	8 μF
C_3	DC-side capacitor	3740 μF
f_s	Switching frequency	20 kHz
T_i	Deadtime	200 ns

To perform a complete steady-state waveform analysis, it is needed to obtain the expressions of the transformer secondary current and the magnetizing current. The transformer secondary current during the first half cycle is written as

$$i_s(t) = \frac{1}{n}[i_p(t) - i_m(t)] \tag{13}$$

The magnetizing current remains unchanged during modulation stages I and III, and it increases in stage II with the dynamic equation given by

$$L_m \frac{di_m(t)}{dt} = \frac{u_{dc}}{n} \tag{14}$$

Accordingly, the expression of the magnetizing current in each modulation stage can be obtained as

$$i_m(t) = \begin{cases} -\dfrac{u_{dc}D_1T_s}{2nL_m} & t_0 \le t \le t_1 \\ -\dfrac{u_{dc}D_1T_s}{2nL_m} + \dfrac{u_{dc}(t-t_1)}{nL_m} & t_1 < t \le t_2 \\ \dfrac{u_{dc}D_1T_s}{2nL_m} & t_2 < t \le t_3 \end{cases} \tag{15}$$

The waveform of the secondary current can be readily derived according to (13), (15) and (A1). At this point, the waveforms of all converter state variables can be obtained according to the time-domain steady-state analysis model presented above.

C. Model Comparisons

The parameters of the converter, as listed in Table I, are utilized to compare the steady-state models. The capacitance C is designed to limit the introduced capacitive reactive power to approximately 5% of the rated active power [16].

Fig. 4 and Fig. 5 illustrate the waveforms obtained from both the simulation results and the theoretical analysis based on the two steady-state models discussed in subsections III. A and III. B. The steady-state waveforms during one switching cycle are presented, with solid gray lines representing the simulation results and dotted lines representing the theoretical analysis results. The control variables D_1 and D_2 are equal to 0.376 and 0.014, respectively. The grid voltage within this switching cycle is 155 V. As shown in Fig. 4, the theoretical analysis results derived from the proposed steady-state model match well with the simulation waveforms. In contrast, the simplified model presented in [9]–[15], which neglects the ac-side capacitor voltage ripples, is unable to accurately reflect the steady-state performance of the converter, as shown in Fig. 5. i_s is magnified by 4 times in Fig. 4 for easier observation.

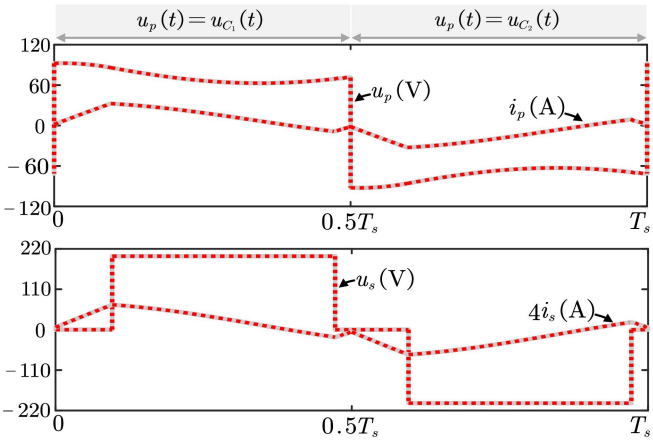


Fig. 4. Comparisons between the simulation results and theoretical analysis results using the proposed steady-state model.

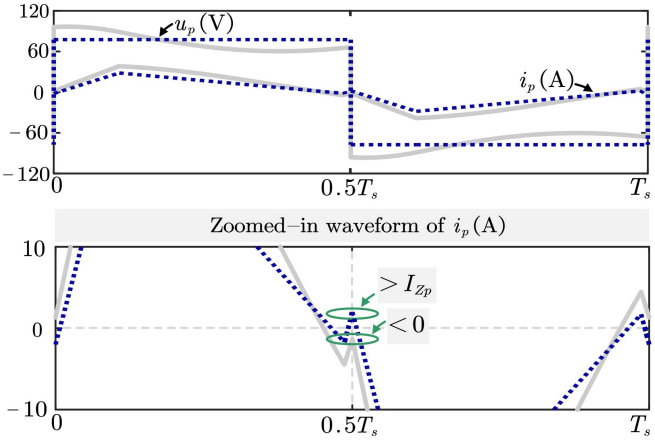


Fig. 5. Comparisons between the simulation results and theoretical analysis results using the simplified steady-state model.

The zoomed-in waveform of i_p shown in Fig. 5 indicates that the actual or simulated value of i_p is negative, whereas the value calculated by the simplified model is greater than a positive value I_{Zp} (I_{Zp} is the current value required for ZVS operation in the front-end circuit, which will be explained in the next section). This implies that if the simplified steady-state model is used to determine the control variables, ZVS will be lost. A more detailed explanation will be provided in the next section.

IV. EFFECTS OF THE CAPACITOR VOLTAGE RIPPLE

Firstly, the transmission power derived from (2) and the proposed steady-state model, based on the converter parameters listed in Table I, can be plotted for different values of D_1 and D_2, as illustrated in Fig. 6. The value of the grid voltage is 155 V for the analysis. It should be noted that for

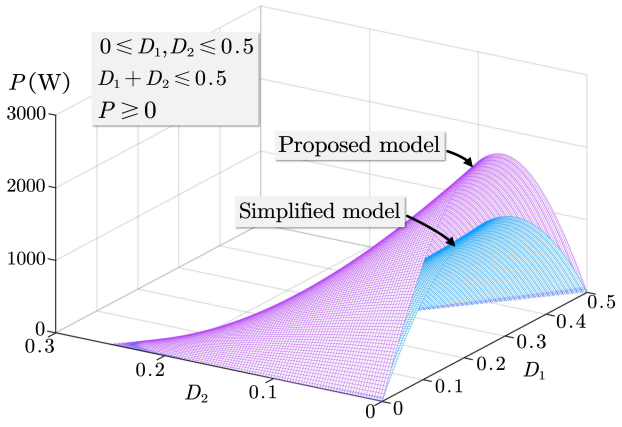


Fig. 6. Transmission power for different values of D_1 and D_2.

the modulation mode depicted in Fig. 2, D_1 and D_2 should satisfy the following constraints.

$$\begin{cases} 0 \leq D_1, D_2 \leq 0.5 \\ D_1 + D_2 \leq 0.5 \end{cases} \tag{16}$$

Fig. 6 reveals that the actual transmission power of the converter, when considering the ac-side capacitor voltage ripple, significantly deviates from the values obtained without accounting for this factor. This conclusion remains valid for various values of the grid voltage throughout the entire fundamental cycle.

Subsequently, to further explain the impact of ac-side capacitor voltage ripple on the ZVS of the converter, the modulation methods proposed in [11] and [12] are briefly introduced. With unity PF, the transmission power of the converter should track its reference, which is expressed as

$$P_{ref}(t) = u_g(t) i_{gref}(t) = U_g I_{gref} \sin^2(\omega_0 t) \tag{17}$$

where U_g is the amplitude of the grid voltage, I_{gref} is the amplitude of the grid current reference, and ω_0 is the fundamental angular frequency of the grid voltage.

To achieve ZVS in both the front-end cycloconverter and the back-end full-bridge circuit, the currents on the primary and secondary sides must meet the following constraints

$$i_p(t_3^{'}) > I_{Zp} = \frac{|u_{ac}|}{\sqrt{L_\sigma / C_{eqf}}} \approx \frac{|u_g|}{\sqrt{L_\sigma / C_{eqf}}} \tag{18}$$

$$i_s(t_1^{'}) > I_{Zs} = \frac{u_{dc}}{\sqrt{L_\sigma / C_{eqb}}} \tag{19}$$

$$i_s(t_2^{'}) < -I_{Zs} = -\frac{u_{dc}}{\sqrt{L_\sigma / C_{eqb}}} \tag{20}$$

where C_{eqf} and C_{eqb} represent the equivalent output capacitances of the MOSFETs in the front-end and back-end circuits, respectively. The currents at switching instants $t_1^{'}$, $t_2^{'}$, and $t_3^{'}$ can be determined by substituting these time values into (A1) ($t_r^{'} = t_r - d_i T_s$ and $r = 1, 2, 3$). The control variables are calculated according to (21) and (22) to meet the conditions specified in (18). By appropriately designing the parameters of the circuit, $i_s(t_1^{'})$ and $i_s(t_2^{'})$ can naturally satisfy (19) and (20), based on the control variables derived from (21) and (22)

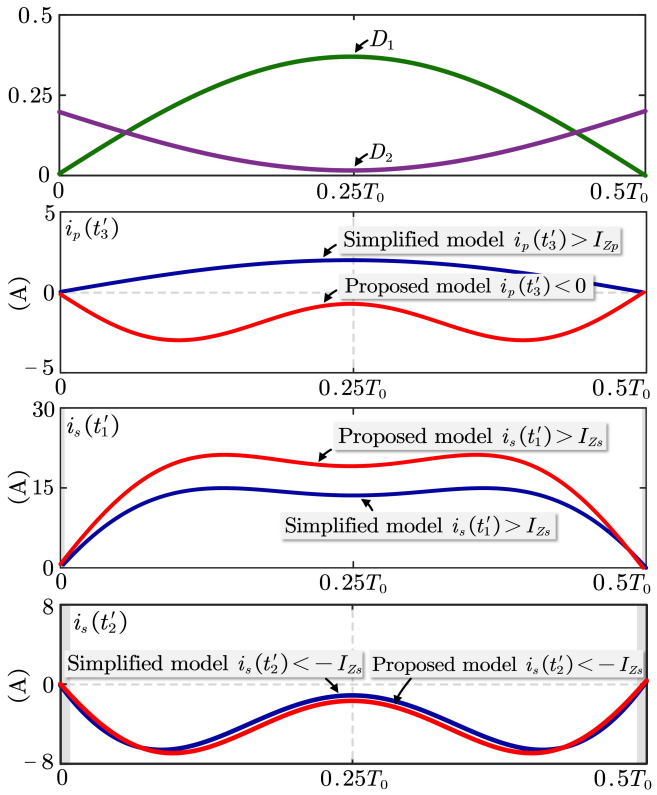


Fig. 7. Converter control variables and transformer primary/secondary currents over half a cycle of the grid voltage.

[12]. For detailed information on the modulation method, refer to [11] and [12].

$$D_1 = \frac{n|u_g|(1 - 4d_i) - 8nf_s L_\sigma I_{Zp}}{4u_{dc}} \tag{21}$$

$$D_2 = \frac{nP_{ref} f_s L_\sigma}{|u_g| u_{dc} D_1} + \frac{D_1}{2} - \frac{1}{4} \tag{22}$$

Using the circuit parameters listed in Table I as an example, Fig. 7 illustrates the control variables, as well as the transformer primary and secondary currents over half a cycle of the grid voltage. The reference of the active power is 500W. According to the simplified model, the primary current at $t_3^{'}$ satisfies the ZVS condition; however, the actual current value calculated by the proposed model does not meet this condition. This analysis indicates that employing the simplified model for designing the modulation strategy can result in the loss of ZVS in the front-end cycloconverter. Nevertheless, the back-end full-bridge circuit still adheres to the ZVS constraints specified in (19) and (20), as shown in Fig. 7, except for the light-load range in the gray area, due to the insufficient magnitude of the primary and secondary currents [12]. The loss of ZVS in the gray interval leads to negligible switching losses because of the low transmission power.

V. Optimized Modulation Method Considering the Capacitor Voltage Ripple

As analyzed above, the steady-state performance of the converter can be affected by the ac-side capacitor voltage ripple.

TABLE II
POWER LOSS MODEL OF THE AC-DC DAB CONVERTER

Loss	Classification	Expression
Power switch	Conduction losses	$R_{DSon}I^2_{Drms}$
losses	Switching losses	$(E_{onM}+E_{offM})f_s$
Transformer	Copper losses	$I^2_{prms}R_{pri}+I^2_{srms}R_{sec}$
losses	Core losses	$k_T f_s^{\alpha 1} B_T^{\beta 1} V_{eT}$
Inductor	Copper losses	$I^2_{prms}R_L$
losses	Core losses	$k_L f_s^{\alpha 2} B_L^{\beta 2} V_{eL}$
Capacitor loss	Ohmic losses	$R_C I^2_{Crms}$

TABLE III
DEFINITIONS OF THE SYMBOLS

Symbols	Definitions
R_{DSon}	Drain-source on-state resistance of the MOSFET
I_{Drms}	RMS value of the MOSFET on-state current
E_{onM}	Turn-on energy losses in the MOSFET
E_{offM}	Switch-off energy losses in the MOSFET
I_{prms}	RMS value of the transformer primary current
I_{srms}	RMS value of the transformer secondary current
R_{pri}	Equivalent transformer primary resistance
R_{sec}	Equivalent transformer secondary resistance
k, α, β	Steinmetz coefficients
B	Peak magnetic flux density
V_e	Core volume
R_L	Equivalent resistance of the auxiliary inductor
R_C	Equivalent series resistance of the capacitor
I_{Crms}	RMS current of the capacitor

The ZVS in the front-end circuit fails when using modulation methods that do not consider this ripple. The transformer primary and secondary currents contain ac components at the resonant frequency of the $L_\sigma C$ circuit, which can also influence the RMS value of the current. The efficiency of the converter may not be optimal when using the existing modulation methods that do not account for the ac-side capacitor voltage ripple. To optimize the efficiency of the converter and realize ZVS in the front-end circuit, an optimized modulation method is proposed in this section.

The optimization algorithm is employed to find the optimal values of D_1 and D_2 that satisfy the constraints of the optimization problem. The optimization problem is formulated as follows

$$\min_{\boldsymbol{z}} P_{loss}(t,\boldsymbol{z}) \tag{23}$$

subject to (16) and (24). $\boldsymbol{z}$ in (23) and (24) equals $[D_1; D_2]$. $P_{ref}(t)$ in (24) is given by (17), facilitating the realization of unity PF operation. In this article, ΔP_{ref} in (24) is set to 1W.

$$P(t,\boldsymbol{z}) \in [P_{ref}(t)-\Delta P_{ref}, P_{ref}(t)+\Delta P_{ref}] \tag{24}$$

The overall power losses of the DAB converter, P_{loss}, in (23) primarily consist of four components: power switch losses, transformer losses, inductor losses, and capacitor losses

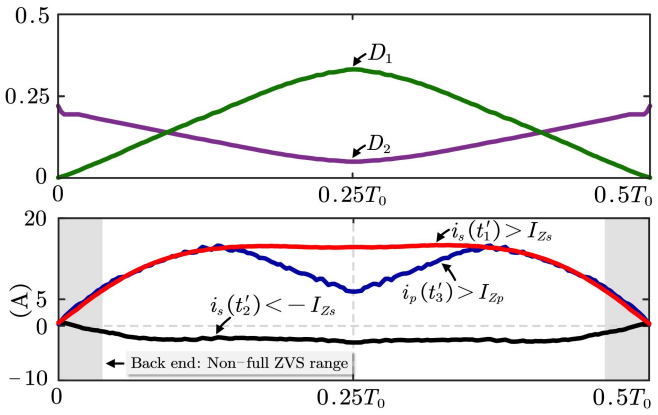


Fig. 8. Optimization results for an active power level of 500 W.

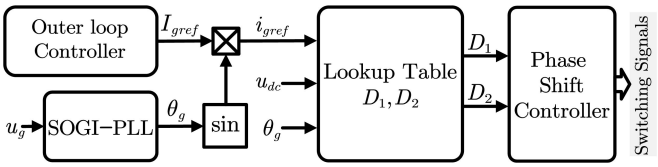
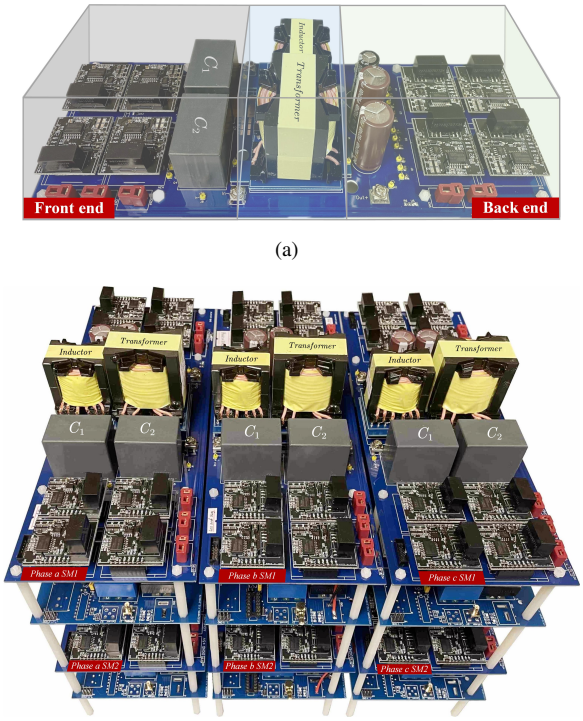


Fig. 9. Control block diagram of the ac-dc DAB converter.

[17]–[20]. The power switch losses include conduction losses and switching losses, while the power losses in the magnetic components consist of copper losses and core losses. The calculations for these power losses are summarized in Table II. The definitions of the symbols in Table II are provided in Table III.

Generally, in each switching cycle throughout the full period of the grid voltage, the optimal control variables D_1 and D_2 are derived by minimizing the power losses of the converter. The proposed steady-state analysis model should be utilized to calculate the current and voltage values of the converter for various values of D_1 and D_2. These results are then substituted into the power loss model to determine the overall power loss for specific control variables. In this study, a GA is employed for optimization. As GA is a widely used optimization method and has been extensively covered in the literature [21]–[24], detailed explanations are omitted here.

An example of the optimization results using the parameters listed in Table I is shown in Fig. 8. The active power reference is 500 W. It can be observed that the converter achieves ZVS in the front-end circuit over the full cycle of the grid voltage, indicated by $i_p(t_3^{'}) > I_{Zp}$. The back-end circuit does not achieve full ZVS operation under very light-load conditions, as indicated by the gray range. Specifically, S_3 and S_4 lose ZVS at load condition below 7%, and S_5 and S_6 lose ZVS at load condition below 3%. The constraints given in (18)–(20) are not treated as hard constraints for the proposed modulation and the optimization target is to maximize the power conversion efficiency. In the power losses calculation, if one switch realizes ZVS, the turn-on loss of this switch is zero, otherwise, the turn-on loss is calculated according to the equation shown in Table II. If ZVS of the power switches is treated as hard constraint, then power conversion efficiency



(a)

(b)

Fig. 10. Photographs of the prototypes. (a) The single-stage ac-dc DAB converter. (b) Three-phase SST with two modules in each phase.

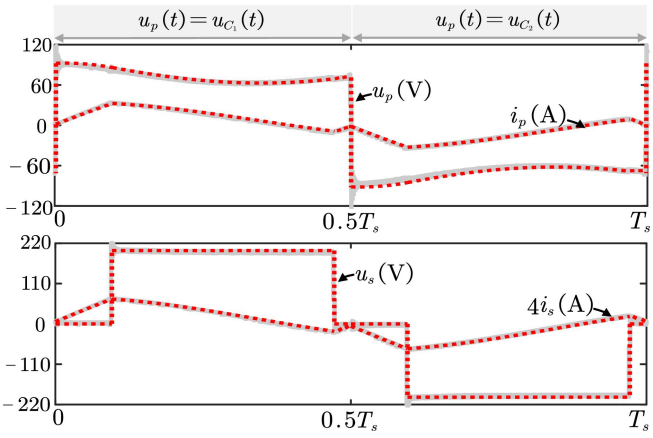


Fig. 11. Comparisons between the experimental results and theoretical analysis results using the proposed steady-state model.

will be subjected to ZVS realization.

The overall control block diagram of the ac-dc DAB converter is shown in Fig. 9. A second-order generalized integrator phase-locked loop (SOGI-PLL) is employed to track the phase angle of the grid voltage. Lookup tables are utilized to store the optimal control variables for various operating points. An outer-loop controller, such as dc-side voltage control or ac-side power control, can be used to generate the amplitude of the grid current reference.

VI. Experimental Results

The photograph of the ac-dc DAB converter is shown in Fig. 10 (a), and the corresponding parameters are listed in Table I. For higher voltage and power applications, additional converter modules can be assembled into a three-phase SST, as illustrated in Fig. 10 (b). In this configuration, each phase consists of two submodules, and the connection of these modules is depicted in Fig. 1(b). The experimental verification primarily focuses on the performance of a single module. The main controller used is DSP TMS320C28346, and the power switches employed are C3M0015065D from Wolfspeed.

The steady-state waveforms of the converter under the same conditions as those in Fig. 4 are shown in Fig. 11. The solid gray lines represent the experimental results, while the red dotted lines depict the theoretical analysis results based on the proposed steady-state model. It can be observed that they are well aligned with each other, verifying the correctness and accuracy of the proposed model.

The steady-state waveforms of the converter, using the modulation method presented in [12] (without considering the ac-side capacitor voltage ripple) and the proposed modulation method (which accounts for the voltage ripple), are shown in Fig. 12. Fig. 12 (a) and (b) depict the waveforms with 500 W output power, while Fig. 12 (c) and (d) illustrate the waveforms with 200 W output power. Under all conditions, the PF exceeds 0.99, and the grid current maintains a sinusoidal waveform with low total harmonic distortion (THD).

Zoomed-in waveforms of the transformer primary voltage (u_p) and primary current (i_p) are shown in Fig. 13. The current values within the red circles indicate whether ZVS is achieved in the circuit. According to the ZVS constraints discussed in Section IV, the front-end circuit fails to achieve ZVS when using the modulation method presented in [12]. In contrast, the proposed modulation method successfully achieves ZVS for the front-end cycloconverter. The peak values of the primary current shown in Fig. 13 (a)–(d) are 36.2 A, 32.2 A, 27.8, and 21.8 A, respectively. Correspondingly, the RMS values over one switching cycle are 19.8 A, 17.8 A, 14.0 A, and 11.1 A, respectively. By employing the proposed modulation approach, both the peak and RMS values of the primary current are significantly reduced. The switching dynamics of S_{1a} and S_{2a} are shown in Fig. 14. u_{ds} and u_{gs} are the drain-source voltage and gating signal, respectively. S_{1a} achieves ZVS using the proposed modulation method, while it loses ZVS with the modulation method presented in [12].

The efficiency of the converter under various power levels is shown in Fig. 15. Using the proposed modulation method, the efficiency is improved by over 2.66% at an active power of 500 W and by over 11.21% at 100 W. The experimental results indicate that neglecting the ac-side capacitor voltage ripple when designing the modulation method can significantly affect the power conversion efficiency of the converter.

VII. Conclusion

The impact of ac-side capacitor voltage ripple on the steady-state performance of matrix-type single-stage ac-dc DAB converter has not been thoroughly examined in the existing literature. This study develops a time-domain steady-state model that incorporates capacitor voltage ripple to accurately characterize the operating performance of the converter. The

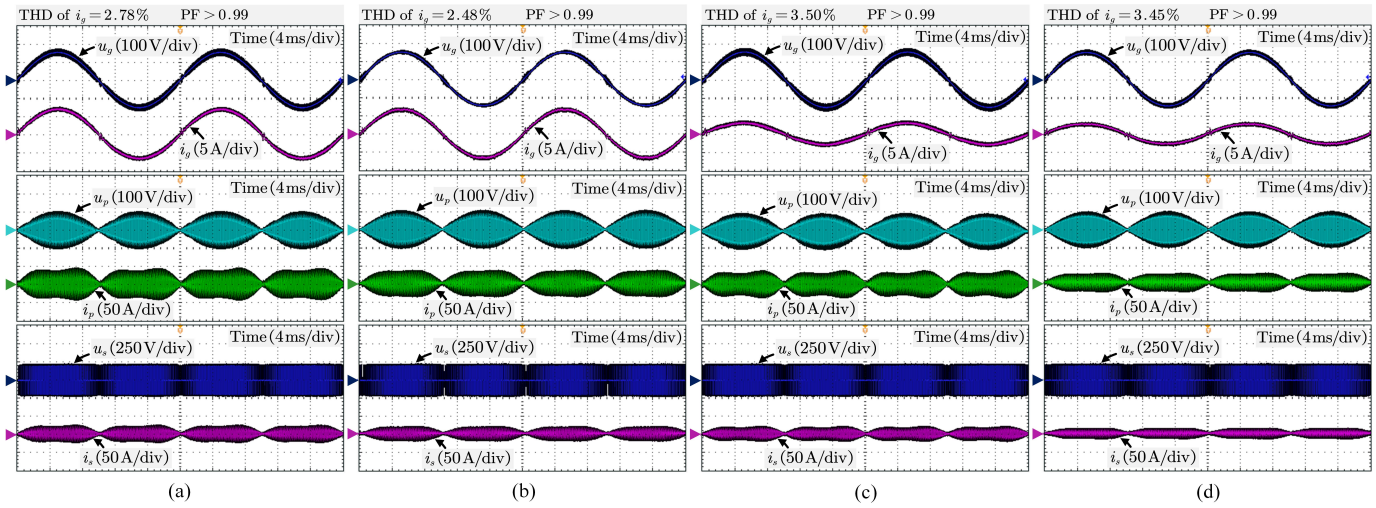


Fig. 12. Steady-state waveforms of the ac-dc DAB converter. (a) and (b): 500 W output power. (c) and (d): 200 W output power. (a) and (c): using the modulation method presented in [12]. (b) and (d): using the proposed modulation method.

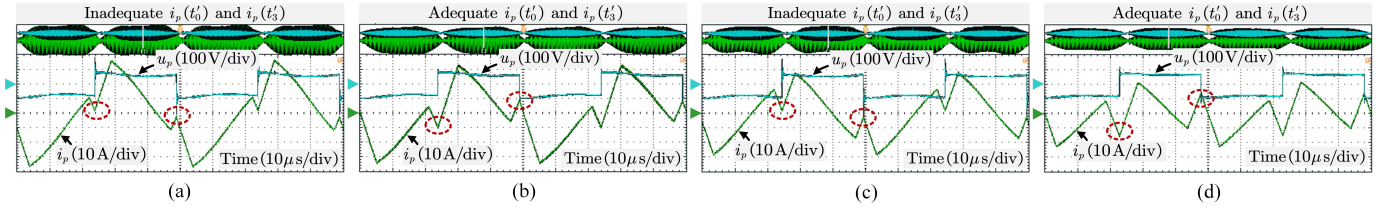


Fig. 13. Zoomed-in waveforms of the transformer primary voltage and current. The power levels and modulation methods in conditions (a)–(d) of Fig. 13 correspond to those shown in Fig. 12 (a)–(d).

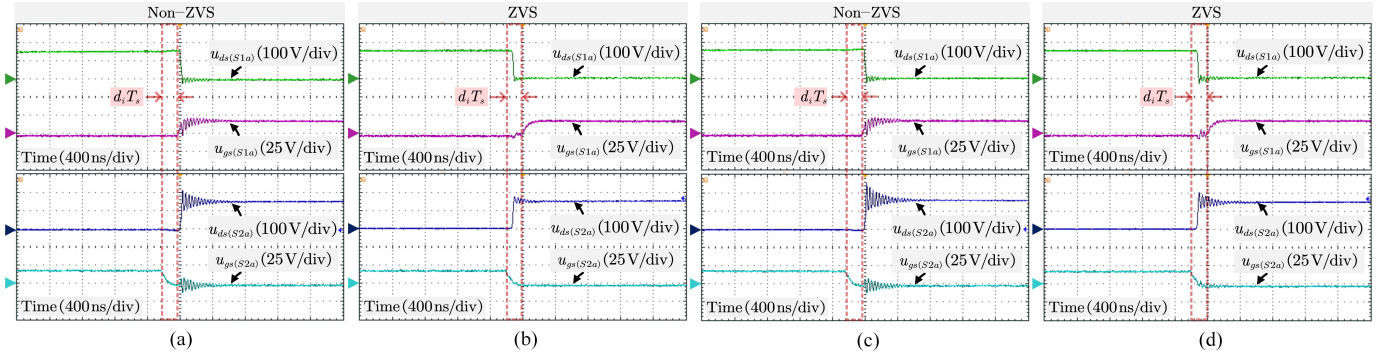


Fig. 14. Zoomed-in waveforms of the switching dynamics. The power levels and modulation methods in conditions (a)–(d) of Fig. 14 correspond to those shown in Fig. 12 (a)–(d).

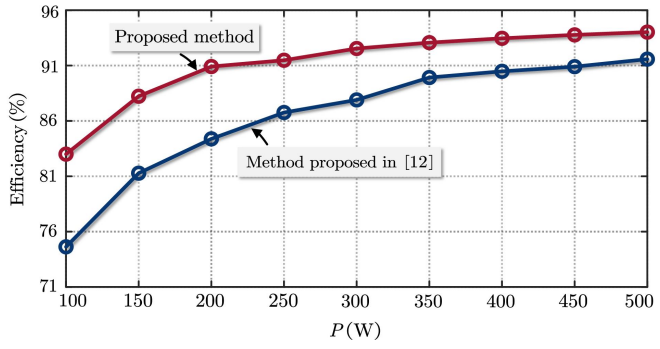


Fig. 15. Efficiency of the converter under various power levels.

findings indicate that ac-side capacitor voltage ripple can lead to the failure of ZVS operation in the front-end circuit if the modulation strategy is designed based on a simplified steady-state model that neglects this ripple. Additionally, the capacitor voltage ripple affects the waveforms of the transformer primary and secondary currents, thereby further influencing the power losses of the converter. An optimized modulation method is subsequently proposed to achieve unity PF, realize ZVS operation, and enhance power conversion efficiency. Simulation and experimental results are presented to validate the theoretical analysis. Future research in this area will focus on the multi-objective design of the converter, considering the effects of ac-side capacitor voltage ripple. The proposed systematic analysis and optimization scheme can also be extended to other matrix-type converter families, such as full-bridge and multi-port ac-dc DAB converters with small ac-side capacitance [26]–[31].

APPENDIX

Transformer primary current $i_p(t)$ and capacitor voltage $u_{C_1}(t)$ are expressed as follows

$$\begin{aligned} i_p(t) =& i_p(t_x)\cos[\omega_r(t-t_x)] + \frac{u_{C_1}(t_x)}{L_\sigma\omega_r}\sin[\omega_r(t-t_x)] - \\ & i_g\{\cos[\omega_r(t-t_x)]-1\} - \frac{yu_{dc}}{nL_\sigma\omega_r}\sin[\omega_r(t-t_x)] \end{aligned} \tag{A1}$$

$$\begin{aligned} u_{C_1}(t) =& -L_\sigma\omega_r i_p(t_x)\sin[\omega_r(t-t_x)] + u_{C_1}(t_x)\cos[\omega_r(t- \\ & t_x)] + L_\sigma\omega_r i_g\sin[\omega_r(t-t_x)] - \frac{yu_{dc}}{n}\{\cos[\omega_r(t- \\ & t_x)]-1\} \end{aligned} \tag{A2}$$

where $\omega_r = \sqrt{\frac{1}{L_\sigma C}}$, x and y are given as

$$x = \begin{cases} 0 & \text{Modulation stage I} \\ 1 & \text{Modulation stage II} \\ 2 & \text{Modulation stage III} \end{cases} \tag{A3}$$

$$y = \begin{cases} 0 & \text{Modulation stages I and III} \\ 1 & \text{Modulation stage II} \end{cases} \tag{A4}$$

The expressions of $i_p(t_0)$, $i_p(t_1)$, $i_p(t_2)$, $i_p(t_3)$, $u_{C_1}(t_0)$, $u_{C_1}(t_1)$, $u_{C_1}(t_2)$ and $u_{C_1}(t_3)$ can be obtained by substituting t_0, t_1, t_2 and t_3 into (A1) and (A2).

The grid current is expressed as

$$i_g = Q_2 i_p(t_0) + Q_3 u_{C_1}(t_0) + Q_4 \tag{A5}$$

where Q_1, Q_2, Q_3 and Q_4 are given by

$$\begin{aligned} Q_1 = 1 + \frac{2u_{dc}}{T_s n u_g}\{ & \frac{\sin[\omega_r(t_2-t_0)]-\sin[\omega_r(t_1-t_0)]}{\omega_r} - \\ & t_2 + t_1 \} \end{aligned} \tag{A6}$$

$$Q_2 = \frac{2u_{dc}}{Q_1\omega_r T_s n u_g}\{\sin[\omega_r(t_2-t_0)]-\sin[\omega_r(t_1-t_0)]\} \tag{A7}$$

$$Q_3 = \frac{2u_{dc}}{Q_1 L_\sigma\omega_r^2 T_s n u_g}\{\cos[\omega_r(t_1-t_0)]-\cos[\omega_r(t_2-t_0)]\} \tag{A8}$$

$$Q_4 = \frac{2u_{dc}^2}{Q_1 L_\sigma\omega_r^2 T_s n^2 u_g}\{\cos[\omega_r(t_2-t_1)]-1\} \tag{A9}$$

A matrix equation, denoted as (A10), is formulated to calculate the current and voltage values for given circuit parameters and control variables D_1 and D_2.

$$\boldsymbol{A}\boldsymbol{x} = \boldsymbol{b} \tag{A10}$$

where $\boldsymbol{x}$, $\boldsymbol{b}$, and $\boldsymbol{A}$ are given by

$$\begin{aligned} \boldsymbol{x}^T = [& i_p(t_0), i_p(t_1), i_p(t_2), i_p(t_3), \\ & u_{C_1}(t_0), u_{C_1}(t_1), u_{C_1}(t_2), u_{C_1}(t_3)]^T \end{aligned} \tag{A11}$$

$$\boldsymbol{b}^T = [b_1, b_2, b_3, b_4, b_5, b_6, b_7, b_8]^T \tag{A12}$$

where

$b_1 = Q_4\{\cos[\omega_r(t_1-t_0)]-1\}$,

$b_2 = Q_4\{\cos[\omega_r(t_2-t_0)]-1\} + \frac{u_{dc}}{nL_\sigma\omega_r}\sin[\omega_r(t_2-t_1)]$,

$b_3 = Q_4\{\cos[\omega_r(t_3-t_0)]-1\} + \frac{u_{dc}}{nL_\sigma\omega_r}\{\sin[\omega_r(t_3-t_1)]-\sin[\omega_r(t_3-t_2)]\}$, $b_4 = 0$,

$b_5 = -Q_4 L_\sigma\omega_r\sin[\omega_r(t_1-t_0)]$,

$b_6 = -Q_4 L_\sigma\omega_r\sin[\omega_r(t_2-t_0)] + \frac{u_{dc}}{n}\{\cos[\omega_r(t_2-t_1)]-1\}$,

$b_7 = -Q_4 L_\sigma\omega_r\sin[\omega_r(t_3-t_0)] + \frac{u_{dc}}{n}\{\cos[\omega_r(t_3-t_1)]-\cos[\omega_r(t_3-t_2)]\}$,

$b_8 = \frac{u_g T_s}{2} - \frac{Q_4 T_s^2}{8C} - \frac{u_{dc}(t_2-t_1)}{n}$.

$$\boldsymbol{A} = \begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} & a_{15} & a_{16} & a_{17} & a_{18} \\ a_{21} & a_{22} & a_{23} & a_{24} & a_{25} & a_{26} & a_{27} & a_{28} \\ a_{31} & a_{32} & a_{33} & a_{34} & a_{35} & a_{36} & a_{37} & a_{38} \\ a_{41} & a_{42} & a_{43} & a_{44} & a_{45} & a_{46} & a_{47} & a_{48} \\ a_{51} & a_{52} & a_{53} & a_{54} & a_{55} & a_{56} & a_{57} & a_{58} \\ a_{61} & a_{62} & a_{63} & a_{64} & a_{65} & a_{66} & a_{67} & a_{68} \\ a_{71} & a_{72} & a_{73} & a_{74} & a_{75} & a_{76} & a_{77} & a_{78} \\ a_{81} & a_{82} & a_{83} & a_{84} & a_{85} & a_{86} & a_{87} & a_{88} \end{bmatrix} \tag{A13}$$

where

$a_{11} = \cos[\omega_r(t_1-t_0)] + Q_2\{1-\cos[\omega_r(t_1-t_0)]\}$,

$a_{15} = \frac{\sin[\omega_r(t_1-t_0)]}{L_\sigma\omega_r} + Q_3\{1-\cos[\omega_r(t_1-t_0)]\}$,

$a_{21} = \cos[\omega_r(t_2-t_0)] + Q_2\{1-\cos[\omega_r(t_2-t_0)]\}$,

$a_{25} = \frac{\sin[\omega_r(t_2-t_0)]}{L_\sigma\omega_r} + Q_3\{1-\cos[\omega_r(t_2-t_0)]\}$,

$a_{31} = \cos[\omega_r(t_3-t_0)] + Q_2\{1-\cos[\omega_r(t_3-t_0)]\}$,

$a_{35} = \frac{\sin[\omega_r(t_3-t_0)]}{L_\sigma\omega_r} + Q_3\{1-\cos[\omega_r(t_3-t_0)]\}$,

$a_{51} = (Q_2-1)L_\sigma\omega_r\sin[\omega_r(t_1-t_0)]$,

$a_{55} = \cos[\omega_r(t_1-t_0)] + Q_3 L_\sigma\omega_r\sin[\omega_r(t_1-t_0)]$,

$a_{61} = (Q_2-1)L_\sigma\omega_r\sin[\omega_r(t_2-t_0)]$,

$a_{65} = \cos[\omega_r(t_2-t_0)] + Q_3 L_\sigma\omega_r\sin[\omega_r(t_2-t_0)]$,

$a_{71} = (Q_2-1)L_\sigma\omega_r\sin[\omega_r(t_3-t_0)]$,

$a_{75} = \cos[\omega_r(t_3-t_0)] + Q_3 L_\sigma\omega_r\sin[\omega_r(t_3-t_0)]$,

$a_{81} = \frac{Q_2 T_s^2}{8C} - L_\sigma$, $a_{85} = \frac{Q_2 T_s^2}{8C}$,

$a_{12} = a_{23} = a_{34} = a_{56} = a_{67} = a_{78} = -1$,

$a_{41} = a_{44} = 1, a_{84} = L_\sigma, a_{88} = \frac{T_s}{2}$,

$a_{13} = a_{14} = a_{16} = a_{17} = a_{18} = 0$,

$a_{22} = a_{24} = a_{26} = a_{27} = a_{28} = 0$,

$a_{32} = a_{33} = a_{36} = a_{37} = a_{38} = 0$,

$a_{42} = a_{43} = a_{45} = a_{46} = a_{47} = a_{48} = 0$,

$a_{52} = a_{53} = a_{54} = a_{57} = a_{58} = 0$,

$a_{62} = a_{63} = a_{64} = a_{66} = a_{68} = 0$,

$a_{72} = a_{73} = a_{74} = a_{76} = a_{77} = 0$,

$a_{82} = a_{83} = a_{86} = a_{87} = 0$.

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