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An Online Gate Oxide Degradation Monitoring Method for SiC MOSFETs Based on Turn-ON Gate Current Change Rate

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***Abstract*—Gate oxide degradation (GOD) presents a reliability issue for silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs), especially under high-temperature and high-electric-field conditions. This letter proposes an online condition monitoring (CM) method based on the peak value of the turn-on gate current change rate ($di_g/dt_{,max}$). The technique utilizes a non-invasive PCB Rogowski coil to measure $di_g/dt_{,max}$, demonstrating high practicality. Accelerated aging tests under positive and negative high-temperature gate bias (HTGB) and high-temperature gate switching (HTGS) conditions reveal correlations between $di_g/dt_{,max}$ and GOD, with variations of 5.61%, 5% and 8.33%, after 160 hours of aging. Double pulse test (DPT) results indicate that $di_g/dt_{,max}$ is independent of external factors such as temperature, drain-source voltage (V_{ds}), drain current (I_{ds}) and package aging. Results from a buck converter further validate the feasibility of long-term online monitoring.**

***Index Terms*—condition monitoring, gate current, gate oxide, PCB Rogowski coil, SiC MOSFET.**

I. Introduction

Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) have significantly improved the efficiency and power density of electronic devices due to their excellent characteristics. The performance of SiC MOSFETs has gained initial market recognition [1]. For example, SiC technology provides faster charging speeds, higher efficiency, and lighter designs in electric vehicles. However, the reliability of the gate oxide in SiC MOSFETs remains a major challenge in their development. Furthermore, power devices serve as the core components of power electronic converters and represent the most vulnerable parts of the system. Research indicates that power devices exhibit the highest failure rate in converter systems, accounting for about 31% [2]. Therefore, it is essential to implement online condition monitoring (CM) of the SiC MOSFET gate oxide.

Many studies have proposed various parameters and methods for monitoring the gate oxide degradation (GOD) in SiC MOSFETs. The commonly used electrical parameters for gate oxide CM can be categorized into three types: static and dynamic parameters and parameters based on parasitic capacitance. Static parameters include threshold voltage (V_{TH}), on-state resistance ($R_{ds,on}$), body diode voltage (V_{sd}), and gate leakage current (I_{GSS}) [3]-[5]. Dynamic parameters include transconductance (g_m), switching waveforms, such as turn-on ($t_{d,on}$) and turn-off ($t_{d,off}$) delay times, Miller plateau time (t_{GP}) and voltage (V_{GP}), as well as turn-on di_{ds}/dt with fixed delay time ($di_{ds}/dt_{,delay}$) and the peak value of the bandpass filtered gate voltage during turn-on transitions ($V_{GS,M}$) [6]-[10]. Parameters based on parasitic capacitance include gate-source capacitance (C_{GS}), gate-drain capacitance (C_{GD}), input capacitance (C_{iss}), gate charge (Q_{GC}), and gate charging time (t_{GC}) [11]-[13].

All parameters except those related to parasitic capacitance are temperature-sensitive. However, temperature compensation is very challenging. V_{TH} requires simultaneous capturing of the gate-source voltage V_{GS} and I_{ds} during the turn-on transient, in addition to the high sensitivity to T_j, which makes online measurement difficult. $R_{ds,on}$ is affected by both chip and package, and package-related degradation also affects its value. This makes it the most commonly used parameter for monitoring package aging. Monitoring V_{sd} for GOD requires injecting a small current, which limits its feasibility in real operating conditions. I_{GSS} is another parameter related to GOD. However, I_{GSS} is typically nA level in the healthy state and only jumps to mA level in the late stages of aging. Therefore, this parameter is more suitable for failure warning rather than CM.

For switching transient parameters, the fast switching speed makes online measurement difficult and susceptible to noise interference. Typically, the switching speed is usually reduced by increasing the gate drive resistance $R_{g,on}$. However, this method complicates the drive circuit and limits the advantage of the fast-switching capability of SiC MOSFETs. Finally, these parameters are also influenced by V_{ds} and/or I_{ds}. In [9] it was proven that the $di_{ds}/dt_{,delay}$ has a low temperature sensitivity and is less affected by V_{ds} and I_{ds}. However, only its feasibility under a limited number of pulse conditions was assessed, and no long-term experimental validation was conducted. Calibration of $V_{GS,M}$ is relatively complex and requires an offline adjustment of the filter frequency [10].

The authors studied the relationship between changes in C_{GS}, C_{GD}, C_{iss} and aging [11], [12]. The sensitivity of parasitic capacitance to aging is low, typically resulting in changes at the pF level, although it is insensitive to T_j and unrelated to package aging. This makes online measurement extremely challenging, and is usually only possible through offline measurement. To address this problem, researchers in [12], [13] converted the changes in parasitic capacitance into equivalent changes in Q_{GC} and t_{GC}. However, monitoring Q_{GC} requires interrupting the normal operating sequence, which complicates the control strategy. Measuring t_{GC} needs two sets of drive circuits, resulting in a complex circuit structure and significantly increased cost.

This letter proposes using $di_g/dt_{,max}$ as a precursor to GOD and presents a PCB Rogowski coil-based detection method for monitoring SiC MOSFETs. The $di_g/dt_{,max}$ has advantages over traditional CM methods, including non-invasiveness, ease of integration, low temperature sensitivity, and independence from V_{ds} and I_{ds} compared. Furthermore, this parameter can effectively decouple the impact of packaging aging. It can be utilized to monitor the health status of SiC MOSFETs.

II. Gate Oxide Degradation in SiC MOSFET

A. Input Capacitance Characteristics

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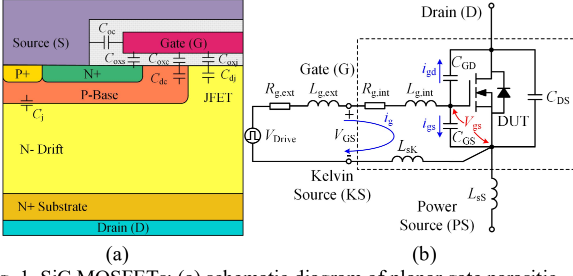

(a) (b)

Fig. 1. SiC MOSFETs: (a) schematic diagram of planar gate parasitic capacitance; and (b) equivalent circuit.

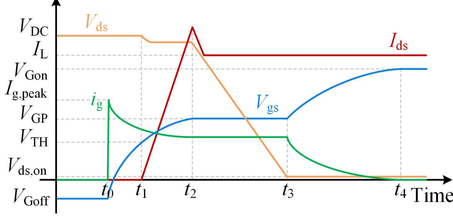

Fig. 2. Simplified SiC MOSFET turn-on waveform schematic.

The process of defect charge trapping inevitably affects the electrical characteristics of SiC MOSFETs. A typical planar gate MOSFET structure and its parasitic capacitance diagram are depicted in Fig. 1(a). C_{iss} consists of C_{GS} and C_{GD}. C_{GS} is composed of the gate-source electrode capacitance C_{oc}, the gate-n$^+$ source region capacitance C_{oxs}, the gate-p-well region surface capacitance C_{oxc}, and the depletion layer capacitance C_{dc} under the gate in the p-well region. Among these, only C_{dc} varies with V_{GS}. C_{GD} is equivalent to a series combination of the gate-drain oxide capacitance C_{oxj} and the drain depletion capacitance C_{dj} beneath the gate oxide layer. Similar to C_{dc}, C_{dj} also varies with V_{GS}. C_{GS} and C_{GD} can be expressed as follows:

$$C_{GS} = C_{oc} + C_{oxs} + \frac{C_{oxc} C_{dc}}{C_{oxc} + C_{dc}} \tag{1}$$

$$C_{GD} = \frac{C_{oxj} C_{dj}}{C_{oxj} + C_{dj}} \tag{2}$$

C_{oc}, C_{oxs}, C_{oxc} and C_{oxj} are determined by the gate oxide structure and not affected by voltage or temperature. The depletion layer capacitances C_{dc} and C_{dj} are given by the following equations, assuming that they are the depletion layer capacitance of a MOS capacitor [12]:

$$C_{dc} = C_{dj} = \frac{C_{ox}}{\sqrt{1 + \frac{2C_{ox}^2 \left(V_{GS} + Q_{ox}/C_{ox}\right)}{qN\varepsilon_s}} - 1}. \tag{3}$$

where C_{ox} and Q_{ox} are gate oxide capacitance and charge. N is the density of the majority carrier. q is the elementary charge, and ε_s is the dielectric constant of the semiconductor.

The above analysis indicates that changes in the Q_{ox} at the gate oxide-semiconductor interface will result in corresponding variations in C_{GS} and C_{GD} as degradation progresses.

B. Degradation Effect on Turn-On $di_g/dt_{,max}$

This letter analyzes $di_g/dt_{,max}$ and uses it as a precursor for GOD. Fig. 2 shows the simplified waveform of the SiC MOSFET turn-on process, which is divided into four stages: turn-on delay stage (t_0 to t_1), current rise stage (t_1 to t_2), Miller plateau stage (t_2 to t_3), and the V_{GS} rise from V_{GP} to V_{Gon} stage (t_3 to t_4). As shown in Fig. 2, the gate current i_g gradually decreases after reaching its peak value during the transient turn-on. Therefore, $di_g/dt_{,max}$ appears during the turn-on delay stage. During this stage, V_{ds} and I_{ds} remain constant, and i_g charges the C_{iss} through the $R_{g,on}$. The equivalent circuit of the SiC MOSFET is depicted in Fig. 1(b). In this case, i_g can be expressed as:

$$i_g = (C_{GS} + C_{GD})\frac{dV_{gs}}{dt} \approx \frac{V_{GS} - V_{gs}}{R_{g,int}} \tag{4}$$

According to (4), the expression for V_{gs} is:

$$V_{gs} = V_{Gon} + (V_{Goff} - V_{Gon})e^{-\frac{t}{(C_{GS}+C_{GD})\cdot R_{g,int}}} \tag{5}$$

where V_{Gon} and V_{Goff} are the gate driving ON/OFF voltage. By substituting (5) into (4), the expression of gate current change rate di_g/dt can be obtained as follows:

$$\frac{di_g}{dt} = \frac{V_{Goff} - V_{Gon}}{\left(C_{GS} + C_{GD}\right) \cdot R_{g,int}^2} e^{-\frac{t}{(C_{GS}+C_{GD})\cdot R_{g,int}}} < 0 \tag{6}$$

The second order derivative of the i_g can be expressed as:

$$\frac{d^2 i_g}{dt^2} = \frac{V_{Gon} - V_{Goff}}{\left(C_{GS} + C_{GD}\right)^2 \cdot R_{g,int}^3} e^{-\frac{t}{(C_{GS}+C_{GD})\cdot R_{g,int}}} > 0 \tag{7}$$

The d^2i_g/dt^2 is greater than 0, indicating that the di_g/dt is increasing monotonically, and since the di_g/dt is constantly less than 0, the absolute value of the $di_g/dt_{,max}$ occurs at the moment t_0, which can be expressed as:

$$|di_g/dt_{,max}| = \frac{V_{Gon} - V_{Goff}}{\left(C_{GS} + C_{GD}\right) \cdot R_{g,int}^2} \tag{8}$$

GOD causes variations in C_{iss} as discussed earlier. Consequently, an increase in C_{iss} will reduce $di_g/dt_{,max}$, while a decrease in C_{iss} will increase $di_g/dt_{,max}$. Based on the above analysis, it can be concluded that $di_g/dt_{,max}$ depends solely on GOD and is unaffected by T_j, V_{ds} or I_{ds}. Moreover, this change effectively decouples the issue of package aging. Therefore, $di_g/dt_{,max}$ can serve as an indicator for GOD.

III. $DI_G/DT_{,MAX}$ EXTRACTION APPROACH

A. Operating Principle of PCB Rogowski Coil

The Rogowski coil is commonly used to measure alternating current (AC) and transient current. Its operating principle is based on Faraday's law of electromagnetic induction and Ampere's circuital law. The structure of a traditional Rogowski coil primarily consists of a coil wound around a flexible non-magnetic frame, along with a return wire, as shown in Fig. 3(a). When a current-carrying conductor perpendicular to the plane of the coil generates a change in magnetic flux, the coil outputs the differential of the induced signal, which represents the rate of change of the measured current i.

The PCB Rogowski coil utilizes copper traces and vias on a PCB board to replace the winding of a traditional Rogowski coil, as depicted in Fig. 3(b), achieving more flexible designs and simplified manufacturing processes. The output voltage (v_p) of the coil is directly proportional to the rate of change of the measured current i, and the v_p can be expressed as:

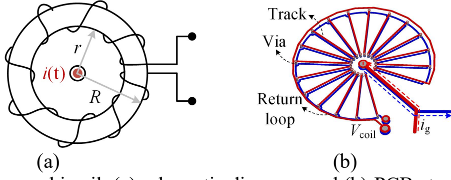

Fig. 3. Rogowski coil: (a) schematic diagram; and (b) PCB structure.

$$v_p = \frac{N_c \mu_0 h}{2\pi} \cdot \ln \frac{R}{r} \cdot \frac{di(t)}{dt} = M \frac{di(t)}{dt} \tag{9}$$

where N_c is the number of coil turns, μ_0 is the magnetic permeability in vacuum, $\mu_0 = 4\pi \cdot 10^{-7}$ H/m, R is the outer diameter, r is the inner diameter, h is the thickness of the PCB board, and M is the coil mutual inductance.

TABLE I
PARAMETERS OF DESIGNED PCB ROGOWSKI COIL

Parameter	Value	Parameter	Value
Outer diameter R	10.061 mm	Coil turns N_c	18
Inner diameter r	1.902 mm	PCB thickness h	1.6 mm
Trace width W	0.254 mm	Trace thickness d	0.035 mm

B. Design of the PCB Rogowski Coil

Measurement bandwidth is a critical parameter of the Rogowski coil. The design bandwidth of the PCB Rogowski coil is affected by its planar traces, vias, and pads, especially the parameter constraints between the traces and vias. Based on the widely used lumped parameter model of the Rogowski coil, its upper resonant frequency f_H is given by:

$$f_H = \frac{1}{2\pi\sqrt{L_S C_S}} \tag{10}$$

where L_S is the parasitic inductance generated by the PCB trace, and C_S is the parasitic capacitance between the traces. In the lumped parameter model, L_S and C_S can be expressed as:

$$L_S = \frac{N_c^2 \mu_0 h}{2\pi} \cdot \ln \frac{R}{r} \tag{11}$$

$$C_S = \frac{\varepsilon_0 \varepsilon_r W l}{h} \tag{12}$$

where ε_0 and ε_r are the vacuum dielectric constant and the relative dielectric constant of the PCB material, respectively, W is the trace width, and l is the total length of the trace.

The formula for measuring the equivalent bandwidth BW of edge signals is [9]:

$$BW = \frac{0.35}{t_r} \tag{13}$$

where t_r represents the rise time of the signal. For discrete SiC MOSFETs, the i_g rise time is typically about 10 ns. According to this formula, the measurement bandwidth of di_g/dt requires at least 35 MHz.

The structural parameters of the coil designed in this section is shown in Table I. Substituting the structural parameters into (10)-(12), with $\varepsilon_0 = 8.854\times10^{-12}$ F/m and ε_r of FR-4 as 5, the calculated f_H of the PCB Rogowski coil is 266 MHz. Therefore, the structural design parameters used in this letter can meet the di_g/dt measurement requirements.

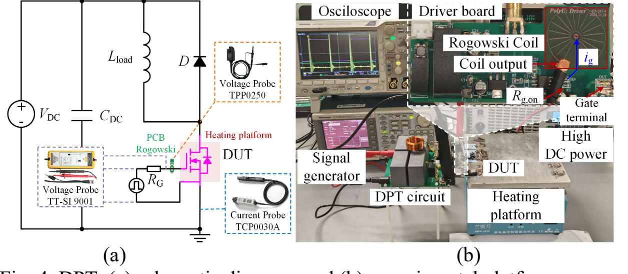

Fig. 4. DPT: (a) schematic diagram; and (b) experimental platform.

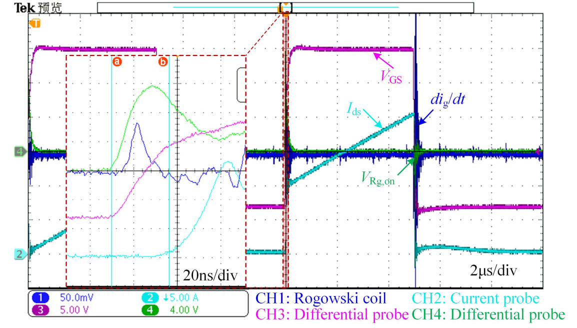

Fig. 5. Experimental waveforms of DPT (V_{GS} = +15/-8 V, $R_{g,on}$ = 15 Ω).

IV. EXPERIMENTAL VERIFICATION

A. Double Pulse Test Verification

This letter uses the high-temperature gate bias (HTGB) test, as specified in standard JESD 22-A108D, to conduct an aging test on the gate oxide layer. The objective is to validate the effectiveness of the proposed CM for GOD based on $di_g/dt_{,max}$. Considering the bias temperature instability (BTI) problem of SiC MOSFET, this letter adopted three accelerated aging test schemes, positive HTGB (P-HTGB), negative HTGB (N-HTGB), and high-temperature gate switching (HTGS) test. The device under test (DUT) is a TO-247-4 packaged discrete planar gate SiC MOSFET, model C3M0075120K. During the aging test, the DUT is placed on a heating platform at 175 °C, with the drain-source short-circuited and a high V_{GS} applied. The high temperature and high V_{GS} stress were maintained for 160 h throughout the test. The aging test was paused every 20 h, followed by a 5 h cooling period. The V_{GS} is set to 30 V in the P-HTGB test, and V_{GS} is set to -20 V in the N-HTGB test. The V_{GS} is set to +25/-15 V with a duty cycle of 0.5 and a switching frequency of 100 kHz in the HTGS test.

This section analyzes and compares the changes in $di_g/dt_{,max}$ before and after aging with DPT. The schematic diagram and experimental platform of the DPT are shown in Fig. 4, and the experimental waveforms are shown in Fig. 5. A PCB Rogowski coil is integrated into the drive circuit, which operates with a gate voltage of +15/-8 V and $R_{g,on}$ = 5.1 Ω, as shown in Fig. 4(b). The $di_g/dt_{,max}$ waveforms of the DUT are presented in Fig. 6 after 160 h of P-HTGB, N-HTGB, and HTGS aging tests. The experimental results indicate that in the P-HTGB test, $di_g/dt_{,max}$ gradually decreases with aging, showing a reduction of 5.61% after 160 h; while in both the N-HTGB and HTGS test, it gradually increases, exhibiting a rise of 5% and 8.33% after 160 h. To verify the relationship between the C_{iss} and $di_g/dt_{,max}$ in

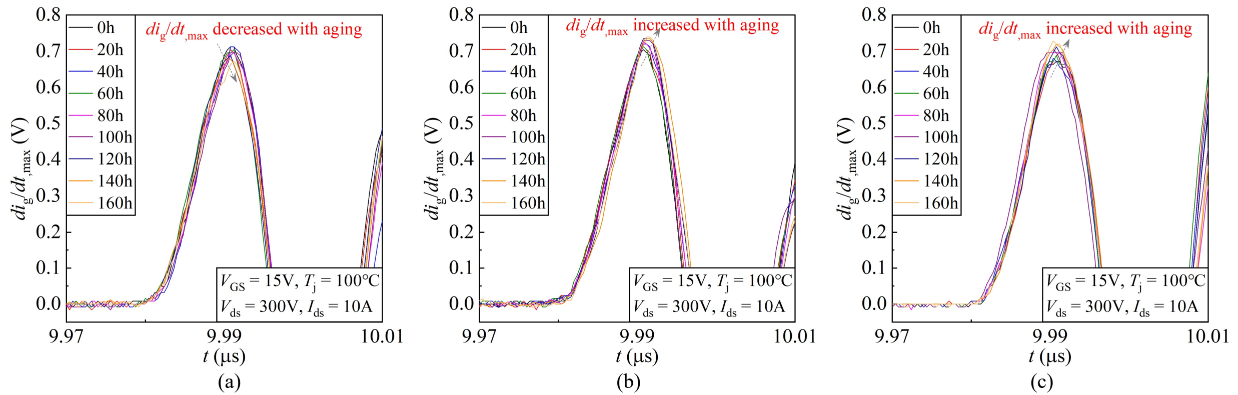

Fig. 6. Waveforms of $di_g/dt_{,max}$: (a) P-HTGB; (b) N-HTGB; and (c) HTGS.

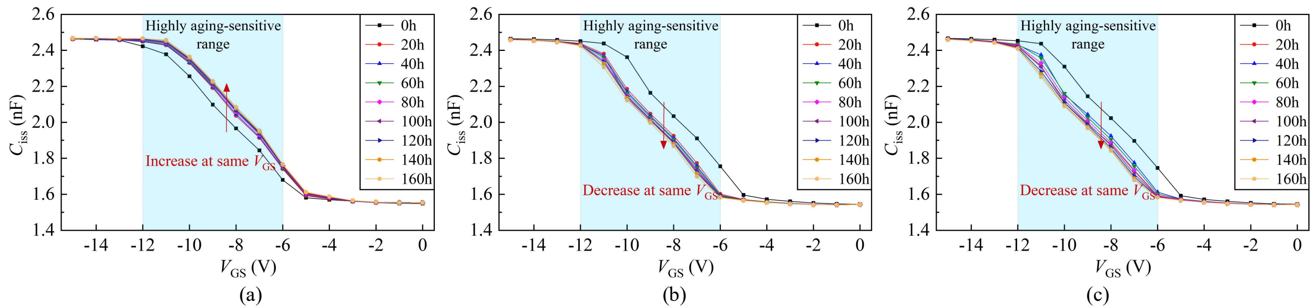

Fig. 7. Changes of C_{iss}: (a) P-HTGB; (b) N-HTGB; and (c) HTGS.

Section II, the experimental results of the C_{iss} are shown in Fig. 7. It is consistent with the theoretical analysis. As shown in (8), P-HTGB increases the C_{iss} of the SiC MOSFET, while N-HTGB decreases it, which is consistent with the results reported in references [11]-[13]. Furthermore, since the current GOD parameters are mainly affected by the T_j, the variations in $di_g/dt_{,max}$ at different times and T_j for V_{ds} = 300 V, I_{ds} = 10 A were also tested. The test results are shown in Fig. 8. The results demonstrate that although $di_g/dt_{,max}$ occasionally increases in the P-HTGB test, its overall trend remains downward. Similarly, it occasionally decreases in the N-HTGB test, but the overall trend is upward.

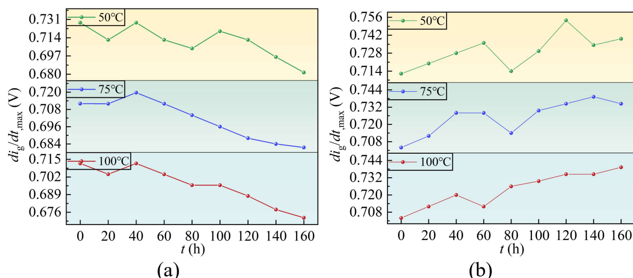

Fig. 8. Changes of $di_g/dt_{,max}$: (a) P-HTGB; and (b) N-HTGB.

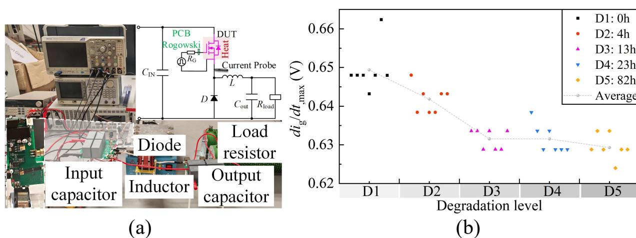

Fig. 9. Buck converter: (a) experimental platform; and (b) test results.

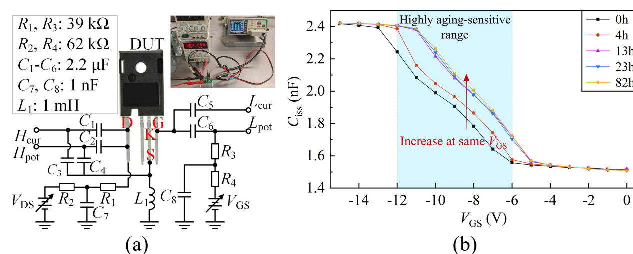

Fig. 10. C_{iss}-V_{GS} Measurement: (a) schematic diagram; and (b) test results.

B. Buck Converter Verification

This section constructs a buck converter as depicted in Fig. 9(a), to validate the feasibility of long-term online monitoring. Since device lifetime depends on stress conditions, aging tests under normal operation take a long time. To accelerate device degradation and induce significant gate oxide aging in the DUT earlier, this letter places the DUT on a heating platform with the temperature set to 100 °C and the V_{GS} set to +15/-8 V. The converter operates at a switching frequency of 200 kHz, with a duty cycle D of 0.5, an inductor L of 1.5 mH, an output capacitor C_{out} of 120 μF, and a load resistance R_{load} of 10 Ω. The maximum allowable operating T_j is 150 °C, according to the DUT datasheet. To ensure safe and reliable operation, a thermal imager is used to monitor the case temperature (T_c) of the DUT in real time. T_c is maintained at about 130 °C by adjusting the bus voltage. Under this condition, the bus voltage is 260 V and the load current is approximately 13 A. The changes of $di_g/dt_{,max}$ at different degradation times are shown in Fig. 9(b), after 82 h of continuous accelerated aging testing. The experimental results demonstrate that $di_g/dt_{,max}$ gradually decreases during the aging process, indicating an increase in the C_{iss} of the DUT. To

validate the above conclusion, a C_{iss} measurement circuit was built as shown in Fig. 10(a). Fig. 10(b) shows the measured C_{iss} values at different degradation periods and V_{GS} of the buck converter. The results confirm that C_{iss} increases with aging at a V_{GS} of -8 V, leading to a gradual reduction in $di_g/dt_{,max}$.

Based on the above analysis, the experimental results prove the feasibility of using $di_g/dt_{,max}$ to monitor the degradation state of gate oxide. Furthermore, the CM method based on $di_g/dt_{,max}$ shows weak coupling with package aging, temperature, load current and bus voltage, demonstrating greater applicability. Additionally, the use of PCB Rogowski coil can achieve non-contact measurement, which has the advantage of being non-invasive compared to RC passive differential circuits. Meanwhile, its mature manufacturing process and excellent scalability ensure that no major issues arise in terms of cost and complexity. However, the method proposed in this letter has some drawbacks when contrasted with traditional monitoring schemes: first, the change in the device before and after aging is relatively small, requiring adjustment through subsequent processing circuits; second, the design of the peak extraction circuit requires the use of high-bandwidth operational amplifiers, which poses certain challenges in circuit design.

V. Conclusion

An online CM method for GOD in SiC MOSFETs using $di_g/dt_{,max}$ has been proposed. A clear relationship between $di_g/dt_{,max}$ and GOD is shown by theoretical and experimental results. Specifically, GOD increases C_{iss}, and $di_g/dt_{,max}$ decreases; conversely, $di_g/dt_{,max}$ increases. It is recorded that $di_g/dt_{,max}$ is decreased by 5.61% in P-HTGB and is increased by 5% and 8.33% in N-HTGB and HTGS after 160 hours of accelerated aging. C_{iss} is increased by 12.41%, resulting in a 3.09% reduction in $di_g/dt_{,max}$, after 82 hours of continuous buck converter operation. The DPT results show the advantages of the proposed $di_g/dt_{,max}$ over the conventional GOD parameters, including low sensitivity to T_j, V_{ds} and I_{ds}. It also eliminates the need to increase drive resistance to reduce switching speed. In addition, the PCB Rogowski coil enables non-contact, real-time measurement of di_g/dt, and has the advantage of easy integration into the drive circuit. The proposed CM technique improves the SiC MOSFET reliability and contributes to developing of more durable and efficient power electronic systems. In the future, the design of the PCB Rogowski coil will continue to be explored to further improve its CM accuracy. At the same time, it will investigate direct measurement of injected charge density or oxide trap charge increment method.

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