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Development and Optimization of Three-DOF Modulation for Single-Stage Matrix AC-DC Converters Based on Real-Time Calculation

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***Abstract*—As the global energy transition accelerates and smart grids develop, solid-state transformers (SSTs) are becoming essential components of the modern power grid. The single-stage matrix (SSM) AC-DC converter, recognized for its simple structure, fewer components, and ease of control, plays a crucial role in SSTs. However, maintaining high efficiency across the operating range is difficult due to the broad input voltage range and the considerable influence of half-bridge capacitors on inductor current. Therefore, this paper establishes a three-degree-of-freedom (DOF) asymmetric modulation method based on traditional extended phase-shifting by introducing a new DOF into the full-bridge structure on the DC side of the SSM AC-DC converter. Through mode classification and modeling of the three-DOF modulation, along with various methods such as single-objective and multi-objective optimization and considerations of the impact of half-bridge capacitors on inductor current, an optimized modulation trajectory (OMT) is developed. OMT ensures that the peak-to-peak value of the inductor current is minimized, all power switches achieve zero-voltage switching, and it is capable of real-time calculation. An experimental platform is established to validate the proposed OMT. The results indicate that, compared to recent work, the OMT improves the converter's efficiency by a maximum of 3.96%, thereby confirming the method's effectiveness and accuracy.**

***Index Terms*—The single-stage matrix AC-DC converter, modulation trajectory, efficiency, real-time calculation**

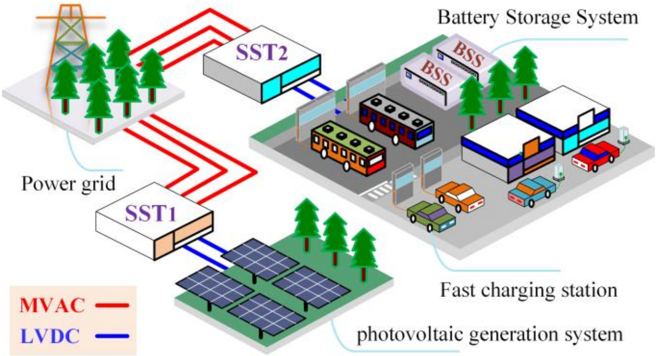

Fig. 1 Solid-state transformers (SSTs) have typical applications in new power grids, where SST1 connects photovoltaic generation systems to the grid, and SST2 links fast charging stations to the grid.

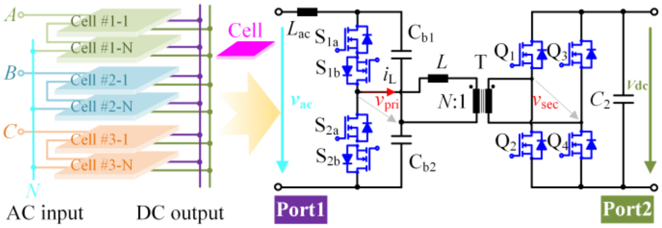

Fig. 2 The new SST uses the SSM AC-DC converter as its fundamental cell. In a three-phase input system, the input for each phase is formed by multiple SSM converters connected in series. The outputs of all SSM converters are then connected in parallel.

I. INTRODUCTION

In recent years, in pursuit of the goals of "carbon peaking" and "carbon neutrality" to reduce carbon emissions, distributed generation (DG) sources such as photovoltaic power and fuel cells, along with energy storage systems including electric vehicles and battery storage, have experienced rapid growth in both number and scale [1-2]. However, since these systems inherently feature DC input/output rather than AC, the use of AC-DC converters is essential for facilitate energy conversion [3]. The AC-DC solid-state transformer (SST), by integrating power electronic converters and high-frequency transformers, not only provides an appropriate voltage level interface between the AC grid and DC loads/DG sources but also enable flexible management of power flows between ports [4-5], as illustrated in Fig. 1. Accordingly, the robust development of the SST is a critical pathway to support the advancement of renewable energy.

Fig. 2 illustrates an advanced design of a SST utilizing the single-stage matrix (SSM) AC-DC converter. This architecture achieves high efficiency and power density through an input series and output parallel strategy [6]. The SSM is central to this design, integrating a half-bridge on the AC side and a full-bridge on the DC side, characterized by its simple structure, fewer components, and ease of control [6-11]. In [9], a high-performance SST using the resonant SSM converter handles AC inputs up to 6.6 kV, outputs 400 V DC while maintaining a transmission power of 25 kW, and achieves a

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power density of 24.5 W/in^3 with a peak efficiency of 97.5%. In [10], a 2.2 kW SSM prototype constructed using advanced silicon carbide (SiC) semiconductor materials achieves an efficiency of 96.1% and a power density of 2.49 kW/L. In [11], a 3.3 kW electric vehicle charger based on the SSM converter maintains a peak efficiency of 97.8% and achieves a high power density of 3.9 kW/L.

The SSM AC-DC converter, due to its inherent bridge structure, faces challenges similar to those encountered by dual active bridge (DAB) DC-DC converters [12-16]. Specifically, under the conventional single-phase-shift (SPS) modulation scheme, these converters are prone to losing their zero-voltage switching (ZVS) characteristics and generating a large amount of reactive power over a wide voltage range [6], [9-16]. To address this issue, an optimized modulation scheme based on a two-degree-of-freedom (DOF) extended phase-shift (EPS) modulation scheme is proposed in [10], which achieves ZVS across the entire operational range and enhances the efficiency of the SSM converter. In [17], a modulation scheme that can achieve a ZVS or zero-current switching (ZCS) operation in all switches is developed. In [18], a fixed-frequency EPS modulation method is proposed for power factor correction that eliminates the need for an internal current control loop and allows real-time calculation of two-DOF without a lookup table. However, these methods still encounter two challenges: first, they cannot simultaneously minimize conduction and switching lossesr; second, in the AC-side half-bridge configuration, the proposed optimization schemes often struggle to align with theoretical expectations due to the neglect of the dynamic impact of capacitors on the inductor current. To elaborate, during the parameter design process of the SSM AC-DC converter, smaller bridge arm capacitors are typically selected to meet power factor requirements. However, these smaller capacitors can lead to significant fluctuations in the inductor current, thereby affecting the stability of the carefully designed modulation schemes aimed at achieving ZVS, ultimately reducing the efficiency of the converter.

In previous studies, the authors conducted extensive research on modulation schemes for DAB converters [14-16]. The proposed five-DOF scheme reduces conduction and switching losses significantly by introducing duty and phase shift ratios independently in the primary and secondary full-bridge configurations [16]. Therefore, to maximize efficiency across the entire operating range of the SSM AC-DC converter, this paper proposes a three-DOF modulation scheme based on research on DAB converters. This scheme introduces the duty cycle of the power switches as a new DOF in the DC-side full-bridge structure, thereby expanding the optimization space based on the EPS modulation scheme. Then, to address the impact of half-bridge arm capacitors on the inductor current, this paper aims to develop a simple model to quantify their effects on current. Ultimately, these effects will be integrated into the three-DOF modulation scheme, ensuring that the theoretical analysis aligns with practical operations and resulting in a comprehensive solution. Comprehensively, the main contributions of this paper are as follows: 1) Asymmetric modulation has been successfully integrated into the SSM AC-DC converter for the first time, resulting in a new three-DOF modulation method, along with the mode classification, analysis, and modeling; 2) The proposed optimized modulation technique (OMT), along with its simple analytical expressions, enables real-time computation while ensuring that both conduction and switching losses of the inductor current are minimized under the influence of fluctuations in half-bridge arm capacitance.This approach fully leverages the potential of the SSM AC-DC converter, ensuring high efficiency across the entire operating range.

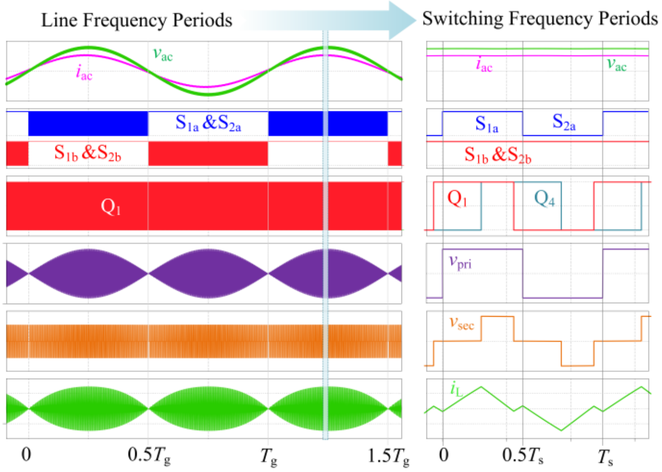


Fig. 3 The typical waveforms of the SSM AC-DC converter under EPS modulation scheme. From left to right, the waveforms corresponding to the line frequency cycle and the switching frequency cycle. From top to bottom, the waveforms include: input voltage (v_{ac}), input current (i_{ac}), driving signals for the power switch in the half-bridge converter on the AC side, driving signals for the switch in the full-bridge converter on the DC side, voltages on the primary and secondary sides of the high-frequency transformer (v_{pri} and v_{sec}), and the inductor current (i_L).

The rest of the paper is organized as follows, Section II analyzes and discusses the three-DOF modulation scheme, modeling two of its modes. Then, Section III focus on optimizing this scheme based on single-objective and multi-objective. Section IV examines the impact of capacitance on the fluctuations of the inductor current, complete simple modeling, and offer compensation for optimized modulation, ultimately proposing to the OMT scheme. Section V verifies the theoretical correctness by setting up an experimental platform. Finally, conclusions are drawn in Section VI.

II. ANALYSIS AND MODELING OF THERE-DOF MODULATION TECHNIQUES

A. *Operating principle under EPS modulation scheme*

Fig. 2 shows the structure of the SSM AC-DC converter, each equipped with four power switches on both its AC primary and DC secondary sides. The transformer turn ratio is set to N:1, and the switching frequency is set at f_s, and the corresponding switching cycle is T_s. The input voltage and current operate at a link frequency f_L, and the cycle of the link frequency is T_L.

Fig. 3 illustrates the typical waveform of the SSM under the EPS modulation scheme. During the positive half-cycle of the link frequency, the power switches S_{1a} and S_{2a} operate in a complementary manner. Meanwhile, the power switches S_{1b} and S_{2b} remain in a normally open state. The power switches of the full-bridge converter on the DC side operate with a 50% duty cycle, with Q_1 and Q_2 conducting complementarily, as do Q_3 and Q_4. In the EPS, the phase shift between the power switch S_{1a} and Q_1, often referred to as the external phase shift, plays a crucial role in active power transfer. To further optimize the steady-state performance of the SSM AC-DC converter, the EPS introduces a phase shift between Q_1 and Q_4 in the full bridge [12]. This additional DOF helps converter to regulate steady-state performance.

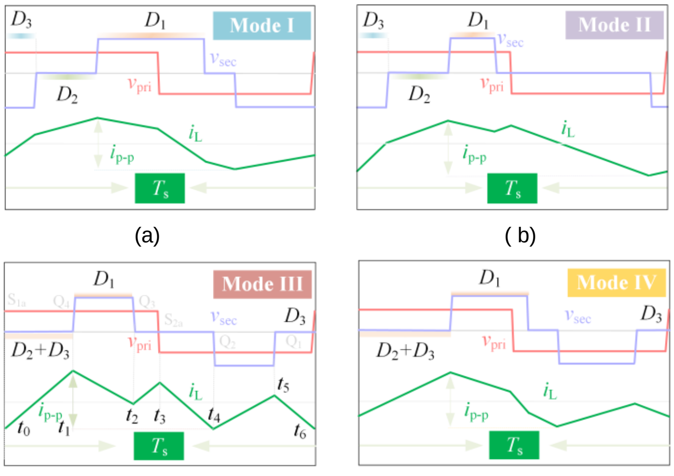
B. Construction and Classification of the Three-DOF

The AC side of the half-bridge power switches in an SSM AC-DC converter can operate in two ways: 1) With switches toggling at a 50% duty cycle; and 2) With switches operating in any configuration, provided that the upper and lower bridge arms switch complementarily. For example, power switch S_{1a} may have a 30% duty cycle while S_{2a} has 70%, with the DC bias managed by the bridge capacitors. While this flexibility enhances optimization potential, the nonlinearity and complex coupling effects hinder the SSM AC-DC converter's ability to achieve an analytical modulation trajectory [19]. Consequently, this paper does not delve deeper into this way.

The DC side of the full-bridge power switches in an SSM AC-DC converter not only allows for an internal phase shift but also permits power switches to operate with non-50% duty cycles, resulting in two-DOF. Specifically, Q_2 and Q_4 have the same conduction time, with a duty cycle of less than or equal to 0.5, defined as D_1, while Q_1 and Q_3 have the same conduction time, with a duty cycle of greater than or equal to 0.5, defined as D_2. Combined with the external phase shift D_3, the SSM AC-DC converter has three completely independent DOFs. Notably, D_1 is introduced primarily because, under asymmetric control, the switching losses of the SSM AC-DC converter are reduced [15-16]. The resulting three-DOF modulation is fundamentally similar to the EPS shown in Fig. 3, with the only difference being the addition of an extra-DOF, which provides greater optimization potential.

To analyze the newly proposed three-DOF modulation scheme, the first step is to categorize the modes. To facilitate positive power transfer, the midpoint of the high level of v_{pri} should occur before the midpoint of the high level of v_{sec}. Taking the trigger time of switch S_{1a} as a reference, this configuration can generate four effective modes under the three-DOF modulation scheme, as shown in Fig. 4. When $D_3 >$ 0, modes I and II can be realized, while modes III and IV can be achieved when $D_3 < 0$.

In the second step, we will analyze the four modes. To maximize power output within the three-DOF modulation scheme, D_1 and D_3 need to operate as close to their boundary conditions as possible. However, due to the timing limitations of each mode, only Mode I successfully achieves this goal. Specifically, in Modes II and III, to satisfy the boundary condition $D_2 + D_3 + D_1 \leq 0.5$, D_1 must be less than 0.5. In Mode IV, $D_3 \leq 0$, which also prevents D_3 from reaching its maximum boundary. Mode III is characterized by an inductor current waveform that approximates a triangular shape, which is particularly advantageous under low-power conditions, as it optimally balances conduction and switching losses [16]. Accordingly, analysis suggests that Mode III is suitable for low-power conditions, while Mode I is more appropriate for high-power conditions. Modes II and III do not present significant functional or performance advantages; thus, this paper will not explore these two modes further.



(a) (b)

(c) (d)

Fig. 4 Classification of modes under the three-DOF asymmetric method: (a) Mode I, characterized by the conditions $D_3 \geqslant 0$, $D_1 + D_2 \leqslant 0.5$, and $D_2 + D_3 + D_1 \geqslant 0.5$; (b) Mode II, characterized by the conditions $D_3 \geqslant 0$, and $D_2 + D_3 + D_1 \leqslant 0.5$; (c) Mode III, characterized by the conditions $D_3 \leqslant 0$, $D_2 + D_3 + D_1 \leqslant 0.5$, and $1 - D_1 - D_3 \geqslant 0.5$; (d) Mode IV, characterized by the conditions $D_3 \leqslant 0$, and $D_2 + D_3 + D_1 \geqslant 0.5$.

The voltage conversion ratio M of the SSM converter, as well as reference values for current and power transfer, are defined:

$$M=\frac{\left|v_{\mathrm{ac\_max}}\right|}{2NV_2};I_{\mathrm{bv}}=\frac{NV_2}{2f_sL};P_{\mathrm{bv}}=\frac{\left(NV_2\right)^2}{2f_sL} \tag{1}$$

In Eq. (1), $v_{\mathrm{ac\_max}}$ represents the maximum value of the input AC voltage, and L denotes the inductance. By deriving voltage and current equations at various switching times, and applying the principle that the average inductor current over one cycle is zero, specific expressions for the steady-state characteristics of each mode can be obtained [19]. These results can be normalized and summarized in Table I.

Mode I maximizes power transfer with a normalized boundary of $M/4$, representing the maximum power transmitable under both SPS and EPS modulation schemes [12]. This shows that the three-DOF modulation scheme does not reduce the power transmission capability of the SSM AC-DC converter. In Mode III, the expression for power transmission is simpler, depending only on D_1 and D_3, indicating that changes in D_2 do not affect power transfer.

There are two key reasons for focusing on the peak-to-peak current $I_{p\text{-}p}(\boldsymbol{D})'$ in Table I: 1) The peak-to-peak value indicates twice the current stress, which is positively correlated with conduction losses [15-16]; and 2) Subtracting the minimum current from the maximum eliminates strong coupling effects between different DOFs, simplifying the expression for further optimization [19]. However, uncertainties related to $\boldsymbol{D}$ can lead to variations in the maximum and minimum current positions. For instance, in Mode III, during the positive half-cycle of the line frequency, the maximum current may occur at switches Q_1, Q_4, and S_{2a}, while the minimum may be at Q_2, Q_3, and S_{1a}. This results in nine potential scenarios; however, some of them are contradictory. For example, if the maximum current occurs while S_1 is conducting, the condition $D_2 + 2D_3 \leq 0$ must hold. However, the power transfer expression requires that $D_2 + 2D_3$ be greater than zero to transmit positive power, creating a contradiction. Ultimately, as shown in Table I, four feasible scenarios were identified.

TABLE I
THE NORMALIZED EXPRESSIONS FOR POWER, BOUNDARY, AND PEAK-TO-PEAK INDUCTOR CURRENT UNDER VARIOUS MODES

	Output power	Boundary	Inductor Peak-to-Peak Current
Mode I	$P' = -\frac{M}{2}\left(4D_1^2 + 4D_1D_2 - 4D_1 + 4D_2^2 + 8D_2D_3 - 4D_2 + 8D_3^2 - 4D_3 + 1\right)$	$\left(0, \frac{M}{4}\right]$	$I'_{\text{p-p}} = 2D_2M - 2D_1M + 4D_3M + 2D_1$
Mode III	$P' = 2MD_1\left(D_2 + 2D_3\right)$	$\left(0, \frac{M}{8}\right]$	$I'_{\text{p-p}} = \begin{cases} I'_{10} = 2M\left(D_2 + D_3\right) \\ I'_{14} = \left(2D_2M - 2D_1M + 4D_3M + 2D_1\right) \\ I'_{30} = M - 2D_1 \\ I'_{34} = 2M\left(D_3 - D_1 + 0.5\right) \end{cases}$

III OPTIMIZATION OF THERE-DOF MODULATION SCHEMES

A. Optimization based on the single objective

First, we establish the optimization equation for minimizing the peak-to-peak value of the inductor current $I_{\text{p-p}}(\boldsymbol{D})'$, as presented in Eq. (2). $P(\boldsymbol{D})'$ represents the expression for the normalized transmission power, P_*' is the normalized value of the given power, and $h_i(\boldsymbol{D})$ denotes the inequality constraints imposed by the modulation DOFs.

$$\begin{aligned} &\text{Minimize} \quad I_{\text{p-p}}\left(\boldsymbol{D}\right)' \\ &\text{Subject to} \quad P\left(\boldsymbol{D}\right)' - P_*' = 0 \\ &\qquad\qquad h_i\left(\boldsymbol{D}\right) \le 0 \ \left(i = 1, 2, \dots, n\right) \end{aligned} \tag{2}$$

Using the Karush-Kuhn-Tucker (KKT) conditions, Eq. (2) can be solved. By using MATLAB for solving and filtering, the single-objective optimization (SOO) modulation trajectories are obtained, as shown in Table II.

As shown in Table II, the SOO is divided into four segments. The first three segments operate in Mode III, with the maximum inductor current occurring at time t_1 and the minimum at time t_4, while the final segment operates in Mode I. As shown in Table II, the optimization solutions for the first and fourth segments of the SOO satisfy $D_1 + D_2 = 0.5$, indicating a shift from three-DOF asymmetric modulation to two-DOF symmetric modulation. Additionally, a key feature of the first segment is that the inductor current values at times t_1 and t_3 are equal, as are the current values at times t_0 and t_4.

Assuming that power and input voltage can vary freely, a detailed comparison will be made between the SOO scheme and recent work [10]. Figs 5(a) and (b) illustrate how $I_{\text{p-p}}(\boldsymbol{D})'$ varies with output power at $M = 0.2$ and $M = 0.7$. The proposed SOO consistently demonstrates its advantages, especially under low-power conditions, regardless of changes in M and P. Notably, the method in [10] does not cover the entire transmission power range; its maximum power corresponds to the highest achievable value in Mode III of the SOO scheme.

TABLE II
OPTIMAL SOLUTION UNDER THE SINGLE-OBJECTIVE

Power Range	Optimal solution
$\left(0, P_{\text{b1}}' = \frac{M^2\left(1-M\right)}{2\left(2M-3\right)^2}\right]$	$\begin{cases} D_1 = \frac{M + \sqrt{M^2 - 16P' + 8MP'}}{8 - 4M} \\ D_1 + D_2 = 0.5; D_3 = \frac{\left(M-1\right)D_1}{M} \end{cases}$
$\left(\frac{M\left(1-M\right)}{2\left(2M-3\right)^2}, P_{\text{b2}}' = \frac{M^2\left(1-M\right)}{2\left(M-2\right)^2}\right]$	$\begin{cases} D_1 = \sqrt{\frac{P'}{2\left(1-M\right)}}; D_2 = -3D_3 \\ D_3 = -\frac{\sqrt{2P'\left(1-M\right)}}{2M} \end{cases}$
$\left(\frac{M^2\left(1-M\right)}{2\left(M-2\right)^2}, P_{\text{b3}}' = \frac{M^2\left(1-M\right)}{2}\right]$	$\begin{cases} D_1 = \sqrt{\frac{P'}{2\left(1-M\right)}}; D_2 = \frac{1}{2} - D_1 - D_3 \\ D_3 = \sqrt{\frac{P'}{2M^2\left(1-M\right)}} - \frac{1}{2}; \end{cases}$
$\left[\frac{M^2\left(1-M\right)}{2}, \frac{M}{4}\right]$	$\begin{cases} D_3 = \frac{1}{4} - \frac{1}{4}\sqrt{\frac{\left(M-4P'\right)}{M\left(2M^2-2M+1\right)}} \\ D_2 = \frac{\left(M-1\right)}{2}\left(4D_3-1\right), D_1 + D_2 = 0.5 \end{cases}$

Figs 6(a) and (b) show the switching characteristics of all power switches under the two modulation schemes. In the SOO scheme, only the power switch Q_3 fails to achieve ZVS in certain regions, as indicated by the blank area in Fig. 6(a). The boundaries of the hard-switching (HS) region for Q_3 are defined by P_{b1}' and P_{b3}', corresponding to the initial and final power values of the second and third segment optimization solutions in Mode III, respectively. In contrast, Fig. 6(b) shows that all power switches in the modulation scheme proposed in [10] achieve soft-switching. In summary, in the SOO modulation, both the first and fourth segments minimize the peak-to-peak value of the inductor current while ensuring that all power switches achieve ZVS. However, in the second and third segments, at least one switch cannot achieve ZVS. Therefore, the modulation trajectory between $P_{\text{b1}}'$and P_{b3}' in Mode III may require additional constraints to achieve optimal efficiency.

B. Multi-objective optimization of Mode III

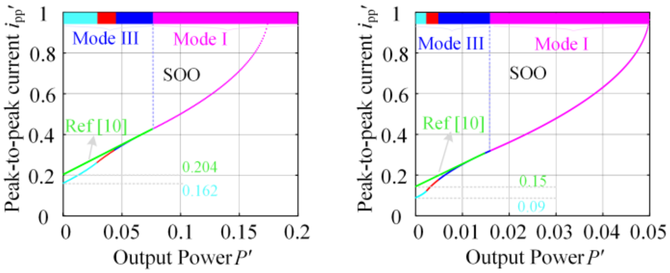
Before optimization, it is essential to ensure that Q_3 can achieve ZVS in Mode III. As shown in Fig. 4(c), the turn-on moment for switch Q_3 corresponds to time t_2, and the expression for current at this moment is as follows:

$$i_2' = -\frac{1}{2}\left(M - 4D_2M - 4D_1M - 4D_3M + 4D_1^2 + 4D_1D_2\right) \tag{3}$$

To achieve ZVS for Q_3, it is necessary for i_2' to be less than 0. From Eq. (3), its expression includes the complex factor $4D_1^2 + 4D_1D_2$. To obtain a simpler analytical solution, the expression for i_2' needs to be simplified. Fortunately, the expression for the turn-on moment of S_{2a} is quite straightforward, as shown:

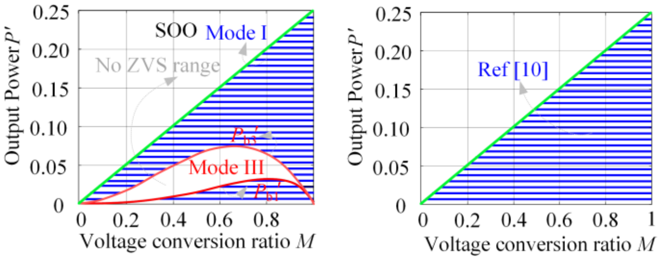
$$i_3' = -\frac{1}{2}\left(4D_1^2 + 4D_1D_2 - M\right) = A \tag{4}$$

Assuming $i_3' = A$, it can be derived from Eq. (4) that $M - 2A =$



(a) (b)

Fig. 5 A comparison of the peak-to-peak value of the inductor current between the SOO and the modulation obtained in [10] under the same conditions. (a) When M = 0.2; (b) When M = 0.7.



(a) (b)

Fig. 6 A comparison of the soft-switching ranges between the SOO and the modulation obtained in [10] under the same conditions. (a) SOO modulation scheme; (b) modulation scheme proposed in [10].

$4D_1^2 + 4D_1D_2$. Substituting $M - 2A$ into Eq. (3) yields

$$M - 2D_2M - 2D_1M - 2D_3M - A > 0 \tag{5}$$

By substituting Eq. (5) into Eq. (2) and applying the KKT algorithm again, the optimized modulation trajectory for Mode III under multi-objective constraints is obtained. To eliminate the assumed variable A from the optimization trajectory, set i_2' = 0. Consequently, the modulation trajectory can be derived

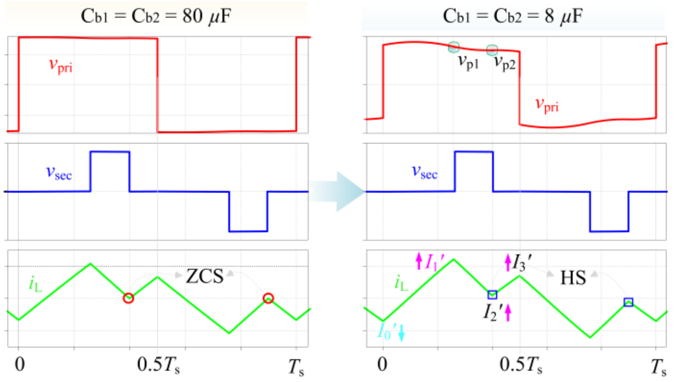
$$\begin{cases} D_1 = \sqrt{\dfrac{P'}{2(1-M)}}; P' \in \left(P_{b1}', P_{b3}'\right] \\ D_1 + D_2 = \dfrac{1}{2}; D_3 = \dfrac{P'}{4D_1M} - \dfrac{D_2}{2} \end{cases} \tag{6}$$

To validate the performance of the modulation trajectory derived from Eq. (6), it was compared with the previously proposed SOO. The results show that the peak-to-peak values from both SOO and Eq. (6) are essentially identical, indicating that a minimal peak-to-peak value can still be achieved even with the added ZVS constraints. Regarding soft-switching implementation, Eq. (6) ensures that all power switches in the SSM AC-DC converter achieve soft-switching, with Q_2 and Q_3 turning on with ZVS while the remaining switches also achieve ZVS. These findings confirm the effectiveness of the modulation trajectory obtained from Eq. (6).

Finally, substituting the modulation trajectory between $P_{b1}'$and P_{b3}' in Table II with Eq. (6) generates a new modulation trajectory for the entire operating domain, referred to as the multi-objective optimization (MOO) modulation scheme.

VI CONSIDERING THE IMPACT OF HALF-BRIDGE ARM CAPACITORS ON INDUCTOR CURRENT

The above derivation process is based on the ideal conditions and does not consider the effects of bridge arm capacitors in the AC side half-bridge structure of the SSM converter. Typically, these capacitors are chosen assuming that reactive power constitutes 5% of the active power [21]. This assumption leads to voltage fluctuations at the output, which can cause deviations in the inductor current from what was theoretically expected. For example, as shown in Fig. (7), using an 80 μF capacitor stabilizes the voltage but results in a power factor below 0.99, not meeting design standards. Conversely, a smaller 8 μF capacitor maintains a good power factor but causes significant voltage fluctuations. This forces the power switch to perform hard switching, increasing losses and reducing the efficiency of the modulation strategy. Thus, it's important to consider the impact of half-bridge capacitors on output voltage when optimizing the system.



(a) (b)

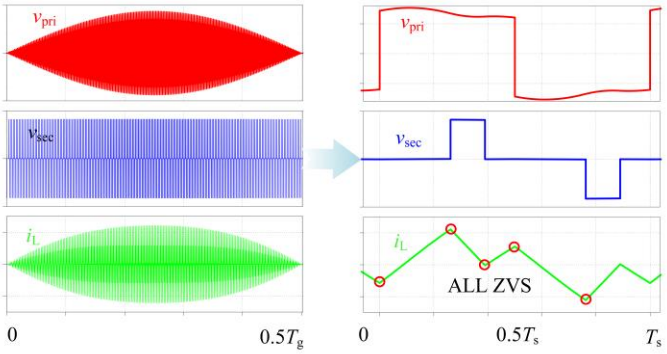
Fig. 7 Under the MOO modulation scheme, a comparison of typical waveforms with different capacitance values for the bridge arm capacitors of the input half-bridge. The operating conditions are as follows: v_{ac} = 220 VAC, v_2 = 200 VDC, L = 32.1 μH, N = 1.287: 1, and P_g = 300 W. (a) $C_{b1} = C_{b2}$ = 80 μF; (b) $C_{b1} = C_{b2}$ = 8 μF.

As shown in Fig. 7(b), the behavior of the current at each power switch moment is consistently influenced by capacitors, with the current always increasing in absolute value. In the MOO modulation, since Q_3 is supposed to turn on at zero current, it experiences the most significant impact. To reset the current I_2 to zero after fluctuations, there are two methods. The first method, which involves altering the rate of change from current I_1 (when Q_4 turns on) to I_2, is complex and unclear. The second method extends the duration D_1 to give the current I_2 enough time to return to zero when Q_3 turns on. This extension is defined as ΔD_1. Thus, the effects of the capacitor on the current I_2 before and after can be described as follows.

$$\begin{cases} 0 = I_1 + \dfrac{0.5|v_{ac}| - NV_2}{f_s L} D_1 \\ 0 = I_1 + \Delta I + \dfrac{0.5|v_{ac}| + \Delta v_p - NV_2}{f_s L}\left(D_1 + \Delta D_1\right) \end{cases} \tag{7}$$

In Eq. (7), ΔI is the fluctuation in current at I_1, and Δv_p represents the voltage fluctuation, calculated as the difference between v_{p1} and v_{p2}. v_{p1} is the output voltage when switch Q_4 is on, and v_{p2} is the voltage when switch Q_3 is on. Given that D_1 is usually small, as mentioned in Eq. (6), calculations can be simplified by assuming $\Delta v_p = 0$. By normalizing and solving Eq. (7), it is possible to obtain

$$\Delta D_1 = \frac{\Delta I'}{2(1-M)} \tag{8}$$



(a) (b)

Fig. 8 Typical waveform after adding compensation, with parameters consistent with those in Fig. 7.

In Eq. (8), $\Delta I'$ represents the normalized value of ΔI. To solve for ΔD_1, specific current fluctuations must be determined. However, calculating ΔI is complex, involving multiple factors such as arm capacitance, inductance, switching frequency, transformer ratio, and transmission power, requiring iterative calculations. For simplicity, this paper assumes that ΔI remains within 10% of I_1 and is substituted into Eq. (8) to obtain

$$\Delta D_1 = 0.1D_1 \tag{9}$$

Substituting Eq. (9) into Eq. (6), further obtain

$$D_1 = 1.1\sqrt{\frac{P'}{2(1-M)}} \tag{10}$$

Therefore, combining Table II and Eq.(10), we have formed the final optimized modulation trajectory (OMT). From Fig. 8, it is evident that after adding compensation, all power switches achieve ZVS, and their RMS values are also kept very low.

V. EXPERIMENTAL TEST

To thoroughly explore and validate the effectiveness and feasibility of the proposed OMT modulation scheme, a SSM AC-DC converter is constructed, as shown in Fig. 9. The input and output parameters and hardware design of the converter are consistent with the parameters obtained in Fig. 7, and the bridge arm capacitance is selected as 8 μF.

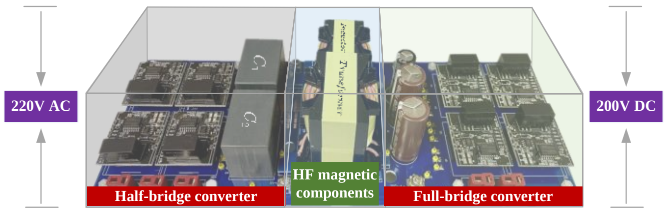


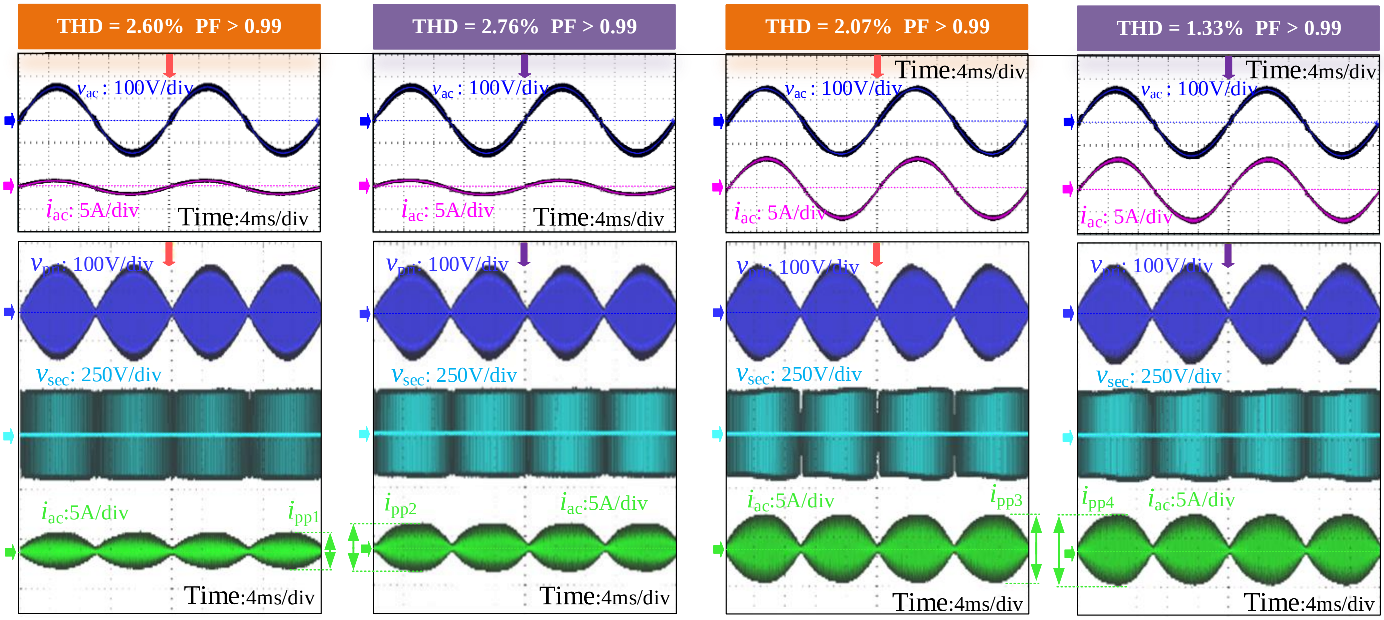
Fig. 9 Experimental prototype of the SSM AC-DCconverter. The input is 220Vac, and the output is 200V dc, with a maximum power of 500W. The switching frequency is set at 20kHz, L = 32.1 μH, N = 1.287: 1, and C_{b1} = C_{b2} = 8 μF.

Fig. 10 displays the typical waveforms of the SSM AC-DC converter under OTM and the method proposed in [10], with average output powers of P_g = 100W and P_g = 500W at the link frequency cycle. From top to bottom, the waveforms shown are the input voltage v_{ac}, input current i_{ac}, primary and secondary side bridge output voltages v_{pri} and v_{sec}, and the inductor current i_L. In all four cases, the THD of the AC side current is less than 3%, and the power factor is greater than 0.99, indicating high-quality outputs from both OTM scheme and the work in [10]. Comparatively, under similar conditions, Fig. 10(a) shows that the peak-to-peak inductor current in the OTM scheme is less than that in [10]. As power increases, the peak-to-peak differences in inductor currents between Figs. 11(c) and (d) diminish, yet the values from the OTM scheme consistently remain slightly smaller.

Fig.11 presents the typical waveforms corresponding to the switching cycles at the peak AC voltage for the four scenarios discussed in Fig. 10. From top to bottom, the waveforms represent the output voltage v_{pri} of the AC-side half-bridge converter, theoutput voltage v_{sec} of the DC full-bridge converter, and the inductor current i_L. A comparison between Figs. 11(a) and (b) reveals that under the OTM scheme, the inductor RMS current measures 6.73 A, with a peak-to-peak value of 23.2 A. In contrast, the method from [10] results in an inductor RMS current of 8.96 A and a peak-to-peak value of 35.2 A. Clearly, The OTM scheme offers significant advantages in both RMS and peak-to-peak values. Furthermore, under the same conditions, all power switches in the OTM scheme achieve ZVS, whereas in [10], two power switches, S_{1a} and S_{2a} on the AC-side half-bridge, fail to achieve ZVS due to unaccounted fluctuations from capacitor voltages, resulting in substantial switching losses. To further observe the behavior of the switches during the dead time, Figs 12(a) and (b) display the gate drive signal v_{gs} and the voltage v_{ds} across power switch S_{1a} for the two modulation methods. It is evident that under the OTM scheme, the current flowing through S_{1a} is sufficiently large, allowing v_{ds} to completely drop to zero before the current begins to rise, thus achieving ZVS. In contrast, in [10], the current direction through S_{1a} is reversed, causing the energy stored in the parasitic capacitance to dissipate as losses, as reflected in the significant overlap between $v_{gs.}$

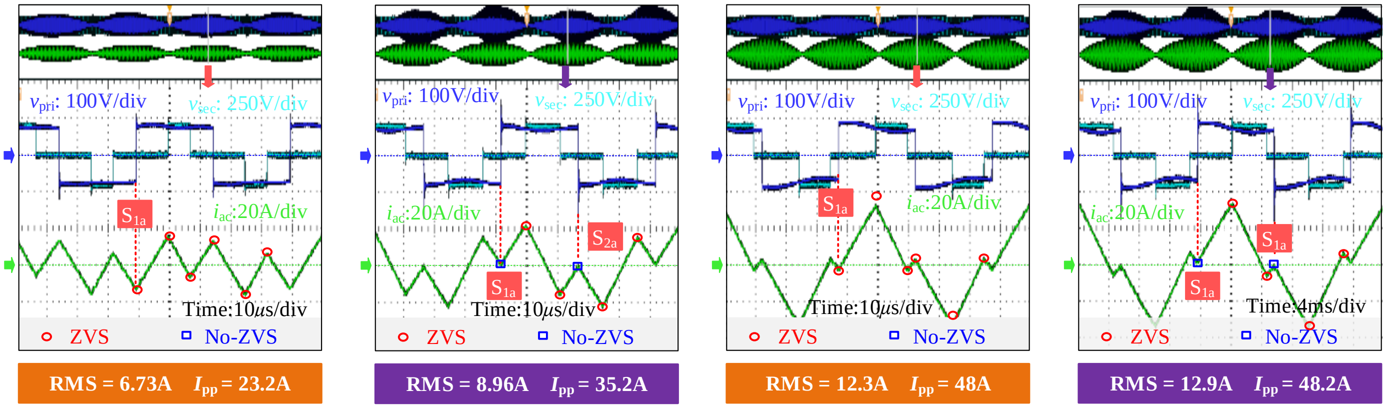
Next, in comparing Figs 11(c) and (d), it is observed that under the OTM scheme, the inductor RMS current is 12.4 A, with a peak-to-peak value of 48 A. In contrast, the method from [10] results in an inductor RMS current of 12.9 A and a peak-to-peak value of 48.2 A. The differences between these results are minimal, supporting the earlier theoretical analysis which suggested that under light load conditions, OTM has a more pronounced advantage in peak-to-peak values, an advantage that diminishes as the power increases. Additionally, all power switches in the OTM scheme continue to achieve ZVS, while two power switches in [10] still fail to achieve ZVS. Figs 12(a) and (b) further illustrate the switching behavior of S_{1a} during the dead time for both modulation schemes. These observations confirm that under the OTM modulation, power switch S_{1a} consistently achieves ZVS. Conversely, under the modulation method from [10], power switch S_{1a} experiences hard switching. This validation not only underscores the effectiveness of the OTM scheme but also confirms the correctness of the proposed method.

Finally, Fig. 13 compares the efficiency of the SSM AC-DC converter under the OTM scheme and the method from [10]. D Efficiency measurements were taken at 50 W intervals, assessing both input and output. As depicted, the OTM scheme consistently outperforms the method from [10], particularly under light load conditions, with a maximum efficiency improvement of 3.96%. Even at higher loads (500 W), OTM maintains an efficiency advantage of approximately 0.5%.



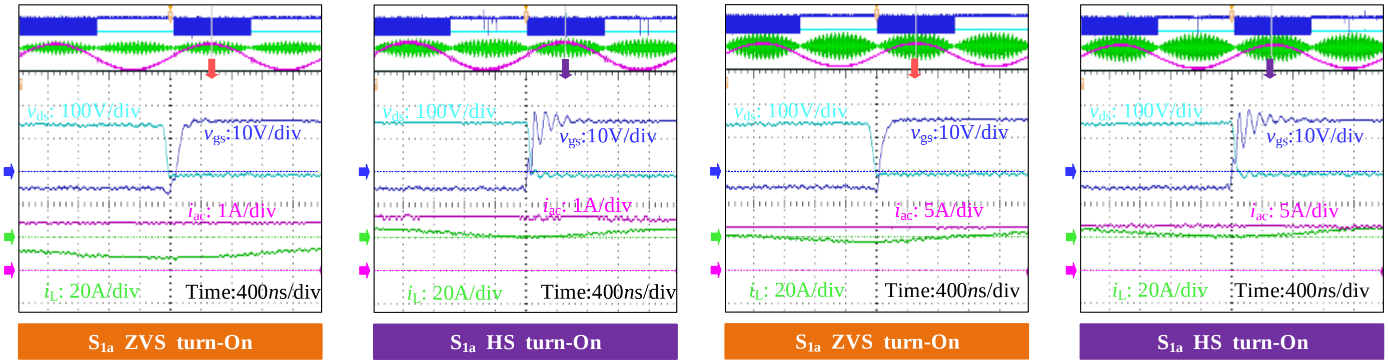
(a) (b) (c) (d)

Fig. 10. Comparison of waveforms for the link frequency cycle at P = 100W and P = 500W using our proposed OTM scheme and the optimized modulation scheme from [10]. (a) OTM scheme at P = 100W; (b) Optimized modulation scheme from [1] at P = 100W; (c) OTM scheme at P = 500W; (b) Optimized modulation scheme from [1] at P = 500W.



(a) (b) (c) (d)

Fig. 11 Comparison of waveforms the power switch waveforms at peak input voltage for an average link frequency cycle at P = 100W and P = 500W using our proposed OTM scheme and the optimized modulation scheme from [10]. (a) OTM scheme at P = 100W; (b) Optimized modulation scheme from [10] at P = 100W; (c) OTM scheme at P = 500W; (b) Optimized modulation scheme from [10] at P = 500W.



(a) (b) (c) (d)

Fig. 12. Comparison of the switching behavior of power switch S_{1a} under different conditions. (a) OTM scheme at P = 100W; (b) Optimized modulation scheme from [10] at P = 100W; (c) OTM scheme at P = 500W; (b) Optimized modulation scheme from [10] at P = 500W.

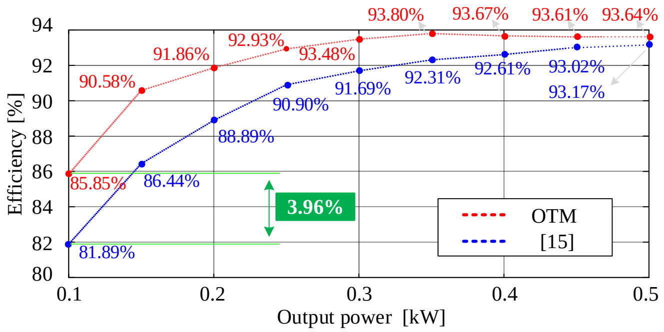


Fig. 13 Efficiency comparison between the OTM and the work presented in [1].

VI. CONCLUSION

To address the issue of low efficiency across the entire operating range of the solid-state transformer's critical module, the SBM converter, due to significant fluctuations in input voltage and the impact of bridge arm capacitance on inductor current, this paper innovatively proposes a three-DOF asymmetric modulation scheme. This approach introduces a new degree of freedom by allowing the power switches in the DC-side full-bridge converter to operate at non-50% duty cycles, thereby enhancing the optimization design space. Building on this foundation, we completed tasks such as mode classification, modeling, and analysis. To derive a modulation strategy that is optimal, straightforward, and capable of real-time operation, we sequentially employed single-objective optimization, multi-objective optimization, and considerations of the influence of capacitor voltage on inductor current, ultimately proposing the OTM modulation scheme. Finally, we constructed an SBM prototype to conduct experimental validation. Compared to recent works, our proposed scheme achieves a maximum efficiency improvement of 3.96%, and even under heavy load conditions, the efficiency still increases by 0.5%.

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