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Photonic logic tensor computing beyond Tbit/s per core

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The soaring demand for computing resources has spurred great interest in photonic computing with higher speed and larger computing capacity. Photonic logic gates are of crucial importance due to the fundamental role of Boolean logic in modern digital computing systems. However, most photonic logic schemes struggle to exhibit the capability of massively parallel processing and flexible reconfiguration, owing to weak and fixed nonlinearity in optical elements. Here, we propose a photonic logic tensor computing architecture for the first time and fabricate the photonic universal logic tensor core (PULTC) with a parallel logic computing capacity beyond Tbit/s. Ten wavelength channels and four spatial channels are designed in the PULTC, where the logic computing speed in each channel can reach 50 Gbit/s. After the nonlinear mapping of microring modulators, arbitrary logic operations can be achieved by configuring the Mach–Zehnder interferometer mesh. We further develop a photonic logic tensor card and demonstrate various functions including cellular automata, image encryption and decryption, and image edge extraction. Our work offers an innovative route for photonic universal logic computing with high-parallel capability and propels the practical applications of photonic logic computing.

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1. INTRODUCTION

The prosperity of the artificial intelligence and communication industry leads to a swift growth in the demand for computing resources. However, electronic circuits are approaching physical limitations, challenging the continuation of Moore's law [1–3]. Boolean logic gates, as the building blocks of modern digital computing systems, require novel ways to break through the constraints of traditional electronic hardware [4–7]. With the maturity of fabrication technology, photonic integrated circuits have shown immense application prospects in computing tasks because light offers satisfactory benefits such as low latency, high parallelism, and large bandwidth [8]. Over the past few decades, a variety of photonic logic circuits have been demonstrated. Recent advances have been proven to outperform the electronic counterpart in both operating speed and power efficiency [9]. Additionally, some highly innovative methods previously demonstrated by discrete optical components, such as frequency-domain logic [10,11] and multi-valued logic [12], offer new opportunities for compact, ultra-fast, and ultra-low-energy integrated logic implementations. However, the nonlinear requirement in logic operations makes it difficult to demonstrate massively parallel processing and flexible reconfiguration.

State-of-the-art photonic logic can be categorized into all-optical (AO) and electronic–optical (EO) methods. Typically, the AO methods exploit photonic nonlinear elements such as photonic crystals [13,14], silicon microring resonators [15,16], and plasmonic nanostructures [17,18] to execute logic operations, where parallel and reconfigurable logic is difficult to implement, restricted by weak and fixed optical nonlinearity. The EO methods leverage EO modulators to load electrical binary signals onto optical carriers and design specific optical circuits to achieve logic functions [19–23]. Despite the exemption of optical nonlinearity, the fixed optical structures hinder the reconfigurability of logic

operations. And the logic parallelism has been explored with a limited number of multiplexed wavelength channels [9,24,25], which cannot fundamentally expand the computing capacity.

High parallelism is an inherent key advantage of photonic computing. Multiple dimensions of light, such as wavelength [26,27], mode [28,29], and even ratio frequency [30], have been leveraged to greatly expand the photonic linear computing capacity. User-defined functions can be easily achieved by configuring relevant thermal electrodes [31,32] or phase change materials [33,34] in the linear networks. Limited by the nonlinear properties, it is still a big challenge to take full advantage of photonic parallelism and flexible reconfiguration capability in optical logic computing.

In this paper, we present a photonic logic tensor computing architecture that enables parallel processing of logic functions for the first time. By employing the EO nonlinearity of the microring modulators (MRMs), the electrical logic signals are nonlinearly mapped into a higher-dimensional vector space. Then, arbitrary logic operations can be directly achieved through a linear transformation of the following Mach–Zehnder interferometer (MZI) mesh. The narrow bandwidth of MRMs and the broad bandwidth of the MZI mesh make it possible to multiplex massive wavelength channels, thereby performing logic operations in parallel. We fabricate the photonic universal logic tensor core (PULTC) with 10 independent wavelength channels and 4 independent spatial channels, where the EO bandwidth of MRMs is more than 50 GHz and the wavelength transmission bandwidth of the MZI mesh exceeds 80 nm. The total computing capacity exceeds Tbit/s per core. Based on the PULTC, we developed a photonic logic tensor card with peripheral component interconnect express (PCIe) and Ethernet interfaces for practical application scenarios. We further execute various computing tasks such as cellular automata, image encryption and decryption, and image edge extraction. The PULTC fully leverages the advantages of optical parallelism and programming ability, paving the way for large-capacity universal photonic logic computing.

2. RESULTS

A. Principle of PULTC

The novel photonic logic tensor computing architecture is shown in Fig. 1(a), which can support parallel logic computing with multiple input channels. Parallel electrical binary signals are first input into the PULTC. Since two input binary signals will yield four possible combinations, all the output logic signals lie in a four-dimensional vector space. Therefore, it is not feasible to achieve arbitrary logic output through directly running a linear transformation of input Signal A and Signal B. Here, the PULTC first maps the input electrical signals in a two-dimensional vector space to the output optical signals in a four-dimensional vector space by generating two linearly independent signals, i.e., continuous wave (CW) and Logic AB during the modulation process, where Logic AB is a nonlinear mapping process. Arbitrary logic output can be generated by programming the following optical linear network [35,36]. Considering each MRM operates at a certain resonance wavelength, multiple wavelength channels can be processed in parallel by using MRMs. The following optical linear network will execute the same logic functions for all input wavelength channels. We can obtain the corresponding logic results by demultiplexing the wavelength channels. In addition to the wavelength dimension, the spatial dimension can also be utilized to simultaneously execute different logic operations for the same input signals. Parallel processing in both the wavelength and spatial dimensions endows the PULTC with immense computing capacity.

The inner structure of the PULTC is presented in Fig. 1(b), which is composed of a nonlinear mapping region and a linear transformation region. In the nonlinear mapping region, CW with multiple wavelengths is first divided equally into two channels. One channel remains CW, while the other is modulated by a series of MRMs. Here, we regard MRMs as optical switches. When the input electrical signal is Logic 0, the MRM is in the resonant state, and the optical output is Logic 0. When the electrical signal is Logic 1, the MRM is in the non-resonant state, and the optical output is Logic 1. The narrow bandwidth of the resonant peak allows each MRM to modulate one wavelength independently without mutual interference. Thus, the parallel input of electrical Signal A (A_1, A_2, …, A_n) can be loaded into the corresponding wavelength channels (λ_1, λ_2, …, λ_n). The CW and Signal A are then evenly split into two channels, respectively. Among them, one channel of the CW and one channel of Signal A are directed into the cascaded dual-waveguide MRMs. Figure 1(c) illustrates the MRM's modulation process of input electrical Signal B. With the electrical signal applied to the MRM, the CW in the upper waveguide is modulated into Signal B, and Signal A in the lower waveguide undergoes the Logic AND operation with Signal B. Only when both Signal A and Signal B are Logic 1, the optical output of the lower waveguide is Logic 1. The other two channels retain the initial input signals, which output CW and Signal A, respectively. The nonlinear mapping process can be written as

$$E=\begin{bmatrix}A\\B\end{bmatrix}\in S_E=\begin{bmatrix}0&0&1&1\\0&1&0&1\end{bmatrix}\xrightarrow{\text{nonlinear mapping}} I=\begin{bmatrix}CW\\B\\AB\\A\end{bmatrix}\in S_I$$
$$=\begin{bmatrix}1&1&1&1\\0&1&0&1\\0&0&0&1\\0&0&1&1\end{bmatrix}, \tag{1}$$

where E and I represent the input electrical signals and output optical signals of the nonlinear mapping region, and S_E and S_I represent all the possible states of E and I. The full rank of S_I indicates that the input two-dimensional vector plane is mapped to a four-dimensional vector space, enabling the following part to achieve arbitrary logic operations through a linear transformation. Note that this nonlinear mapping method is not limited to two input signals. It can also generate 2^N linearly independent vectors for N-input binary signals, which is discussed in Supplement 1, Section S1. Figure 1(d) shows the linear transformation region composed of m columns of MZIs, where each column can perform 1×4 optical vector multiplication. To achieve this, one column of MZIs needs to adjust both the amplitude ratios and phase differences of the four input signals and then coherently combine them. The amplitude ratios are controlled by the heaters on the inner arms of MZIs, and the phase differences are controlled by the heaters on the outer arms. For one MZI, the output of the lower port can be expressed as

$$O_{\text{down}}=ie^{i\theta}(e^{i\varphi}\cos\theta\, I_{\text{up}}-\sin\theta\, I_{\text{down}}), \tag{2}$$

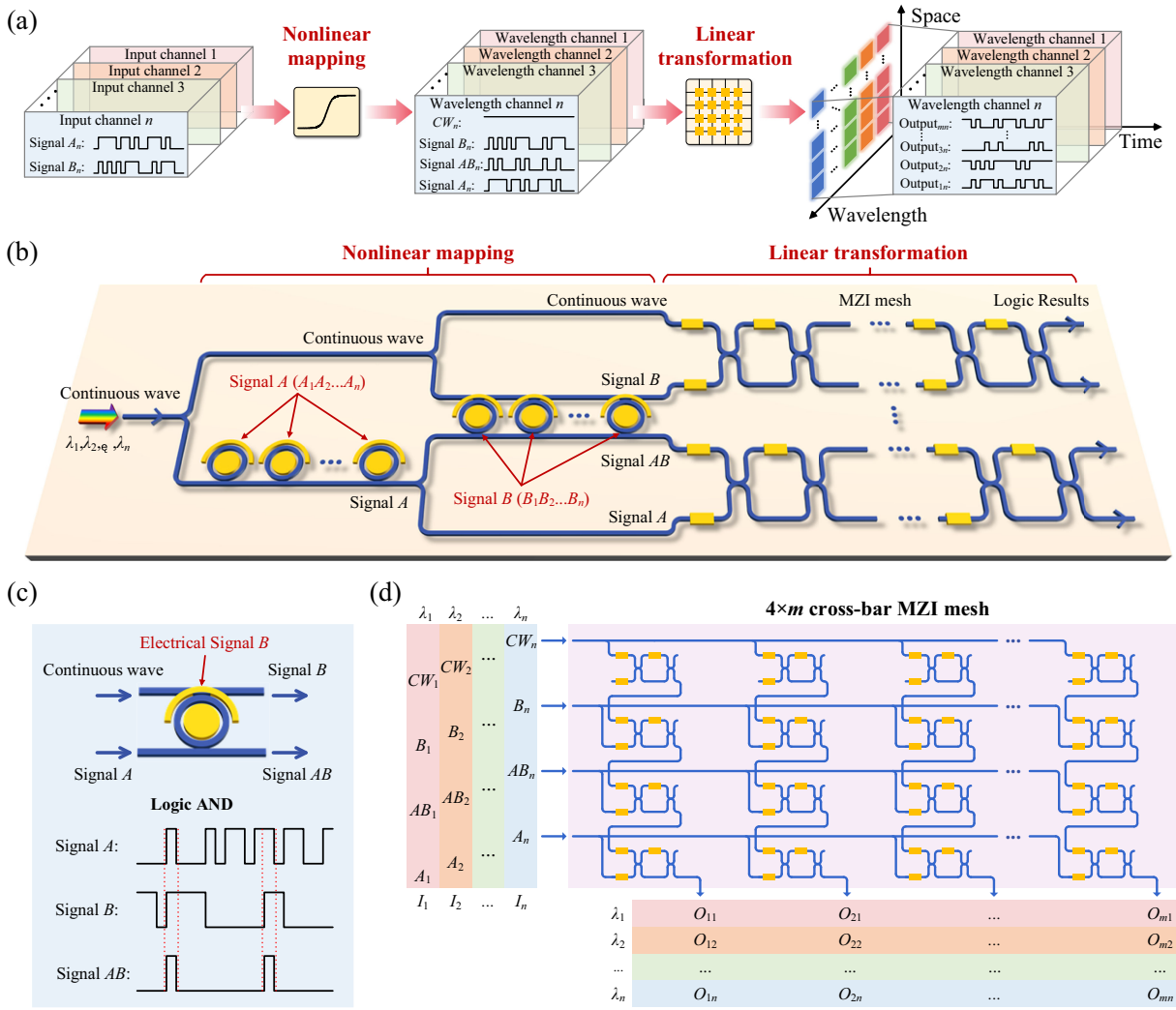

Fig. 1. Operating principle of the PULTC. (a) A sketch map of photonic logic tensor computing. (b) The inner structure of the PULTC, including a nonlinear mapping region and a linear transformation region. (c) The MRM's modulation process of input Signal B. (d) A $4 \times m$ linear transformation matrix realized by the cross-bar MZI mesh. CW, continuous wave.

where φ represents the phase difference of the signals in the input-side outer arms of the MZI (the phase shift in the lower arm is assumed to be zero for simplicity), the phase difference of the signals in the inner arms is 2θ, and I_{up} and I_{down} represent the signals fed into the upper and lower input ports of the MZI, respectively. Therefore, the optical vector multiplication of one column of MZIs is written as

$$O_{\text{MZI}} = \begin{bmatrix} e^{i(\varphi_1+\varphi_2+\varphi_3+\varphi_4+\theta_1+\theta_2+\theta_3+\theta_4)} \cos\theta_1 \cos\theta_2 \cos\theta_3 \cos\theta_4 \\ i e^{i(\varphi_3+\varphi_4+\theta_2+\theta_3+\theta_4)} \sin\theta_2 \cos\theta_3 \cos\theta_4 \\ e^{i(\varphi_4+\theta_3+\theta_4)} \sin\theta_3 \cos\theta_4 \\ -i e^{i\theta_4} \sin\theta_4 \end{bmatrix}^T \times \begin{bmatrix} CW \\ B \\ AB \\ A \end{bmatrix}, \tag{3}$$

where φ_i and θ_i are determined by the phase differences of the input-side outer arms and inner arms in the ith MZI. We can sequentially derive the phase shift differences between the inner and outer arms of each MZI from bottom to top of the target transformation vector. Scaling up, the linear transformation process implemented by m columns of MZIs is expressed as

$$O = \begin{bmatrix} T_1 \\ T_2 \\ \vdots \\ T_m \end{bmatrix} I = \begin{bmatrix} T_1 I \\ T_2 I \\ \vdots \\ T_m I \end{bmatrix}, \tag{4}$$

where T_i represents the 1×4 linear transformation vector of the ith column in the MZI mesh, O represents the output optical logic matrix, and each row of O represents the logic results $(T_i I)$ at the ith output port. Considering that the optical signals I can contain n wavelengths, the tensor transformation process can be given by

$$O = \begin{bmatrix} T_1 \\ T_2 \\ \vdots \\ T_m \end{bmatrix} [I_1, I_2, \ldots, I_n] = \begin{bmatrix} T_1 I_1 & T_1 I_2 & \ldots & T_1 I_n \\ T_2 I_1 & T_2 I_2 & \ldots & T_2 I_n \\ \vdots & \vdots & \ddots & \vdots \\ T_m I_1 & T_m I_2 & \ldots & T_m I_n \end{bmatrix} = \begin{bmatrix} O_{11} & O_{12} & \ldots & O_{1n} \\ O_{21} & O_{22} & \ldots & O_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ O_{m1} & O_{m2} & \ldots & O_{mn} \end{bmatrix}, \tag{5}$$

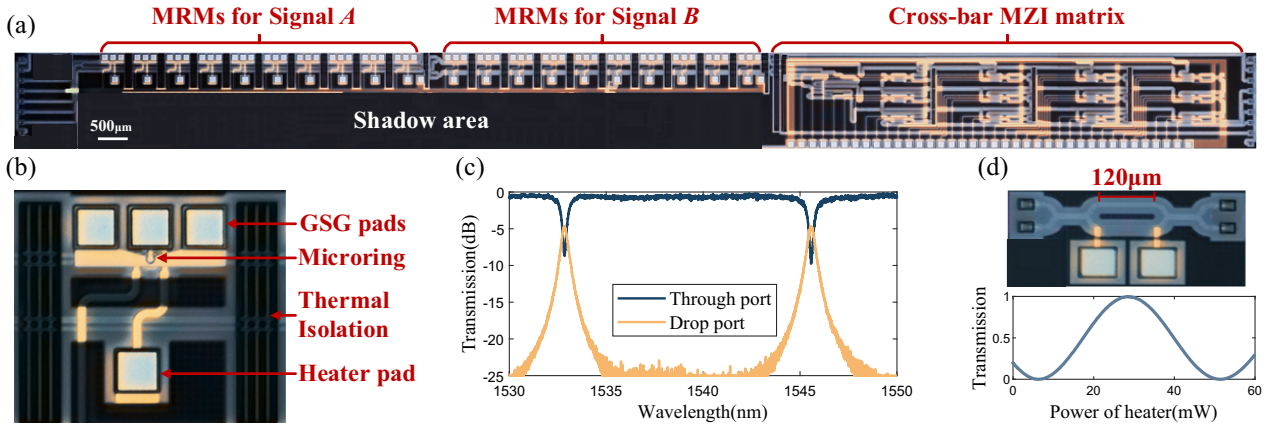

Fig. 2. Fabrication of the PULTC chip. (a) The microscope image of the PULTC chip. (b) A zoomed-in view of the MRM. (c) The MRM's transmission spectra of the through port and the drop port. (d) The imparted phase dependent on the power of the heater in the MZI.

where I_j represents the output signal in the wavelength of λ_j from the nonlinear mapping region, and O_{ij} represents the logic output from ith columns of the MZI mesh at a wavelength of λ_j. By combining the spatial and wavelength dimensions, the PUTLC can execute $m \times n$ logic operations simultaneously, significantly enhancing the computing capacity by $m \times n$ times.

B. Fabrication of the PULTC Chip

The PULTC chip is fabricated on a silicon-on-insulator (SOI) platform with a 220 nm thick silicon and a 2 μm thick buried oxide layer, as shown in Fig. 2(a). Ten carrier-depletion MRMs are utilized to load Signal A and Signal B, respectively, supporting a maximum of 10 parallel logic signals. The MRM component is taken from a process design kit provided by the foundry Chongqing United Microelectronics Center. A zoomed-in image of the MRM is shown in Fig. 2(b). The GSG pads serve as the interface for high-speed electrical signals, and the heater pad is connected to the heater on the MRM, which can adjust the position of the resonance peak. To avoid thermal crosstalk, we add thermal isolation trenches between adjacent MRMs. In Fig. 2(c), we measure the free spectral range (FSR) of the MRM, which is about 13 nm, allowing it to encompass 10 wavelengths within one FSR. We design four columns of MZIs in the PULTC chip corresponding to four parallel output ports. The phase tuning efficiency is measured to be about 20 mW per π phase shift, as shown in Fig. 2(d).

C. Demonstration of PULTC's Functions

We first select one output port in the PULTC to verify the feasibility of logic functions. The MZI mesh is configured to execute the desired linear transformation according to the gradient descent algorithm [31], which is described below:

1. Initialization: the voltages applied to all heaters V_i are set randomly within the range of 3–5 V.
2. Tuning each voltage: set V_i to $V_i + \Delta V$ temporarily. If the cost function $CF(V_i + \Delta V) \geq CF(V_i)$, replace V_i with $V_i + \Delta V$; else, set V_i to $V_i - \Delta V$ temporarily. If the cost function $CF(V_i - \Delta V) \geq CF(V_i)$, replace V_i with $V_i - \Delta V$; else, maintain the original V_i.
3. Repeat Step 2 for all voltages one by one.
4. Repeat Steps 2 and 3 until the CF is converged or reaches the target value.

The CF is defined as

$$CF = \frac{|O^{tgt} \cdot O^{\exp}|}{\|O^{tgt}\| \cdot \|O^{\exp}\|}, \tag{6}$$

where O^{tgt} and $O^{\exp}$ represent the vectors of the target logic and the experimental result, $||$ is to get the absolute value, and $\|\|$ is the two-norm of the vector. All combinations of the two logic input signals (00, 01, 10, and 11) are explored in each iteration. The CF is the correlation between the target and experimental results, ranging from 0 to 1. Figure 3(a) demonstrates the iteration process of the PULTC from a random state to Logic XOR. As the CF gradually approaches 1, the output vector gets closer to the target logic. The PULTC can easily switch to another logic function. By changing the target logic vector O^{tgt}, the output logic will be updated from Logic XOR to Logic XNOR, as shown in Fig. 3(b). Once the voltage settings for each logic operation are obtained, the iteration process is no longer necessary. We can directly switch to the desired logic function by applying the corresponding voltage settings to the MZI mesh. Logic output waveforms of XOR and XNOR in Fig. 3(c) reveal that the PULTC correctly performs logic functions. The extinction ratio (ER) of logic waveforms exceeds 13 dB, while the ER of MRM's resonant peak is less than 10 dB. This ER improvement indicates that the MZI mesh can enhance the signal quality to some extent during the linear transformation of input signals. We then measure the transmission spectrum of the MZI mesh and calculate the spectral responses of four logic functions in Figs. 3(d)–3(g), according to the theoretical input of the MZI mesh in the PULTC (spectral responses of other logic functions are provided in Supplement 1, Section S2). From 1520 to 1600 nm, all logic functions can reach an ER of around 10 dB. This bandwidth is sufficient to support the parallel operation of much more than 10 wavelengths. Figures 3(h)–3(j) depict the parallel output of different logic results from four spatial ports of the PULTC under three different configurations. The ER of all logic functions can exceed 13 dB, illustrating the excellent performance of PULTC's parallel processing in the spatial dimension.

Figure 4(a) depicts the high-speed test platform for the PULTC, where electrical Signal A and Signal B are applied to MRMs' GSG pads by microwave probes. To facilitate the control of the PULTC, we conduct optoelectronic packaging on the chip. The fiber arrays

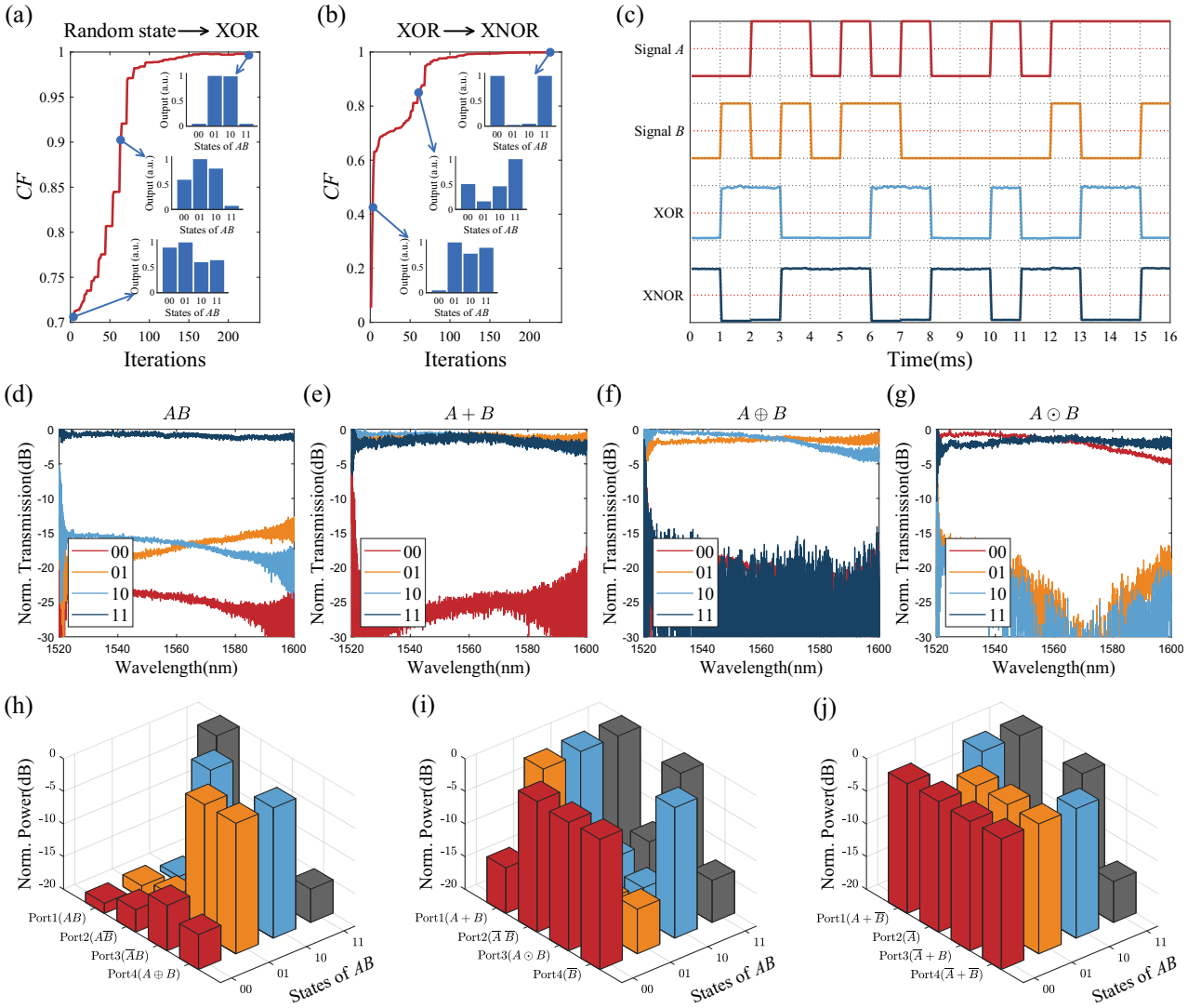

Fig. 3. Basic performance measurement of the PULTC. Iteration processes of the PULTC (a) from the random state to Logic XOR and (b) from Logic XOR to Logic XNOR. (c) Waveforms of Logic XOR and Logic XNOR implemented by the PULTC at the speed of 1 kbit/s. (d)–(g) Spectral responses of Logic AND, OR, XOR, and XNOR in the MZI mesh. (h)–(j) Parallel output of different logic results from four ports of the PULTC.

couple lightwaves into and out from the chip's optical gratings. Through wire bonding, the voltages of the heaters in MRMs and MZIs are applied by a multi-channel power source. We utilize a thermo-electric cooler to sustain the environmental temperature of the PUTLC. The measured EO bandwidth of the MRM in Fig. 4(b) exceeds 50 GHz, demonstrating its satisfactory modulation performance. By configuring the MZI mesh, we realize 14 different logic functions at the bit rate of 25 Gbit/s, which cover all possible cases of two binary signals except for the outputs of all zeros and all ones, as shown in Fig. 4(c). The 14 different logic results are consistent with the theoretical calculations, indicating the universality and reconfigurability of the PULTC. The output signal's quality degrades relative to low-speed scenarios, primarily due to the reduced quality of the original electrical signals. At the speed of 1 kbit/s, the electrical signal exhibits a nearly perfect square wave, whereas at 25 Gbit/s, it approaches a sinusoidal waveform. During the coherent combining of input signals, the long rise and fall times have a pronounced impact on the output signals. This issue can be further improved by using a better signal generator with a higher bandwidth, which would restore the sharpness of the input waveforms and improve ER performance at high speeds.

Further, we develop a photonic logic tensor card with PCIe and Ethernet interfaces for practical application scenarios. The photograph is presented in Fig. 5(a). We opt for a field-programmable gate array (FPGA) as the control unit, equipped with high-speed signal generators and receiver modules, which can support a maximum rate of 2 Gbit/s for signal generation and 6 Gbit/s for signal reception. The photodetectors (PDs) are integrated into the card and acquire the output optical signals through the fiber array. When performing multi-wavelength parallel computing, the wavelength division multiplexer (WDM) is used to divide wavelengths before the integrated PDs (more details of the photonic logic tensor card are provided in Supplement 1, Section S4). By compiling the FPGA, we can control the photonic logic tensor card to execute targeted tasks. Figure 5(b) depicts the evolution of elementary cellular automata (ECA), which can generate complex patterns through simple initial states [37]. The involved cells have two possible states (live or dead), corresponding to binary logic levels (Logic 1 or 0). According to ECA Rule 90, the next state of

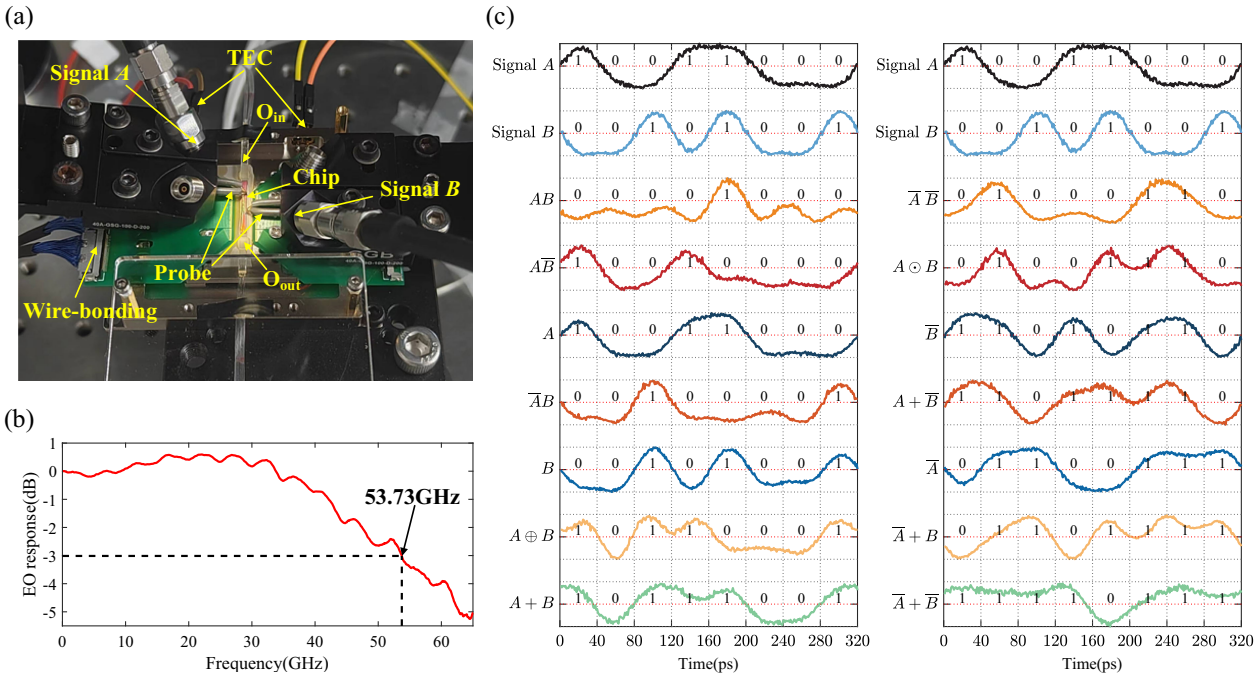

Fig. 4. High-speed performance characterization of the PULTC. (a) A high-speed test platform for the PULTC. (b) The EO response of the MRM. (c) Waveforms of input logic signals and 14 different logic operations at 25 Gbit/s. TEC, thermo-electric cooler.

the center cell is determined by the current states of the two cells around it. Therefore, we treat the states of cells on the left and right sides as logic Signal A and Signal B and feed them into the PULTC. The output results are processed by the FPGA and stored for the next iteration. After 64 iterations, the outcome of each iteration will compose the Sierpinski triangle, which is a classical fractal [38]. The corresponding experimental results of the iteration process are presented on the right side of Fig. 5(b). In some ECA models, the center cell's next state is affected by its current state. These can also be implemented by utilizing two spatial channels of the PULTC. One spatial channel is utilized to predict the state when the center cell is dead, while the other channel predicts the state when the center cell is live. The results of the two spatial channels can be selected by the FPGA according to the real state of the center cell.

In Fig. 5(c), we utilize the photonic logic tensor card to implement parallel encryption and decryption. Two original images are first flattened into sequence signals, serving as Signal A_1 and Signal A_2. Accordingly, two encryption patterns are generated randomly and flattened in the FPGA, which serve as Signal B_1 and Signal B_2. The FPGA controls the PUTLC to perform parallel Logic XOR operations and acquires the computing results detected by the PD array. In the encrypted images, we cannot obtain any information about the original images, indicating successful encryption. To decrypt original images, Logic XOR operations between decryption patterns and encrypted images are required. Only when the decryption patterns are identical to the encryption patterns, the original images can be recovered.

As shown in Fig. 5(d), we demonstrate the function of parallel image edge extraction with three images corresponding to three wavelength channels. For each channel, the original image is first binarized and replicated into two copies. One of them is shifted one pixel diagonally toward the bottom-right direction. The two images are then flattened into sequence signals (Signal A_i and Signal B_i). The above processes are completed in the FPGA. After pre-processing the three original images, it will simultaneously output sequence signals of the three channels to the PULTC, which executes parallel Logic XOR operations. The optical computing results are divided by the WDM into three wavelength channels and detected by different PDs, respectively (more details are provided in Supplement 1, Section S4). On the right side of Fig. 5(d), the experimental results are consistent with the simulated results, indicating that the parallel edge extraction is accurately performed by the photonic logic tensor card.

3. DISCUSSION

The proposed PULTC supports parallel logic computing in both the wavelength and spatial dimensions, whose computing capacity C is given by

$$C = m \cdot n \cdot s, \tag{7}$$

where m and n represent the numbers of multiplexed spatial and wavelength channels, respectively, and s is the operating speed of MRMs. The current PULTC chip has 10 wavelength channels and 4 spatial channels, with the MRM's speed up to 50 Gbit/s (experimental operation at 25 Gbit/s), resulting in a maximum computing capacity of 2 Tbit/s. This can be further enhanced by introducing more wavelength channels. To avoid the bandwidth limitation imposed by the MRM's FSR, we can first cascade multiple MRMs within each FSR, then use wavelength division multiplexers to combine them into the MZI mesh (more details are provided in Supplement 1, Section S5). It is also feasible to use FSR elimination methods of the MRM [39] or an FSR-free structure such as the nanobeam modulator [40]. In this case, the multiplexed wavelength channels depend on the bandwidth of the MZI mesh. The total bandwidth within the wavelength range of 1520–1600 nm can be calculated by

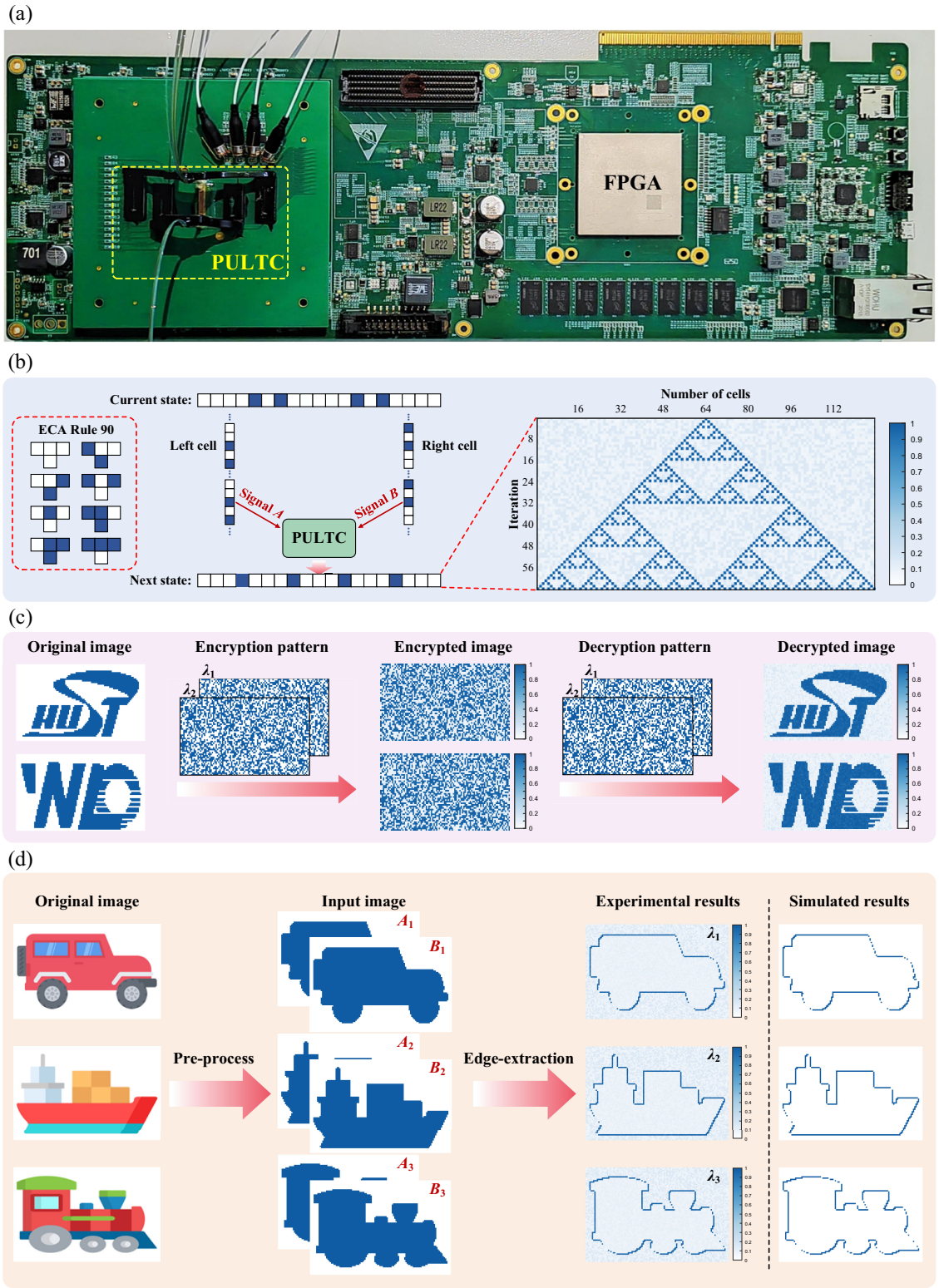

Fig. 5. Demonstration of the photonic logic tensor card. (a) A photograph of the photonic logic tensor card. (b) A simulated elementary cellular automata (ECA) to create the Sierpinski triangle by ECA Rule 90. (c) Parallel encryption and decryption of two images with 50 × 100 pixels. (d) Parallel edge extraction of three binary images with 75 × 115 pixels. Original Images in (d) are from [50].

$$\Delta f = \frac{c}{\lambda_1} - \frac{c}{\lambda_2} \approx 10\ \text{THz}, \tag{8}$$

where $\lambda_1 = 1520$ nm and $\lambda_2 = 1600$ nm. Provided that the bandwidth can be fully leveraged, the total computing capacity can reach 40 Tbit/s after multiplying by the wavelength and spatial dimensions. We can further improve the bandwidth by using ultra-broadband power splitters in the MZI mesh [41]. Optimization in both modulators and the MZI mesh will activate more computing

Table 1. Performance Comparison of the PULTC with Electronic and State-of-the-Art Photonic Logic Gates

Method	Function	Frequency	Computing Capacity	Computing Density	Power Consumption
Electronic CMOS logic gate [48]	–	∼GHz	∼Gbit/s (signal gate)	1000 Tbit/s/mm^2[a]	0.1–1 fJ/bit @GHz (10–100 fJ/bit @10 GHz)
Electronic–optical logic gate [9]	Fixed	20 GHz	40 Gbit/s	20 Gbit/s/mm^2	3.9 fJ/bit[b]
Frequency-domain logic gate [10]	Fixed	640 GHz	640 Gbit/s	–[c]	1 fJ/bit (without modulation)
Photonic logic tensor core	Reconfigurable	25 GHz	1 Tbit/s, currently (40 Tbit/s, potentially)	200 Gbit/s/mm^2	1.5 fJ/bit

[a]The area of a logic gate is assumed to be 1 μm^2 according to the NAND gate [51].
[b]Calculated by the dynamic power consumption.
[c]This method is realized by the discrete optical components.

capacity. To the best of our knowledge, the largest computing capacity in existing optical gates is 640 Gbit/s [10], which is realized by discrete and bulky optical components and cannot support reconfigurability. The joint utilization of wavelength and spatial dimensions allows the PULTC to harness optical parallelism, significantly advancing computing capacity.

The proposed PULTC fully exploits the optical advantages of high energy efficiency and operating speed in both signal modulation and linear transformation. In the PULTC, the MRMs are utilized to load electrical signals while performing nonlinear mapping. Benefiting from the well-developed silicon-integrated photonics, the MRM's power consumption per operation can be reduced to the femtojoule or even sub-femtojoule level with a maximum speed of 128 Gbit/s [42,43]. Once the electrical signals are loaded in light, the linear transformation of the MZI mesh is enough to obtain the desired logic functions, which can be regarded as a passive process. Diverse applications such as optical neural networks [44,45] and signal processing [46,47] have demonstrated the advantages of the MZI mesh in energy efficiency and operating speed. The power consumption per bit is estimated to be 0.32 pJ in the current form of the PULTC, where the thermal power in the MZI mesh accounts for the majority. Assuming the phase change materials are employed to replace heaters, the power consumption per bit can be reduced to 1.515 fJ. By comparison, current complementary metal oxide semiconductor (CMOS) gates dissipate 0.1–1 fJ/bit, while the operating frequency is limited to a few GHz [48]. As mentioned in the previous research, power consumption in CMOS gates will rise with an increase in frequency [9,49]. If the operating frequency is increased to tens of GHz, the power consumption per bit may rise to 10–100 fJ. Although electronic circuits currently offer higher computational density due to the high integration level of transistors, the proposed PULTC has the potential to outperform them in operating speed and energy efficiency (detailed power analysis is provided in Supplement 1, Section S6). A performance comparison of the PULTC with electronic and state-of-the-art photonic logic gates is presented in Table 1. The PULTC realizes reconfigurable logic functions and greatly enhances the computing capacity while maintaining low power consumption.

In summary, we devise a photonic logic tensor computing architecture to realize parallel logic computing for the first time. The PULTC is fabricated to support 10 wavelength channels and 4 spatial channels. The logic computing speed in one single channel can reach 50 Gbit/s, enabling the total parallel computing capacity of the PULTC beyond Tbit/s per core. After optimization, the computing capacity can reach 40 Tbit/s. We further develop the photonic logic tensor card with PCIe and Ethernet interfaces. Based on it, various functions including cellular automata, image encryption and decryption, and image edge extraction are realized. The proposed PULTC opens a new avenue for large-capacity, high-speed, and high-efficiency universal photonic logic computing.

4. MATERIALS AND METHODS

A. Performance Characterization Details of the PULTC

The performance characterization experiment can be divided into low-speed (1 kbit/s) and high-speed scenarios (25 Gbit/s). Heaters in MRMs and the MZI mesh are driven by a multi-channel power source, which is composed of analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and an FPGA chip for total control. The DACs can generate the required output voltages (ranging from 0–10 V) for each channel, while the ADCs are used to sample the output voltages converted from optical results by the PD array. In the low-speed scenario, we directly use the DACs to generate logic signals. In the high-speed scenario, we utilize two channels of a bit pattern generator (SHF 12104A) to generate different electrical signals (Signal *A* and Signal *B*) at 25 Gbit/s, which are applied with reverse bias through bias tees. The signals are then loaded to GSG pads of MRMs via microwave probes (GGB). The optical logic results are acquired by a photodetector (Finisar XPDV) and then recorded by an oscilloscope (Tektronix DSA72004B).

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HZ and WZ conceived the idea. WZ and BW designed the chip. WZ, BW, and WG performed the experiments. WZ, YZ, WW, and NC developed the photonic logic tensor card. HZ, JD, WZ, and BW discussed and analyzed the data. WZ prepared the manuscript. HZ, JD, WH, TH, LC, WD, DH, QW, and XX revised the paper, and XZ supervised the project. All authors contributed to the writing of the manuscript.

Disclosures. The authors declare that they have no competing interests.

Data availability. The datasets used and/or analyzed in the current study are available from the corresponding author upon reasonable request.

Supplemental document. See Supplement 1 for supporting content.

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