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Thermal Networks for Power Semiconductor Modules in Power Electronic Systems: A Review

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***Abstract*—A comprehensive review on the development of thermal network models for power semiconductor modules is conducted in this paper. Driven by the wide-spread applications of the power electronics in numerous applications, the development of power modules is revolutionised with higher requirements in power density, switching frequency, operational temperature and reliability, which in turn induces considerable challenges on the thermal management and modelling. As one of the most promising thermal modelling technologies, the thermal networks describe superior performance in long-term profile-based temperature estimation, excellent multi-physics analysis capability, good hardware compatibility as well as reasonable balance between computational load and accuracy. After revisiting the theoretical basis of the thermal networks, this paper focuses on the evolvement of the thermal networks in terms of format, modelling methodology, thermal boundary condition treatment and verification methods. The state-of-the-art topologies of the representative thermal networks are compared in detail, with a chronology of the thermal networks development being summarised. In addition, the typical application scenarios of the thermal networks and their advantages compared with other technologies are summarised, accompanied by a number of engineering implementation examples. What's more, the future development opportunities and challenges of the thermal networks are discussed, making this paper an all-around reference for researchers and engineers in the power module thermal modelling.**

***Index Terms*—Power Semiconductors; Power modules; Thermal Networks; Power Electronic Systems.**

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I. INTRODUCTION

MODERN power electronics system innovations push the power semiconductor modules towards higher power density, higher switching frequency, higher operating temperature, and better reliability [1]–[3]. All of these developing trends drive more challenges in thermal management of power modules, such as significant thermal coupling effects [4], thermal imbalance among parallel chips [5], transient temperature overshoot [6], etc. Moreover, with the community moving towards wide band-gap (WBG) devices such as silicon carbide metal-oxide-semiconductor field-effect transistor [7] and gallium nitride high-electron-mobility transistor [8], the faster switching speed drives module miniaturisation and parasitic inductance reduction [9], but the shrinking module dimension leads to more concentrated heat flux. As shown in Fig. 1, the intricacies of all these issues require a better knowledge of thermal modeling for the power semiconductor modules.

Thermal network [10] is one of the most widely accepted methods to represent the spatial thermal propagation and dissipation inside power modules. In the thermal network representation, the spatial thermal propagation and dissipation process inside the power modules are modelled by lumped elements, such as thermal resistor and capacitors, while the power losses and temperatures are emulated as currents and voltages in the thermal circuit, respectively. The compact format, circuit-compatible architecture and hardware friendly nature of the thermal networks make them good choices in a number of applications such as long-term profile based thermal simulation, multi-physics modelling or on-line temperature monitoring, where the proper trade-off between accuracy and efficiency is essential.

The thermal networks have significantly advanced the development and application of power modules. The power modules

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generate substantial heat when operating under high power conditions, and if not effectively dissipated, their performance and lifespan can be severely affected. The thermal network enables the modeling of heatsinks, guiding the design of materials, shapes, and sizes to enhance the thermal performance of power modules. In [11], a network composed of multiple thermal resistance chains on the heatsink fins is utilized to consider the temperature gradient effect, based on which different heatsinks are compared to achieve both good heat dissipation performance and low weight. Additionally, the thermal network is often combined with lifetime prediction techniques to calculate the accumulation of thermal stress in power modules during long-term operation, assisting designers in evaluating and optimizing module lifespan. The most common approach involves integrating loss models to compute the junction temperature of power modules, which is fed into a pre-designed lifespan model to achieve predictions [12]. Furthermore, the thermal network can model the thermal pathways, assessing their thermal parameters to guide the design of power modules. This has been reported in [13] to compare automated designs of power module substrates, achieving low thermal resistance and high power density.

The development of the thermal network models can be traced back to 1950's [14]. Since then, the basic formats of one-dimensional (1-D) Cauer and Foster networks have found extensive applications in the thermal modelling and electro-thermal simulation of power devices and modules. In the past two decades, alongside with the booming of carbon neutral solutions such as renewable energies, traction inverters and power transmissions, the theories and practices of the thermal networks for the power semiconductor modules have also marched to a new era. In an adaptation to the modern power modules with higher level of integration, more complex cooling design and harsher operation environment, the thermal networks have evolved from simple compact format to three-dimensions (3-D), from simple linear representations to complex nonlinear characteristics, and from simulation-based approach to experimental hardware compatibility development. Despite of such tremendous progress been made by the power electronics community, a comprehensive review on the thermal networks development is not found. In [15] where the thermal management of the IGBT power modules is reviewed, only a brief overview of the thermal networks is described. The review in [16] is focused on the compact 1-D thermal networks, while other types of thermal networks, the experimental verification and the application scenarios are not included. Although the development of the thermal network technologies is far from completed, the richness of emerging methodologies, topologies and applications deserves a review.

In this paper, a dedicated and comprehensive review on the thermal networks for power semiconductor modules in power electronics systems will be conducted. With key focuses on the current development status, the application scenarios and the existing challenges of the thermal networks, this paper aims at identifying the future research opportunities and proposing a development roadmap for such technology.

The main contribution of this paper lies in the following aspects. First, research milestones of the thermal network technology in the past decade, such as the theoretical background, various formats, derivation technologies, novel topologies and application scenarios will be summarised for an overview of the state-of-the-art development and future research directions. Second, the comparisons, between the thermal networks and other thermal modelling techniques, among various thermal network topologies as well as among different temperature monitoring technologies, will be conducted, which provide guidelines for thermal model selection in various applications. Third, the chronology of the thermal network innovations will also be briefed, with the future developments and challenges being discussed. It is noted that the thermal network research has been applied to a much broader scope, which contains but not limited to the capacitors [17], transformers [18], batteries [19], electrical machines [20]–[22] and very large-scale integrations [23]. However, this review will focus on the existing work regarding the power semiconductor modules. This is because the strong temperature-dependent features of the semiconductor device, packaging materials and cooling technologies make the related research work on the thermal networks highly-representative.

The remaining of this paper is organised as follows. Section II revisits the basic theory of the thermal networks, thermal impedance matrix and lumped element thermal networks. Section III reviews the evolution of the thermal networks, the theoretical derivation methodologies and verification technologies, with the comprehensive comparison among contributions and development milestones. In Section IV, the application scenarios of the thermal networks in power modules and modern power electronic systems are reviewed with details. In Section V, the existing challenges and future opportunities are discussed. Section VI concludes this paper.

II. Fundamentals on Power Modules and Thermal Networks

In this section, a brief introduction of the power modules and the fundamentals on the thermal networks will be conducted. After introducing the basic architectures of incumbent power modules and the internal structures, some insights into the thermal circuit, thermal matrix representation and basic thermal network formats will be discussed. Different thermal modelling technologies will also be compared.

A. Power Modules

In power semiconductor industry, power modules are developed to fulfil the increasing demand on power processing capability and system compactness, where a number of chips are integrated in single packagings. During the operation of the power semiconductor modules, heat will be generated due to power losses. To effectively cool a module, it is usually mounted with cold plates or convection fans. Depending on the heat flow directions, the incumbent power modules can be categorised as single-side cooled and double-side cooled (DSC) ones. The state-of-the-art structures of the single-side cooled power modules are represented by those applied in railway traction [24], electric vehicles [25], renewable energies [26], etc. Typical structures of the DSC power modules can

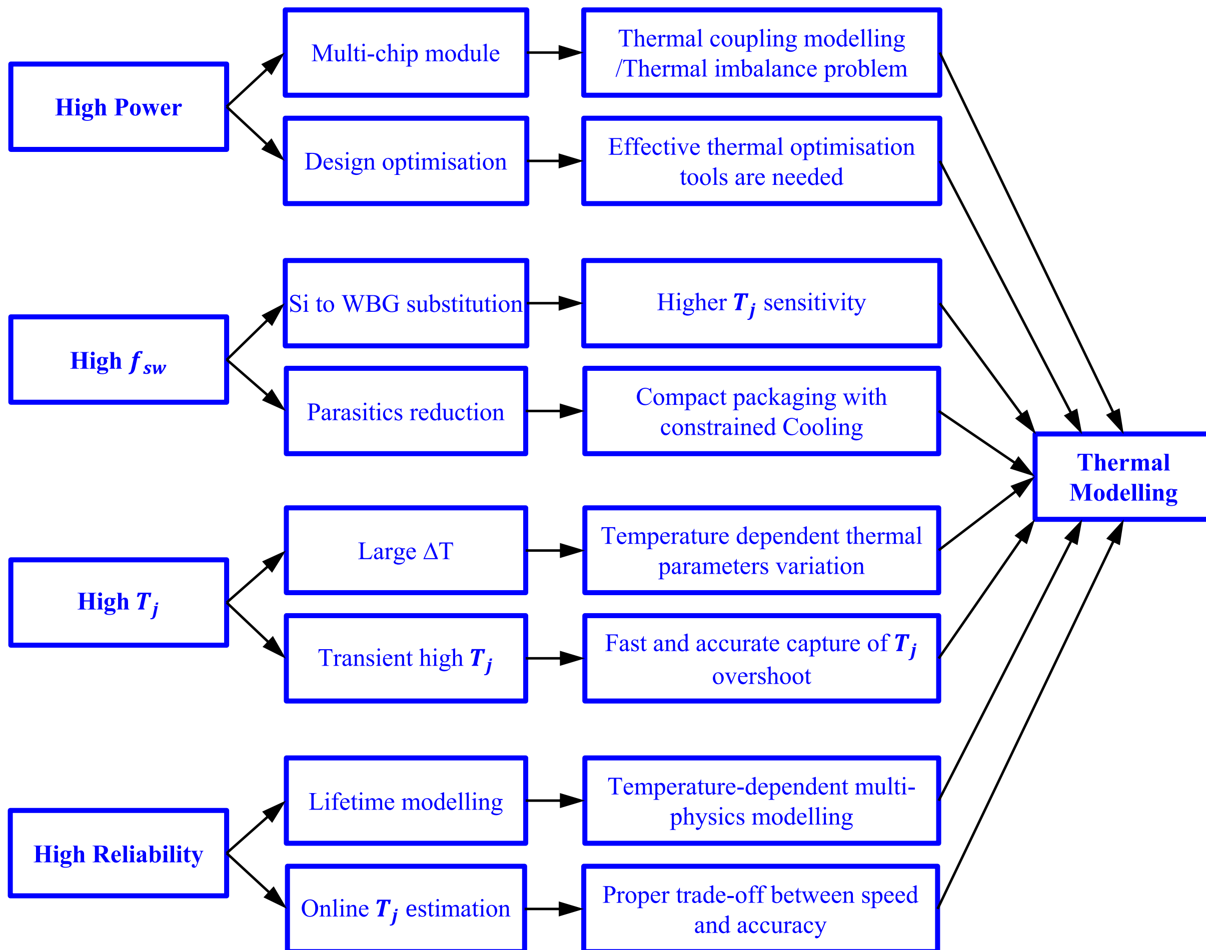

Fig. 1. Thermal modelling serves as the corner stone for advanced packaging technology.

be interpreted from those applied in the electric vehicles [27] or power transmission [28] market.

As a representative case, Fig. 2(a) shows a single-side cooled power module [29]. The power module has a half-bridge layout, where each switch is consisted of six insulated-gate bipolar transistor (IGBT) chips in parallel and the corresponding fast recovery diode (FRD) chips for reverse current commutation. In the vertical direction, the power module can be divided into seven layers, as can be seen from Fig. 2 (b). The module is in turn mounted on a heat sink with thermal grease as the thermal interface material (TIM). The generated heat from the chips will be dissipated vertically to the heat sink, while at the same time, lateral heat propagation cannot be ignored. Fig. 2 (c) demonstrates the simulated temperature field distribution when only IGBT chip U6 is heated. It can be seen that other chips are also affected by the temperature field considerably. Thermal management has been one of the major challenges for power modules, where a number of power chips are closely integrated leading to thermal couplings.

Traditional single-side cooled modules are unable to utilize the top surface of the chip as a thermal path, making it challenging to handle applications with increasing power density. DSC power modules use a wire-bondless packaging design, effectively utilizing the top surface of the chip for heat dissipation. This not only eliminates a major failure mode associated with wire bonds but also significantly reduces thermal resistance, improving cooling efficiency and power density. In light of the rapid development of power modules with DSC structure, new challenges such as thermal imbalance identification [30], cooling efficiency assessment [31] and thermal resistance degradation detection [32] need to be addressed.

B. Electrical and Thermal Analogy

As a result of the similarity between the second-order partial differential equations that describe electrical circuits (Ohm's law) and thermal propagations (Fourier's law) [33], [34], the thermal resistance in the thermal network representation between two nodes can be written as

$$R_{th} = \frac{\Delta T}{P} \tag{1}$$

, where ΔT is the difference due to the constant power flow (P) between the two nodes. Similarly, the thermal capacitance between the two nodes can be expressed as

$$C_{th} = \frac{E_{th}}{\Delta T} \tag{2}$$

, where E_{th} is the thermal energy stored between the two nodes during the constant power flow. In reality where the

power flow varies with time, ΔT also changes with time. There is a phase delay between $\Delta T(t)$ and $P(t)$ due to the energy stored in the thermal capacitance of the material. Likewise in the electrical analysis, such delay can be represented by the thermal impedance between the two nodes as

$$Z_{th} = \frac{\Delta T(t)}{P(t)} \quad (3)$$

. $\Delta T(t)$ and $P(t)$ are the time-varying ΔT and P, respectively.

C. Thermal Impedance Matrix

In a multi-chip power module system, the temperature of one chip will not only be influenced by the heat dissipation of itself, but also by its neighbours. The T_j of N chips in a power module can be derived as [35]

$$\begin{bmatrix} T_j^1 \\ T_j^2 \\ \vdots \\ T_j^n \\ \vdots \\ T_j^N \end{bmatrix} = Z_{ja} \times \begin{bmatrix} P_{loss}^1 \\ P_{loss}^2 \\ \vdots \\ P_{loss}^n \\ \vdots \\ P_{loss}^N \end{bmatrix} + \begin{bmatrix} T_a \\ T_a \\ \vdots \\ T_a \\ \vdots \\ T_a \end{bmatrix} \quad (4)$$

where T_j^n and P_{loss}^n denote the junction temperature and total power loss of chip n ($n \leq N$), respectively. T_a represents the coolant temperature at the inlet, which serves as a reference for the temperature evaluation. The thermal impedance Z_{ja} matrix can be expressed as

$$Z_{ja} = \begin{bmatrix} Z_{ja}^{1,1} & Z_{ja}^{1,2} & \cdots & Z_{ja}^{1,m} & \cdots & Z_{ja}^{1,N} \\ Z_{ja}^{2,1} & Z_{ja}^{2,2} & \cdots & Z_{ja}^{2,m} & \cdots & Z_{ja}^{2,N} \\ \vdots & \vdots & \ddots & \vdots & \ddots & \vdots \\ Z_{ja}^{n,1} & Z_{ja}^{n,2} & \cdots & Z_{ja}^{n,m} & \cdots & Z_{ja}^{n,N} \\ \vdots & \vdots & \ddots & \vdots & \ddots & \vdots \\ Z_{ja}^{N,1} & Z_{ja}^{N,2} & \cdots & Z_{ja}^{N,m} & \cdots & Z_{ja}^{N,N} \end{bmatrix} \quad (5)$$

. $Z_{ja}^{n,n}$ and $Z_{ja}^{n,m}$ are defined as the junction-to-ambient self-heating and coupling thermal impedance, respectively. By denoting the IGBT chips and FRD chips in the low side as U1-U6 and D1-D6 respectively, the simulated $Z_{ja}^{n,n}$ and $Z_{ja}^{n,m}$ curves are illustrated in Fig. 2 (d) [29].

The Z_{ja} matrix can be derived from either simulation or experimental test. It can be readily applied to the electro-thermal co-simulation to enable the self-consistent electro-thermal analysis. One additional advantage of the Z_{ja} matrix is that it can provide comprehensive 3-D spatial temperature distribution, providing enough temperature monitoring points are allocated on the left side of (4).

However, the application of the Z_{ja} matrix is sometimes hindered by its complex format. First, each element of the matrix will need to be extracted [36], [37], involving a large number of simulation runs in the state-space fashion. Second, as can be interpreted from (4), the dimension of the matrix increases tremendously with the number of temperature monitoring points [38]–[42]. Third, the implementation of the matrix as a galaxy of transfer functions in the digital signal processor (DSP) for the profile-based online temperature monitoring or prediction is challenging [43]. Considering the drawbacks in the derivation and direct implementation of the Z_{ja} matrix, it can be replaced by the thermal networks, where the large set of transfer functions is emulated by a number of lumped elements.

D. Foster and Cauer Networks

The thermal network is defined as an electrical analog [44] where the distributed heat propagation problem is described by critical temperature nodes and lumped elements such as thermal resistances [45], thermal capacitances [46], thermal impedances [47], thermal admittances [48] and controlled temperature [49] as well as power sources [50]. Being introduced initially to represent the heat dissipation behaviour of electronic components in lumped-fashion representations and enable circuit-style thermal analysis, the thermal networks have also been extended to characterise the thermal interaction among components that are placed in vicinity with each other. Such methodology focuses on the temperature values at a few critical nodes which are inter-linked by lumped elements and correspond to the physical objects inside the devices or systems. It has the potential to represent the heat propagation problem with high fidelity and low computational cost.

The basic formats of the thermal networks are Cauer and Foster types. In a Cauer network [51]–[53] as shown in Fig. 3(a), the thermal response of the system can be modelled by representing each layer of the thermal dissipation structure with a pair of R_{th} and C_{th}. In cases where thermal dissipation structure and material properties are known, the R_{th} and C_{th} parameters can be derived straightforwardly by adopting the analytical equations. In particular, R_{th} can be derived by

$$R_{th} = \int_0^l \frac{1}{\lambda(T) \cdot A(z)} dz \quad (6)$$

where l and $A(z)$ are the thickness of the layer along the thermal dissipation direction (z direction) and the cross-section area of the thermal dissipation path, respectively. $\lambda(T)$ is the specific thermal conductivity of the material with temperature dependance. C_{th} can be derived by

$$C_{th} = \int_0^l c(T) \cdot \rho \cdot A(z) dz \quad (7)$$

where ρ is the material density. $c(T)$ is the temperature dependent specific thermal capacity of the material. The number of R_{th} and C_{th} pairs usually corresponds to the layer counts inside the power module being studied [54]. It is seen that the Cauer networks can be derived purely from the dimensions and material information, corresponding to the physical structure of the thermal dissipation. The internal nodes of the Cauer network can also be interpreted as the layers inside the physical structure.

The Foster network [55]–[57] as shown in Fig. 3(b) is focused on the temperature difference between the junction and the ambient nodes when the power loss is applied on the chips. The C_{th} elements are not referenced to the ground

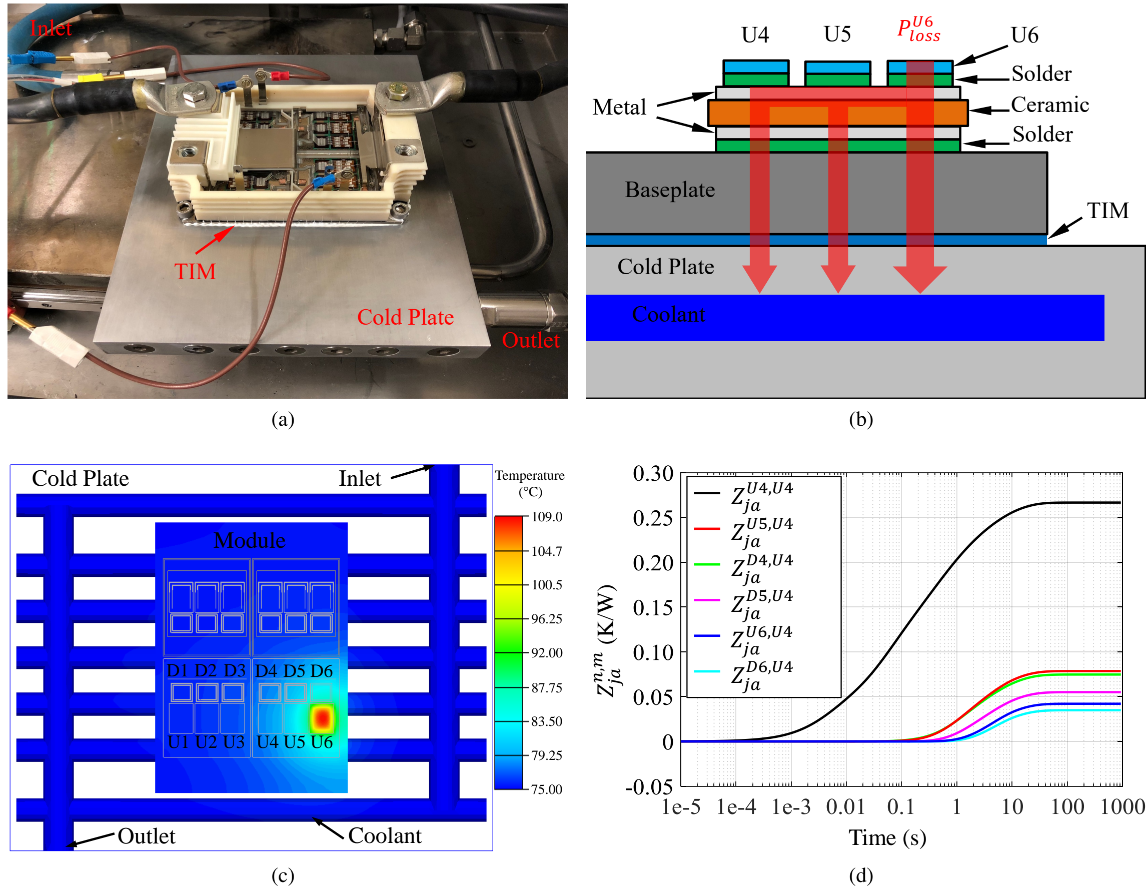

Fig. 2. An example of a multi-chip IGBT power module mounted on a water cooled cold plate. (a) An IGBT power module sample; (b) The cross-section view of the module thermal dissipation structure; (c) The thermal modelling with one of the chip being heated; (d) The self-heating and coupling thermal impedances.

connection, thus the internal nodes describe no physical significance. The R_{th} and C_{th} elements can usually be extracted from the numerical simulation or experimental measurement of Z_{ja} curves. With the known results of Z_{ja}, the following equation is usually adopted to extract R_{th} and C_{th} elements by curve fitting.

$$Z_{ja}(t) = \sum_{i=1}^{n} R_{th,i} \cdot [1 - e^{-\frac{t}{R_{th,i} \cdot C_{th,i}}}] \tag{8}$$

, where n denotes the number of R_{th} and C_{th} pairs in the network. Typically four pairs of lumped elements will suffice to provide a good fit of the Z_{ja} curve.

The loss information for the thermal models can be derived by analytical solutions, numerical simulations or measurement. For simple power circuit such as choppers, DC-DC converters or inverters, analytical formulas could be used. For more complex circuit where analytical solution is unachievable, numerical simulations could be adopted. In some applications, the power loss can also be extracted from experimental test.

A comprehensive comparison between the two networks can be found in TABLE I. Apart from those already discussed above, there are some additional features to mention. In terms of the derivation method, the Cauer network can also be determined by the structure function method, where the continuous variation of R_{th} with C_{th} along the thermal dissipation path is discretised into lumped elements [58]–[63]. The derivation of the Cauer network typically requires longer time since certain knowledge of the power module or extensive numerical calculation as well as intuitive discretion are needed. With more R_{th} and C_{th} pairs [64], the computation speed of the Cauer network is also lower than the Foster counterpart.

E. Comparison among Analytical Methods, Numerical Methods, Thermal Networks and Machine Learnings

Alongside with the fast development of the thermal networks, there are some other established or emerging thermal modelling methodologies. In this sub-section, four major thermal modelling methodologies, namely the analytical methods, numerical methods, thermal networks and MLs will be revisited and compared of the advantages as well as drawbacks. It should be noted that due to the existence of various thermal models within each category and the different levels of compromise between simulation speed and accuracy, only a general and qualitatively comparison of the four methods is provided.

The analytical methods for thermal modelling typically involve solving the thermal diffusion equations which rep-

TABLE I
Comparison between the Cauer and Foster networks

	Cauer Network	Foster Network	Notes
Physical Meaning	Yes	No	[65]
Derivation Method	Analytical/Structure Function	Fittings	Can be derived from each other.
Accuracy @ Four Orders	Medium	Good	Four orders as common choice in module data sheets. [66]
Derivation Time Needed	Long	Short	Cauer network derivation needs knowledge of the module.
Internal Temperature	Yes	No	Internal nodes of Foster network have no physical implications.
Application Readiness	Medium	Good	Cauer network typically needs higher order with slower computation speed.
T_a Variation Immunity	High	Low	[67]

TABLE II
Comparison among the four methods for thermal modelling. One, two and three stars represent dissatisfactory, medium and good performance, respectively.

	Analytical	Numerical	Thermal Networks	ML	Notes
Minimised computational load to obtain model	★★	★	★★★	★	ML needs training data.
Object Complexity	★	★★★	★★	★★★	
Simulation Time	★★	★	★★★	★★	
Model Accuracy	★★	★★★	★	★★	
Temperature Profile	★★	★★★	★★	★	ML is training data limited.
Profile Length	★★	★	★★★	★★★	Trained ML model can be fast.
Boundary Quality	★★	★★★	★	NA	Data-driven ML is boundary free.
Model Dimensions	1-D to 3-D	2-D to 3-D	1-D to 3-D	NA	ML is based on data.
ET Simulation	★★	★	★★★	★★	ML is to be further developed.
Physics Involved	★	★★	★★★	★★★	
Hardware Compatibility	★	★	★★★	★★	

resent the heat dissipation process inside the power module. Based on the given geometry, material properties and boundary conditions, the diffusion equations are solved in an analytical fashion with transformation techniques such as Fourier series expansion [68], [69], Green's function [70] and diffusive representations [71]. The solutions are usually steady state without considering the temperature field variation with time.

The analytical methods typically require simplification of the power module geometries and boundary conditions during the derivation of the mathematical expressions, which are mesh-less methods and computationally light. The explicit 1-D to 3-D mathematical expressions enable the all-around rendering of heat propagations and temperature distributions. They describe reasonable modelling accuracy after compromising with the modelling speed. With proper mathematical transformation, they can be coupled with other models with

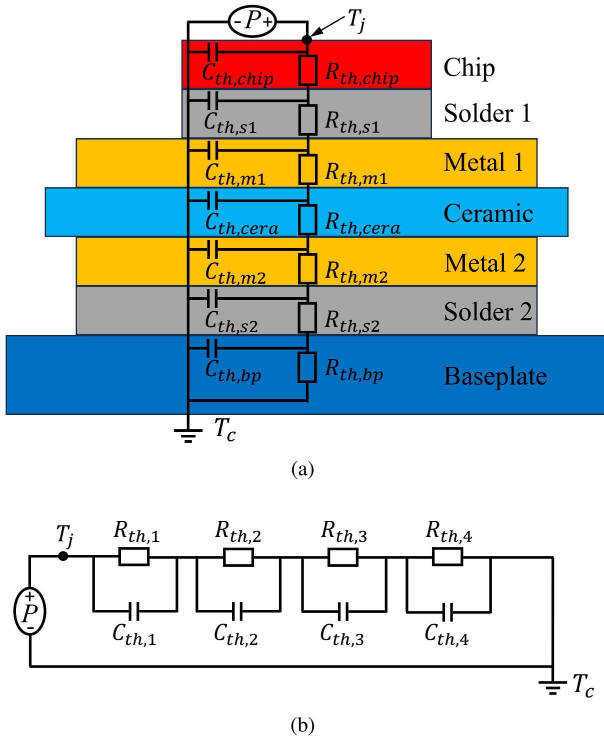

Fig. 3. Schematics of a Cauer and a Foster thermal network with T_c as the reference temperature. (a) The Cauer network with corresponding power module structure; (b) The Foster network.

different focuses, such as the electrical or mechanical domains. The major drawbacks of the analytical methods are the extensive mathematical derivation, complex physics background involved and incapability of cooperation with complex geometries, multi-chip systems [72] or transient thermal behaviours [73]. Those make the corresponding electro-thermal simulation slow and unsuitable for long-term mission-profile based temperature modelling. The compatibility with hardwares during online temperature estimation is also inadequate.

The numerical methods solve the partial differential equations of heat propagation by spatial as well as time discretion and boundary-condition-based iterations. The implementation of the meshes or nodes with high densities greatly improves the simulation precision with detailed spacial distribution and time variation of the heat flow and temperature fields. Based on the time-spatial discretion algorithm, the finite-element method [74], finite-difference method [75] and finite-volume method [76] are commonly used.

The numerical methods can provide the most accurate thermal modelling results with the powerful spatial meshing capability and versatile boundary condition models. It is capable of dealing with complex geometries, various thermal dissipation mechanisms and multiple heat sources. The rich data generated as a result of the simulation can provide comprehensive and accurate mapping of the key physical variables, such as the heat flow and temperature distributions. The standard working flow with commercial tools [77]–[79] also avoids tedious mathematical derivation or physics-based modelling. However, iteratively solving the numerous partial differential equations requires heavy computational load, extensive simulation time and large data storage space. When converged solutions of equations from different physical domains are required, the consumed computational power is also enormous, which makes such methods unsuitable for long-time multi-physics study or mission-profile-based temperature evaluations.

Apart from the traditional engineering methods, the ML based thermal modelling methods have also been developed recently [80]–[82]. Such methods typically incorporate certain type of artificial neural network models to describe the statistical relationship between the input conditions (power loss, ambient temperatures, heat transfer coefficients (HTCs)) and the output (T_j values). Due to the general ignorance of physics meanings in the modelling process, the derivation of the thermal models relies on the training data sets, which can be obtained by experimental test with sensors or simulations.

The data-driven ML techniques can revolutionise the thermal modelling practise. As the model derivation process is data-driven, the method can be generalised as an universal tool as long as good training data is supplied. The methodology is not sensitive to the geometric complexity, boundary conditions or heat transfer physics. Although the training process to derive the thermal model can be computationally heavy, the developed model can be light-weight and accurate. The compatibility with multi-physics simulation has not been fully developed but bears potential. The drawbacks of such method are also worth noting, that large sets of training data and extensive trainings in real-time are needed, to generate the temperature profile under specific working condition. The trained model may be unsuitable for application once the studied thermal systems are modified or degraded.

The thermal network method achieves a decent trade-off among the aforementioned factors. By representing the heat flow mechanism with an equivalent thermal circuit where discrete components are involved, the method simplifies the mathematical description of heat conduction as well as convection. The lumped-element fashion minimises the computational load and makes the long-term multi-physics analysis efficient. As a result of lumped elements used, thermal nodes arranged and boundary condition simplified, the modelling with thermal networks is by nature not as accurate as the other methods. However, it is fairly suitable for long-term profile-based thermal modelling. Due to its computationally light feature, it is suitable for multi-physics study where traditional analytical methods or numerical simulation meet considerable difficulties. The thermal networks can be easily solved within the framework of a SPICE or PLECS simulator and enable convenient electro-thermal coupling simulation. Also, it is readily to be applied in DSPs, where fast on-line T_j monitoring or prediction is needed [83], [84].

The comparison among the four methods can be seen in TABLE II. Here one, two and three stars represent dissatisfactory, medium and good performance, respectively.

III. Evolution of Thermal Networks

The thermal network concept had emerged in, if not earlier than, the 1950s [14]. As a result of the pioneering concept of

the analogy between electrical current flow and heat propagation in materials, thermal networks with the classical electrical T, L and π sections were initially proposed [14], [85]. In the 1970s, the thermal network concept had been extended to give more considerations to the physical geometries of complex structures, in terms of corresponding distributed [86] or lumped elements [87]. The fast growing computational capabilities of research labs in the late 1980s and 1990s, had boosted the wide-spreading adoption of the electro-thermal coupling simulation for electronic devices [88]–[96], where the demands for effective thermal network models were imperative. Since then, the development of thermal network technologies has merged onto the fast track.

A chronology of the thermal network development milestones in the past thirty-five years can be seen in Fig. 4. The progress of the thermal networks from fundamental to advanced formats can be interpreted. Although other key contributions also play essential roles in the development campaign, those listed in Fig. 4 are selected to represent the origins of the various methodologies reviewed in this paper.

The remaining section will discuss in detail on the evolution of the thermal network technologies, in terms of the format, methodologies, non-linear modelling and verifications. After categorising and detailing some representative development work, a comprehensive comparison among different contributions will be carried out.

A. Thermal Network Format

Since its initial development as compact or 1-D format, the thermal networks have evolved to describe 2-D and 3-D fashions [84], [109]. Here, the 1-D format is defined as those where the thermal dissipation is considered to be one dimensional, such as the basic Foster or Cauer formats in Fig. 3. Some 1-D Cauer networks with modified heat spreading angle and thus R_{th} as well as C_{th} are used for modelling thermal coupling but cannot be extended to multiple chip cases [107]. The 2-D format, apart from modelling the heat propagation in single direction, considers the lateral heat dissipation when there are more than one chip in the system and models the thermal coupling among them. Examples of this category include the modified Foster thermal networks with additional controlled temperature sources at junction nodes [110]–[113], Foster thermal networks with shared elements at the bottom of the module [114], modified Cauer thermal networks with additional controlled temperature sources at internal nodes [115], [116], and the Cauer thermal networks with lateral thermal resistances or capacitances to model the thermal cross-coupling [32], [117]–[121]. In most of the incumbent power modules where multiple devices are packaged together, the thermal dissipation during operation describes 3-D feature. To enable an accurate modelling including the time-spatial temperature distribution of the power module, the 3-D thermal networks are introduced, where the lumped elements are populated in a 3-D fashion to represent different paths of thermal dissipation. Some representative 3-D thermal network formats include the 3-D Cauer thermal network [108], 3-D stacked Foster networks [122], [123], and the 3-D node distributed thermal networks with uniformly spreaded lumped elements [124].

On top of the dimensional progression, it is also noted that the thermal networks have been extended to model the double-side thermal dissipation. However, thermal networks for the DSC modules describe additional features. First, unlike single-sided cooling modules, the thermal network here consists of two parallel RC thermal networks: one from the chip to the top surface and the other from the chip to the bottom, as shown in [32]. Typically, due to asymmetric module designs [125], a copper pillar spacer is placed in the middle of the module, increasing the thermal resistance of the top-side thermal path and making the two thermal networks asymmetrical. Second, DSC modules with multiple chips in parallel have several interconnections for heat dissipation [32], resulting in a more complex thermal network topology. Third, it should be noted that the thermal boundary conditions on the two sides of a DSC module may be different. For instance, the coolant temperature on the two sides may describe different values, leading to more complexity of the thermal network structure.

B. Methodology Development of Thermal Networks

Apart from the traditional derivation methodologies of the Cauer and Foster networks, a few more advanced algorithms are also developed for thermal networks with more convenient model derivation, simpler format or higher accuracy.

For model derivation convenience, novel artificial intelligence (AI) or ML process is combined with traditional thermal engineering practice. The AI technology and ac excitation of the system have been adopted to reduce the number of repeated simulation runs or experimental tests in the determination of the Z_{ja} matrix [126]. A thermal neural network (TNN) has been proposed in [127] via the combination of a deep-learning-based temperature model with the lumped element thermal network model. The TNN not only reduces the data sets as well as time needed for the training by incorporation of the lumped element thermal network model, but also substitutes the thermal physics needed in traditional thermal network derivations with artificial neural networks. Such approach bears the potential to achieve high estimation accuracy with small model sizes.

As for the format, simple fashions of thermal networks without losing important information have been developed. In [107], [128], the modified thermal networks, which are derived from modified heat propagation angle or path according to the thermal coupling analysis, can maintain the simple format of the thermal network while considering the thermal coupling phenomenon. To separately model the power module internal thermal coupling and external cooling setup, the thermal models with the cases as the reference nodes are developed in [129], [130]. By intentionally exposing the case node in the thermal network layout, the case temperature can serve as an input for determining the T_j.

To improve the accuracy, a lot of work has been done on top of the traditional Cauer or Foster network topologies. First, the modified Foster thermal network topology with additional corner-frequency-dependent elements have been introduced by

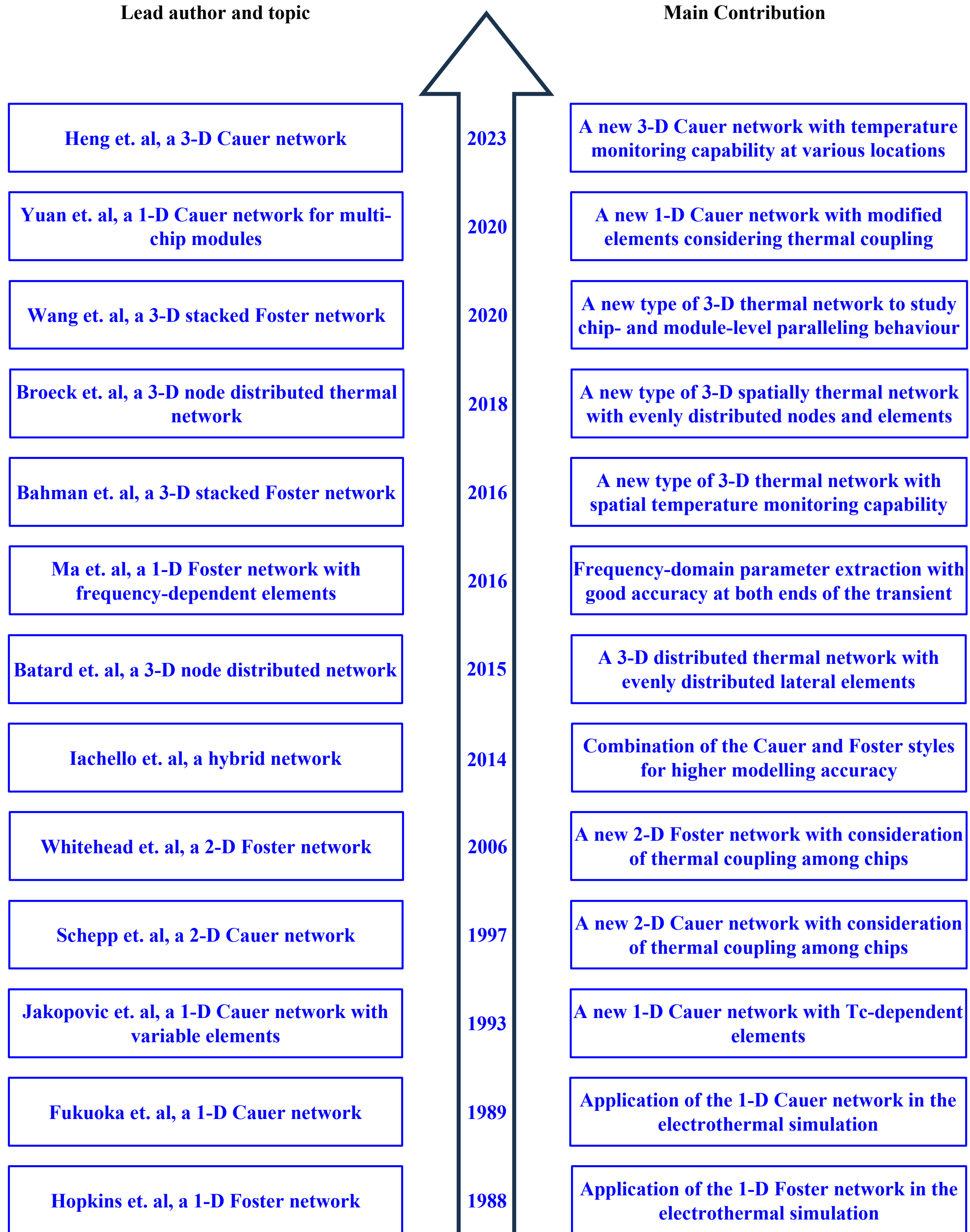

Fig. 4. Representative research works on the thermal network development in a chronological order [54], [97]–[108].

the frequency domain method to achieve satisfied accuracy at both ends of the modelled transient thermal response [54], [131]–[133]. Second, through the static FEM simulations, a better representation of the heat dissipation area has been achieved for higher estimation accuracy of the parameters in the Cauer networks [134], [135]. Third, the temperature-dependent variables are curve-fitted and adopted in the determination of the R_{th} and C_{th} components in the thermal networks, to enable dynamic update of the networks during application [113]. Additionally, the Cauer thermal networks have been improved to provide more accurate modelling of the thermal dissipation angle, by representing single layer of the thermal dissipation structure with multiple pairs of lumped thermal elements [136]–[138].

C. Nonlinear Thermal Networks

The traditional Cauer or Foster networks have simple formats and elements with fixed values, which corresponds to the systems with linear material properties, fixed boundary conditions and stable interconnection qualities. However, in the field application of the power modules, the ambient temperature, power losses, T_j and module ageing are in a dynamically variable status [16]. As the thermal networks being incorporated more and more in the reliability prediction, multi-physics simulation and online temperature estimation, they have been modified in different ways to be physically more sensible. Those modifications can be generally divided into two categories, namely the variable boundary condition treatment and the interconnection degradation modelling.

One of the most important factors that could influence the thermal network modelling quality is the boundary conditions [139] coupled with the non-linear thermal properties of the materials. Here the boundary conditions include all the quantities that could affect the temperatures at the semiconductor junctions or different layers, such as the power loss level, ambient temperature, heat transfer coefficient and coolant flow rate. To take this into consideration during the electrothermal simulation, modified thermal networks are introduced where amplitudes of the lumped elements are modelled as functions of the boundary condition variables. Cauer networks take into consideration of power loss [135], ambient temperature [34], heat transfer coefficient [140], T_j [141], [142], coolant flow rate [143], case temperature [144], heat sink temperature [59] and internal layers' temperatures [134], by variation of the R_{th} and C_{th} as variable-dependent functions, have been proposed. The Foster networks with consideration of power loss [113], ambient temperature [145], [146], heat transfer coefficient [72], coolant flow rate [147] and coolant temperature [147] by curve fittings of the relationship between the lumped elements and variables have also been introduced. In addition, the coolant flow rates and ambient temperature are also considered as variables that impact the elements in the 3-D node distributed thermal network [83].

Another essential factor to be considered is the parameter variation in the thermal networks due to ageing effect during the long-term application in temperature prediction or reliability modelling. As a result of degradation, the key interconnections or interfacing materials might be degraded to a level that the original thermal networks are no longer suitable as the circuit twin of the actual system. In this case, the thermal networks need to be properly updated according to the detected degradation level or help to detect the ageing level. Cauer networks take into consideration of solder void [148], solder degradation [149] and solder delamination [121] by variation of the R_{th} and C_{th} have been proposed. The Foster networks with consideration of TIM degradation [123], solder degradation [150], [151], solder delamination [113] have also been utilised.

D. Thermal Network Verifications

Almost all the thermal networks in the previous studies are presented with verifications either in simulation or experimental fashion. For the simulation verification, the numerical tools such as FEM or FVM are generally used. The operation of the module under application scenarios such as ac current conduction or PWM heating is emulated to extract the T_j response, results of which are compared with the thermal network simulation in a circuit fashion.

As for the experimental setups used for the verification of thermal networks, a few different categories are worth mentioning. First, as a basic format, the dc heating test is extensively adopted, with the purpose of monitoring the temperature variation or further extracting the transient Z_{th} from the cooling curve. Such method can provide detailed thermal response of the thermal system in relatively small time scales. Second, the PWM heating or stepped dc heating tests are incorporated to verify the thermal network performance during modulated dc heating. The resulting temperature variations are compared with those from the corresponding electro-thermal simulations with the thermal networks. This is a basic format to verify the long-term performance of the thermal networks. The comparisons are usually taken at the stable operating periods of the temperature rise, which however bypasses the effects of the thermal capacitances at high-frequency switching. Third, the practical PWM inverter circuits or dc converter circuits are comparatively studied by both the thermal-network-based multi-physics simulation and experimental test. Again, the initial transients of temperature rise during the starting process of the inverters are generally ignored, which could be used for verifying the C_{th} elements of the thermal networks.

E. Comparison of Contributions

While a number of significant progresses have been achieved for the thermal network development, the reported works on thermal networks from various research groups describe their unique advantages but sometimes exclude key factors for simplicity of implementation. It is thus necessary to have a complete comparison of the representative prior arts in the past decade, to provide a general idea of the key aspects of consideration in the development process. Based on the above discussions, the summary of the representative thermal network topologies can be seen in TABLE III. The comparison can serve as the basis for the selection of the thermal network methodologies based on the respective needs of the readers.

From the comparison, a number of observations can be summarised. First, the derivation of the thermal network elements is still strongly dependent on the numerical methods such as FEM. While the community is working together to bypass the heavy computation load of the FEM, the collaboration between the thermal networks and the FEM simulation can ensure reasonable accuracy and efficiency. Second, some of the developed models might meet difficulties due to the absence of key considerations. For example, the models with linear material property may have large simulation errors if the temperature swings are significant. Also, the models without the thermal coupling factors may not be suitable for power modules where strong thermal interaction among chips is prominent. Third, the adoption of variable-dependent elements

TABLE III
Comparison among the representative thermal network topologies in the past decade.

Literature	Network Topology	Derivation Method	Material	Boundary Condition	Coupling	Verification	Notes
Gachovska, 2013 [152], [153]	1-D, Cauer	Eq.(6),(7)	Nonlinear	Fixed T_c	No	PWM Heating	T-dependent R_{th} & C_{th}
Wu, 2014 [141], [154]	1-D, Cauer	FEM+Eq.(6),(7)	Nonlinear	Fixed T_a	No	DC Heating	T-dependent R_{th} & C_{th}
Du, 2020, [148]	1-D, Cauer	Eq.(6),(7) with voids	Nonlinear	Fixed T_a	No	Stepped dc Heating	Void-based R_{th} & C_{th}
Yuan, 2020, [107]	1-D, Cauer	FDM+Eq.(6),(7)	Linear	Fixed T_a+HTC	Yes	PWM Heating	Coupling-based R_{th} & C_{th}
Górecki, 2020, [34]	1-D, Cauer	Test+Numerical	Unknown	Varied P_{loss}, T_a	No	PWM Heating	T-dependent R_{th} & C_{th}
Wang, 2021, [144]	1-D, Cauer	Modified Eq.(6),(7)	Unknown	Fixed T_a	No	PWM Heating	T_c-based R_{th} & C_{th}
Chen, 2021, [59]	1-D, Cauer	FVM	Nonlinear	Variable T_h	No	Z_{th} Measurement	T_h-based R_{th} & C_{th}
Tian, 2021, [142]	1-D, Cauer	Modified Eq.(6),(7)	Nonlinear	Fixed T_a and HTC	No	FEM	T_j-based R_{th} & C_{th}
Yang, 2022, [134]	1-D, Cauer	FEM+Eq.(6),(7)	Nonlinear	Fixed T_a+HTC	No	FEM+PWM Heating	
Heng, 2022, [135]	1-D, Cauer	FEM+Eq.(6),(7)	Nonlinear	Fixed T_a+Variable HTC	No	PWM Heating	
Liu, 2023, [149]	1-D, Cauer	Eq.(6),(7)+Correction	Nonlinear	Fixed T_c	No	Buck Converter	V_f-based R_{th} & C_{th}
Han, 2023, [116]	1-D, Cauer+Source	Eq.(6),(7)	Nonlinear	Fixed T_a+HTC	Yes	Inverter+FEM	Compared with others
Ma, 2016 [54]	1-D, Foster	Frequency domain	Linear	Fixed T_a	No	DC Heating	f-dependent R_{th} & C_{th}
Akbari, 2021, [113]	1-D, Foster	FEM+Fitting	Linear	Variable T_a	Yes	PWM Inverter	Variables-based R_{th} & C_{th}
Zhang, 2022, [151]	1-D, Foster	FEM+Fitting	Nonlinear	Fixed T_a+HTC	No	FEM	PID-based R_{th} & C_{th}
Xu, 2022, [129]	1-D, Stacked Fosters	Test+Fitting	Unknown	Referenced at T_c	Yes	Measured T_c	Module-level TN
Li, 2017, [120]	2-D, Cauer	FEM+Fitting	Linear	Fixed T_a+HTC	Yes	FEM	
Cui, 2022, [121]	2-D, Cauer	Eq.(6),(7)	Linear	Fixed T_a+HTC	Yes	FEM	Peeling-based R_{th} & C_{th}
Chen, 2023, [32]	2-D, Cauer	Test+Fitting	Unknown	Fixed T_c	Yes	FEM	
Guo, 2023, [84]	2-D, Cauer	FEM+Numerical	Linear	Fixed T_a	Yes	FEM+Inverter	
Shahjalal, 2020, [66]	2-D, Stacked Fosters	FEM+Fitting	Nonlinear	Fixed T_a+Variable HTC	Yes	dc converter	
Heng, 2023, [108]	3-D, Cauer	FEM+Eq.(6),(7)	Nonlinear	Fixed T_a+HTC	Yes	PWM Heating	
Bahman, 2014 [104], [155], [156]	3-D, Stacked Fosters	FEM+Fitting	Nonlinear	Fixed T_a+HTC	Yes	PWM Inverter+FEM	
Bahman, 2017 [72], [157]	3-D, Stacked Fosters	FEM+Fitting	Nonlinear	Varied P_{loss}, T_a and HTC	Yes	PWM Inverter+FEM	T-dependent R_{th} & C_{th}
Zhang, 2020, [122]	3-D, Stacked Fosters	FEM+Fitting	Linear	Fixed Surface T	Yes	FEM	
Wang, 2020, [106]	3-D, Stacked Fosters	FEM+Fitting	Unknown	Fixed T_a	Yes	FEM+PWM Inverter	Inside and inter- module
Shi, 2022 [73]	3-D, Stacked Fosters	FEM+Fitting	Nonlinear	Fixed T_a+HTC	Yes	AC Heating+FEM	
Zhang, 2023, [123]	3-D, Stacked Fosters	FEM+Fitting	Nonlinear	Fixed T_a+HTC	Yes	FEM	
Broeck, 2015, [105], [158], [159]	3-D, Node distributed	Discretion+Eq.(6),(7)	Linear	Fixed T_a+HTC	Yes	PWM Inverter	
Ma, 2021, [83]	3-D, Node distributed	FEM+Numerical	Nonlinear	Fixed T_a	Yes	PWM Inverter	
Zhan, 2023, [109]	3-D, Node distributed	FEM+Numerical	Linear	Fixed T_a+HTC	Yes	FEM+Inverter	Compared with others
Lu, 2024, [143]	3-D, Node distributed	FEM	Nonlinear	Varied T_c and P_{loss}	Yes	FEM+PWM Inverter	T-dependent R_{th} & C_{th}

in the thermal network seems to be a popular solution to take into consideration of the nonlinearity caused by the materials, boundary conditions and degradations.

IV. Thermal Network Applications

The thermal network technology has found extensive applications in the past decades due to the abovementioned advantages. In this section, the most common and representative application scenarios of the thermal network technology are summarised, including the online temperature extraction, reliability modelling, multi-physics power electronics performance evaluation and power module status monitoring.

A. On-line T_j Extraction

Apart from the routine voltage and current measurement, the online temperature extraction is essential for monitoring the status of the power electronic systems' operation, avoiding catastrophic failure of the power modules due to over temperature and optimisation of the cooling parameters. In the extraction process, not only the T_j of the semiconductors are important, but also the temperature at different layers of the thermal dissipation path should be considered. Alongside with the development of the power module and the advances in power electronic systems, a number of temperature monitoring methods have been proposed, including the contact methods, Infrared methods, fibre-optic methods, TESP methods [160], [161] and thermal networks.

First, a number of contact-based methods are commonly used, such as the thermocouples [162] and thermistors [163]–[168]. The methods based on thermocouples are invasive that require some kind of modification to the device under test (DUT). The thermistors are based on the thermal resistors whose resistances varies with the temperature. The thermistors provide a cost-effective method to monitor the temperature near the power chips. However, there are a few drawbacks such as measurement accuracy, high-voltage isolation challenge, delays in response and increased process complexity for power modules.

Second, the infrared-based temperature test methods find their application in T_j monitoring, including the infrared cameras, infrared sensors and infrared microscopes. They detect the emitted infrared energy of the DUT and electrically convert it into surface temperature profiles. As a contactless detection method, it has good accuracy in mapping the surface temperature distribution of the DUTs. However, this method typically requires preparation of the DUTs such as encapsulation, gel removal and surface coating. In most of the cases where die top interconnections (such as wire bonds) are indispensable, the detected T_j is typically interfered by that of the interconnections, which introduces inconsistent temperature evaluation result.

The thermal fibre-optic sensors [36], [126], [169] are based on the light absorption/transmission frequency band shift inside the fibres caused by the semiconductor materials at the probe head, such as the gallium arsenide. As a contact-based method, the DUTs should be exposed and form an intimate contact with the probe. Such sensors have been used extensively for researches where the surface temperatures of the power devices are of concern.

Third, the TESP methods take advantage of the correlation between some of the electrical parameters and the T_j of the semiconductors. Those parameters [170] include but are not limited to the on-state voltage drop ($V_{ce(on)}$ for IGBTs and $V_{fd(on)}$ for FRDs), turn-off delay time $t_{d,off}$ [171], gate threshold voltage and peak gate current. The TESP methods have attracted considerable attention due to the non-invasive T_j measurement capability, fast response during measurement and good accuracy. However, a number of disadvantages of this technique should be noted. On the one hand, the measurement accuracy is highly dependent on the calibration [172]. On the other hand, the temperature distribution or the maximum T_j inside the power module cannot be revealed. Additionally, in most power modules where the actively controlled devices (such as IGBTs) are allocated with anti-parallel free-wheeling chips (such as FRDs), the simultaneous measurement of the T_j values is challenging.

Last but not the least, the thermal network based methods adopt the aforementioned topologies for the on-line temperature extractions [30], [173]. During the test or the operation of the power electronic system, the internal temperatures of the power module can be extracted by different methods. For one thing, by measuring the power losses at the power semiconductor chips, the T_j can be calculated by the thermal networks effectively in a circuit fashion. For another, any measurable external temperature levels, such as the temperatures of the heat sink of the cooling system or case of the power module [174], can be used as a reference point to infer T_j or other internal temperature values [166]. Such method is non-invasive that no modification work is needed for the power module under test. Correspondingly, it is also feasible to obtain T_j from the TESP method and then derive the T_c value for a small outline transistor package by the predefined thermal network. In addition, all the critical temperature monitoring points can be included in the thermal networks preparation stage, such that the thermal response of the module internal parts can be derived efficiently. The above feature makes the thermal networks suitable for on-line temperature monitoring purposes. However, it has to be noted that the derivation accuracy is sensitive to the boundary condition and degradations of the interconnections.

A detailed comparison of the above methods for T_j extraction can be found in TABLE IV, where the abovementioned factors are considered.

B. Reliability Modelling

Another representative application of the thermal networks is for the reliability modelling of power devices or modules used in power electronic systems in both short transients with extreme loads [175]–[178] and long-term operations [179]–[182]. It is known that the temperature swings at the semiconductor junctions and different layers of the packaging structure

TABLE IV
Comparison among the temperature monitoring methods.

	Contact Methods	Infrared	Optical Fibres	TSEP	Thermal Networks
Test Preparation	Circuit Setup	Alignment	Alignment	Circuit Setup	Network Derivation
Module Preparation	Opening/Attach	Opening/Coating	Opening/Attach	Circuit Connection	Not Needed
Contactless	No	Yes	No	Yes	Yes
Detection Range	Contact Points	Points/Area	Contact Points	Averaged T_j	All around
Module Internal T	No	No	No	No	Yes
Accuracy	Low	High	High	Medium	Medium
Response Speed	Slow	Medium	Medium	Fast	Fast
Ageing Sensitive	No	No	No	Yes	Yes
Application	On-/off-line	Off-line	Off-line	On-/off-line	On-/off-line

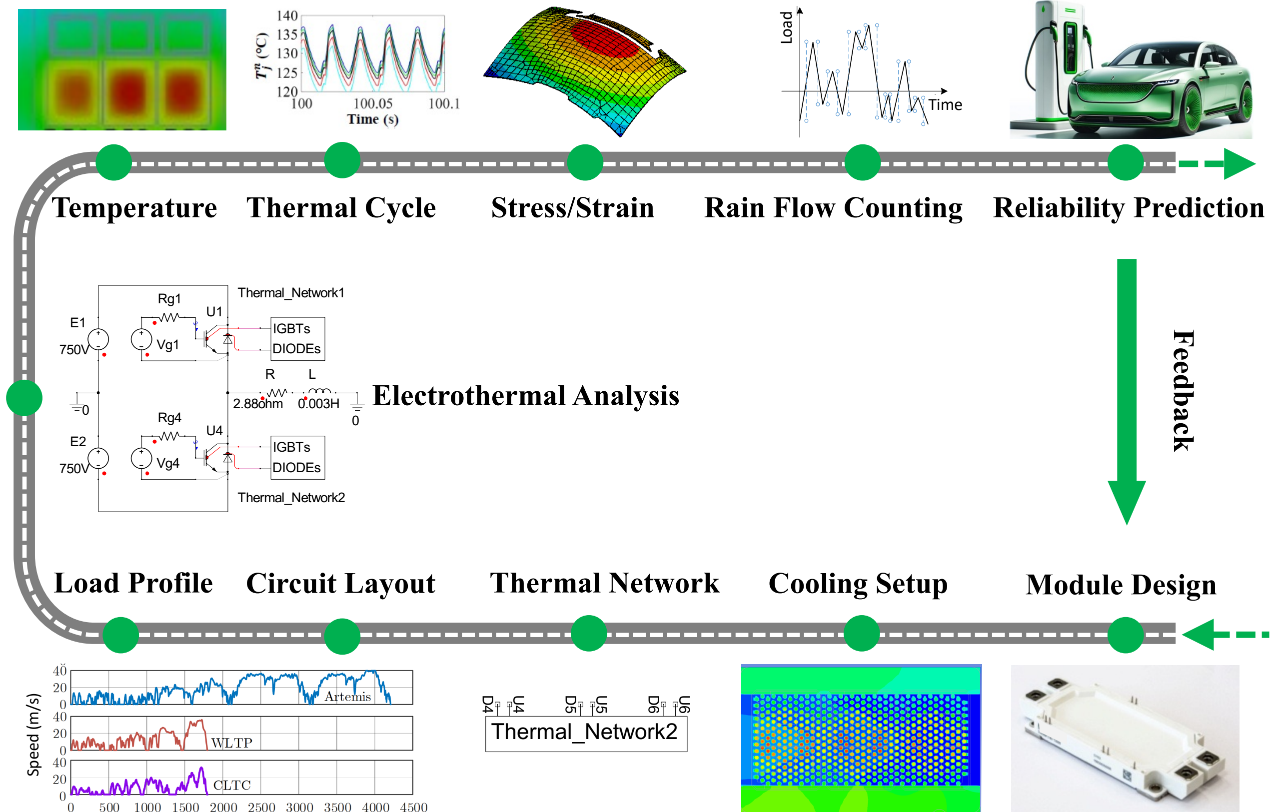

Fig. 5. Working flow of the reliability modelling using thermal networks.

induce considerable thermal-mechanical stress. Such repetitive thermal-induced stress, under long-term mission profiles condition, may accumulated as fatigue inside the materials or at the interfaces [183], [184]. As the power modules are designed to be operational in a relatively long time ranging from years to several decades, the mission-profile based reliability assessment is indispensable for lifetime prediction, which in turn calls for the computationally efficient thermal models for temperature prediction. Due to the nature of the semiconductor power devices, the thermal models for temperature prediction

should be suitable for electrothermal characterisation [185]–[188].

One of the viable working flows for the reliability modelling is illustrated in Fig. 5. In the process, the 3-D physical design of the power module and the cooling boundary conditions are represented by a conservative thermal network, which has been extracted from the Z_{ja} matrix of all the chips in one switch and approximated in a packed conservative format with consideration of both self-heating and coupling thermal impedances [189]. The thermal network can accept the information of power losses while feedback the instant temperature of the internal devices by the pins allocated. The thermal network is then adopted in the electrothermal analysis in a circuit fashion with emulation of the long-term mission profiles. The temperature-induced mechanical stress and strain by the thermal cycles are in turn accounted by rain flow counting and the corresponding lifetime models, where the reliability performance of the power module can be predicted. It is noted that other types of lifetime modelling procedures are also applicable [145], [190]. The thermal networks can also help to derive the layers' temperature during the operation condition for further reliability assessment [189], [191].

C. Multi-physics System Performance Evaluation

Apart from the well known electrothermal coupling analysis for the reliability assessment, the performance evaluation and failure analysis of power semiconductor modules call for the multi-physics analysis where the interaction among multiple physics domains should be considered. For the power modules in power electronic systems, the overall performance depends on the intensive interaction among multiple physical domains [192] such as the electromagnetic (EM) fields, the electrical behaviour, the thermal characteristics and the mechanical stability. The analytical methods and numerical simulations meet tremendous difficulties where more engineering disciplines are involved in the multi-physics coupling analysis, such as extremely long simulation time, huge hardware storage space needed and challenges in achieving numerical convergence. The thermal networks simplify the thermal characterisation and provide convenient interfaces with other engineering domains, forming an efficient multi-physics coupling analysis with broad application scenarios.

Fig. 6 illustrates the application of the thermal network technology in the EM-electrothermal analysis for the multi-chip power modules [26]. In the simulation, the EM networks and thermal networks are both extracted from the 3-D structure to form the reduced-order model representation. Then the multi-physics coupling problem can be solved in a circuit fashion, avoiding solving the complex matrix of space differentiated coupling equations. Apart from the EM-Electrothermal simulation, the thermal network topology can also be applied in other multi-physics analysis, such as electrothermal-mechanical [28], [38] and electrothermal-EMI simulation [193], [194]. It should be noted that the capability of enabling fast and accurate multi-physics simulations also makes the thermal network well suited for power module design optimisation. In particular, for the WBG power module industry where no standard packaging layout exists, customised designs extracted from fast simulation-based optimisation process are essential.

D. Power Module Status Monitoring

The thermal networks have also been used in the other status monitoring process of the power semiconductor modules. In the reliability assessment or long term application process of the power modules, the internal interconnection properties or the external cooling boundary condition may vary. Since the thermal networks can describe the physical thermal dissipation structure effectively, any real-time change of the latter can be correspondingly detected or interpreted by the former.

As an examples, it was proposed in [151] a method of extracting the void levels of the chip solder layer by combination of a thermal network and the proportional integral (PI) control [151]. In the thermal network, the thermal resistances and capacitances corresponding to the chip and its solder layer are established as functions of the dissipated power (P) and solder degradation factor (d), by means of FEM simulation and curve fitting. In the extraction process, the extracted temperature information from the thermal network is fed into the PI controller, which is used to determine the value of d. P and d are then used for updating the thermal resistances and capacitances of the top two layers of the thermal network. The process is iterated until a convergence is reached. Then the level of the chip solder void can be interpreted from the final value of d.

Besides the above methodology, the thermal networks can also be applied in the monitoring of the substrate solder layer degradation via detecting the temperature profiles at the bottom of the module baseplate [195]–[198] or based on eddy current pulsed thermography approach [199], the TIM temperature variation [122], and the coolant status with varying flow speed by the help of NTCs or IR cameras [200], [201].

For different application scenarios, the selection of the suitable thermal modelling approach is a trade-off among various factors, such as the key focus of the modelling, the computational power, the accuracy expectation and the spatial as well as time scale of the system. Besides, the level of complexity for the module structure also plays a key role in decision making. It is suggested to establish key evaluation criteria, assign appropriate weight coefficient to each criterion and score the approaches according to the comparisons in TABLE I-III. This allows for the calculation of an overall score for each modelling method to inform the final decision.

V. Existing Challenges and Future Opportunities

This section will focus on the existing challenges in the development and the future research as well as application opportunities of the thermal networks for the power modules in power electronic systems. It is believed that the development of the thermal networks hasn't touched its limit since the modern electrification revolution is still ongoing, where the power modules are widely adopted in the collection, transmission as

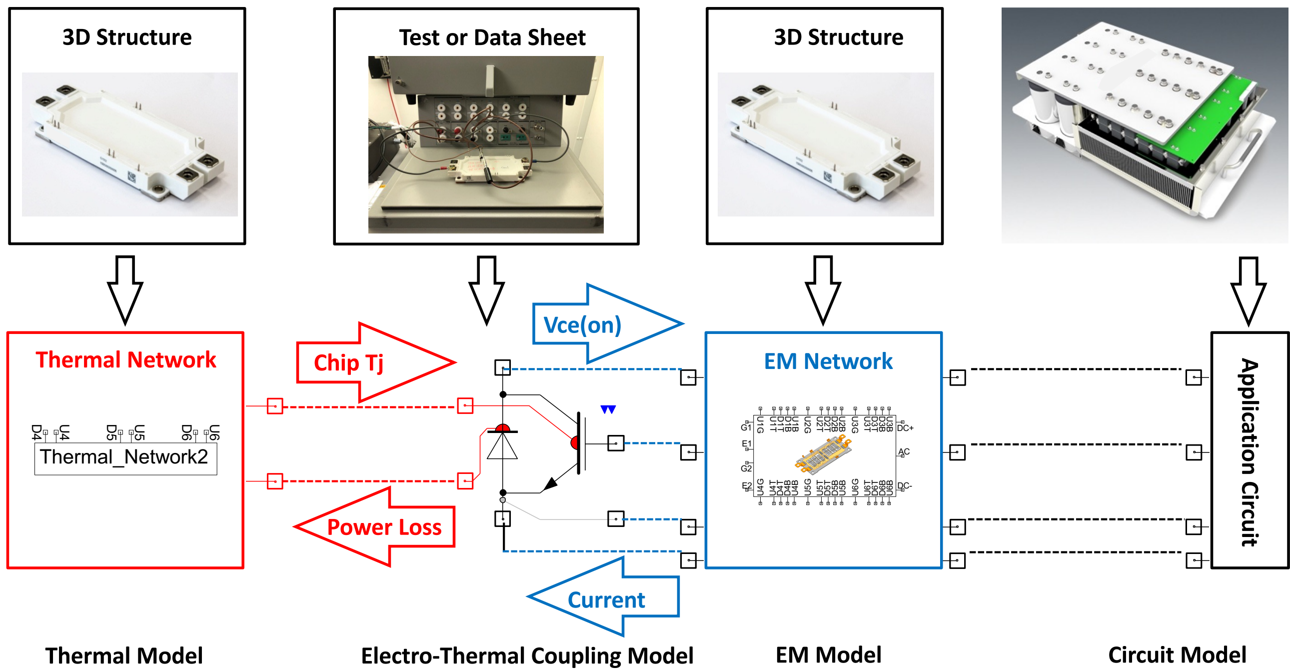

Fig. 6. Scheme of the EM-electrothermal multi-physics simulation (modified from [26]).

well as application of the renewable energies. The emerging application scenarios and power module developments always bring challenges but also hatch new opportunities for the thermal network technology.

A. Existing Challenges

Obviously, the very first challenge for the thermal network development is the trade-off between the simulation speed and modelling accuracy [202], [203]. The traditional Cauer and Foster networks in the basic format, due to the nature of one-dimensional heat flow assumption, describe limited accuracy for thermal modelling of the power modules where lateral heat flow cannot be ignored. The aforementioned countermeasures such as the variable elements, the 3-D thermal networks and the frequency-domain methods, while being effective in the specified cases, still need further verification with broader application scenarios. In particular, the unevenly distributed or unstable boundary conditions, the variable operation conditions hence power loss profiles and the degradation related parameters variations cause major obstacles to balance the model complexity and efficiency. As has been proposed in [204], the maximum allowable errors can be quantitatively defined such that the minimum computational effort with the thermal networks can be sort after.

Another challenge is the incorporation of the thermal network technology into the power module design and optimisation practice. Most of the prior-art literatures have shown the unidirectional thermal network extraction from the 3-D physical structures and corresponding evaluations, but the results cannot be fed back effectively to the power module design practice. For example, the scheme as shown in Fig. 6 has unified the EM network and thermal network in the multi-physics coupling modelling. However, the extracted thermal network and the simulation outcome can't provide direct feedback on how to optimise the 3-D structure to achieve better thermal performance. In an ideal case, the evaluation results should be able to provide indicative information for the optimisation of the power module, such as the layouts of paralleling dies, interconnections and packaging materials. To achieve this, two issues need further investigation. One is the automated extraction, evaluation and result analysis of the thermal networks, a premature example of which has been proposed in [75]. The other is the interpretation of the multi-physics as well as multi-objective results and automated design iterations to form a closed loop of the optimisation cycle.

Third, the large number of chips integrated in single power module and the structural complexity have induced additional challenges. On the one hand, for multi-chip power modules, the number of lumped thermal elements in the corresponding thermal networks increases dramatically. Due to the increased power levels, both the transient over-temperature of the regional hot spots and the averaged temperature should be monitored properly, to account for the catastrophic failure and long-term stress induced reliability problem. The proper algorithms to extract the lumped thermal elements with detailed information and effective convergence are highly demanded [109], [120]. On the other hand, the geometrical complexity of the multi-chip power modules defies the traditional thermal network concept, where the existing parameter extraction methods may not work properly. Examples of such problem include the DSC modules where the local thermal resistance cannot be represented properly [32] and the press-pack module where the contact thermal resistance may change with external clamp pressure [28]. In the DSC modules, the heatsinks on the two sides of the chips can be different, such as metal substrates (direct bonded copper, active metal brazing or

insulated metal substrate) and spacers, due to asymmetric designs. The interconnections on both sides can also vary from soldering to sintering materials, due to process limitations. The various materials used and CTE (coefficient of thermal expansion) mismatch conditions on the two sides of the chips lead to dissimilar degradation rates in terms of reliability, such that the top and bottom portions of the corresponding thermal networks evolve differently. In addition, due to the internal thermal dissipation path complexity, the T_j or T_c measurement cannot reflect the local thermal resistance change inside the DSC modules. Quantifying such degradation with the thermal network variation remains a challenge.

Fourth, the application of the thermal network in wide bandgap (WBG) and ultra-wide bandgap (UWBG) devices raises more challenges. On the one hand, these devices exhibit excellent performance under high power density and high-frequency operating conditions, but their thermal management has become a critical issue due to the high power and heat densities involved. The thermal network effectively simplifies the analysis of complex thermal systems and is well-suited for the thermal management of WBG/UWBG devices, but the accuracy and adaptability with high-frequency excitations should be carefully verified [205]. On the other hand, in compact power electronics systems with WBG and UWBG devices the multi-physics coupling effect becomes stronger, which calls for more accurate representations of the system by the developed thermal networks [206].

B. Future Opportunities

First, the compromise between the model comprehensiveness and simulation efficiency of the thermal network bears considerable optimisation potential. For one thing, most the current compromise has been established on the basis of existing software and hardware capabilities. As the modelling tool iterations and computational hardware configuration improves, the higher data processing capability will allow more sophisticated thermal networks to be implemented. At the same time, ideas of combining the distributed thermal network topology with reduced order modelling techniques, have been investigated to simplify the model while maintaining the accuracy of temperature estimation [207]. For another, the concept of multi-scale and multi-level thermal networks can be a promising solution to achieve good accuracy while limiting the computational power needed. For example, the multi-timescale Cauer thermal network model [42], [43], [208] can be adopted to the different switching modes of the power modules in power electronic systems. The multi-level thermal networks can also be adopted for detailed modelling considering module level and system level [106] or the chip level and module level [128]. Similarly, the Foster networks with different orders are combined with the quantitative error analysis to find the best discretisation number of the periodic power loss profile, which represents the minimum computational effort to achieve the maximum allowable error in the T_j estimation [204]. Those initiative work can be further developed to form a standard architecture with considerations of the application demands, the power loss profiles and fidelity requirements.

Second, a dedicated design and simulation platform for power module optimisation with the thermal networks is in need. As discussed, the multi-physics optimisation with the thermal networks for power modules is promising but lacks closed-loop methodology. A platform with an automated thermal network extraction procedure based on the 3-D physical structure, a cluster of multi-physics evaluation protocols with consideration of the application scenarios and a feedback loop to optimise the module design will be invaluable for power module development. Apart from the thermal networks, other reduced-order modelling techniques can also be integrated with consideration of different physical domains, to form efficient multi-physics evaluation and design iteration. Such tool will enable fast release of power module products while maintaining reasonable cost.

Third, the AI based numerical methods can be combined with the thermal networks modelling, where the physical implications of the latter can effectively enhance the accuracy and applicability of the former. Alongside with the development in power electronics technologies, the increasing availability of power module designs, thermal performance data and reliability records can provide larger set of training data for the ML based approach, such that the hybrid thermal networks can be derived effectively. Despite the few pioneering work being done in this area [127], more endeavour is needed to expand the application scenarios of the developed thermal networks and improve the ML models.

Fourth, the combination of thermal networks with other software tools or hardware setups represents a new trend. It will not only create adaptive topologies with the real-time power module status, but also enable the online system monitoring with fast response. Early-stage research work in this area includes the combination of the network topologies with the FEM simulation to form an interactive optimisation process of the former [209], the integration of a 2-D Cauer thermal network with a staggered cycle-by-cycle temperature calculation method for real-time application with acceptable lag [84] and the incorporation of additional temperature sensors to improve the temperature prediction accuracy during the power module application in the power electronic assemblies [147], [165]. While the ideas of software-in-the-loop or hardware-in-the-loop have been demonstrated in some specific case studies, future research opportunities rely on the novel integration methods, more efficient interaction and advanced sensor technologies.

Based on the above discussion, the proposed technology roadmap on future thermal network development can be seen in Fig. 7, where the current status and future development trend of thermal networks have been considered. Driven by the applications, the thermal network technology will develop towards multi-scale, higher accuracy, more AI involvement and more interaction with design optimisation.

VI. Conclusion

In this article, the historical development, current status and main trend of thermal networks for power semiconductor modules have been reviewed. Being initially introduced as analogy

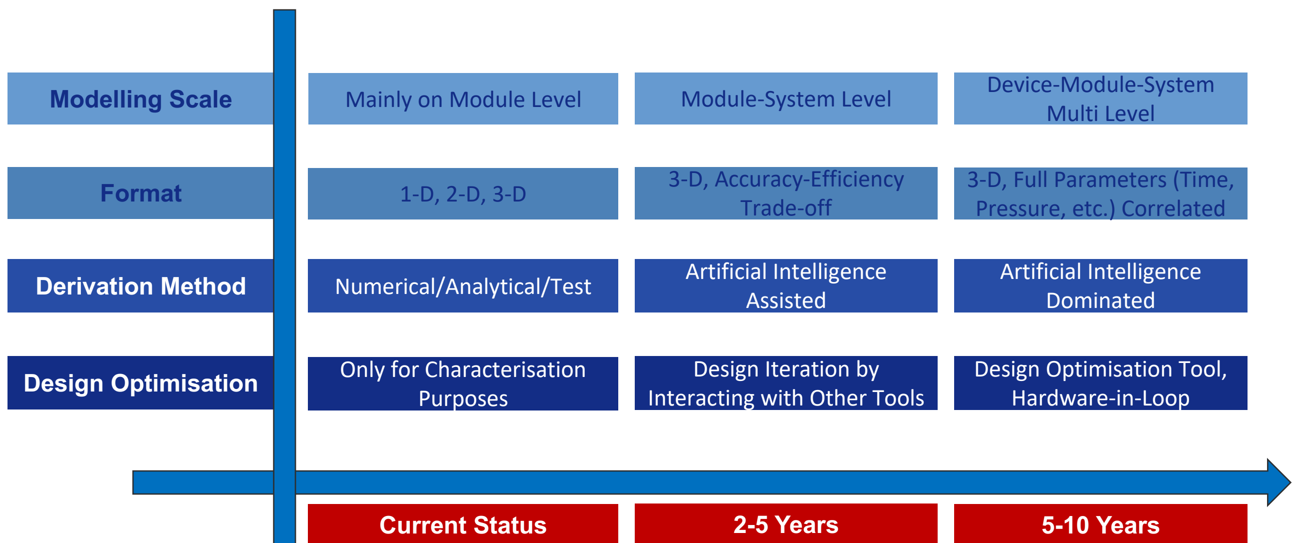

Fig. 7. Proposed technology roadmap for thermal network development, where the current status as well as the future trend in terms of modelling scale, format, derivation method and roles in design optimisation have been considered.

of the electrical circuits, the thermal network technologies have achieved tremendous developments, thanks to the booming of the power electronics for greener and more sustainable future of the human society. Moving forward alongside with the development of power modules for the power electronic systems, the thermal networks have evolved in the format, methodology as well as comprehensiveness, to achieve balance between the model complexity and computational cost. The satisfactory performance of the thermal network modelling in a broad range of applications, including thermal management, reliability assessment, multi-physics study and system status monitoring, has attracted considerable amount of research interests, by which a cluster of contributions from numerous research groups have been witnessed in this paper. The development of the thermal network technology is still far from the end of the journey, with both legacy and emerging challenges to be tacked. Having presented comprehensive summaries of the thermal network technologies in the fashion of comparison tables and representative cases, this article further provides visions of future research opportunities in the related field.

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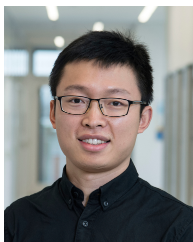

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