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Device Physics and Architecture Advances in Tunnel Field-Effect Transistors

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ABSTRACT

The persistent pursuit of miniaturization and energy efficiency in semiconductor technology has driven the scaling of complementary metal-oxide-semiconductor field-effect transistors (CMOS FETs, i.e., the MOSFETs) to their physical limits. Conventional MOSFETs face intrinsic challenges, especially the Boltzmann limit that imposes a fundamental lower bound on the subthreshold swing ($SS \geq 60$ mV dec^{-1} at room temperature). This limitation severely restricts voltage scaling and exacerbates static power dissipation. To overcome these bottlenecks, tunnel field-effect transistors (TFETs) have emerged as a promising post-CMOS alternative. The advantages of ultra-small *SS* well below the Boltzmann limit, as well as ultralow leakage currents, make TFETs ideal for low-power electronics and energy-efficient computing in the future information industry. However, its current development has encountered significant resistance to further performance improvement requirements; new breakthroughs have evolved to be based on interdisciplinary research that covers materials science, device technology, theoretical physics, and so on. Here, we provide a review on the design and development of TFET, which mainly describes the device physics model of tunnel junctions, and discusses the optimization direction of key parameters, the design direction of potential structures, and the development direction of the innovation system based on the device physics. Also, we visualize the framework for the figures of merit of TFET performance and further forecast the future applications of TFET.

1 | Introduction

1.1 | Fundamental Limitations Driving Beyond-CMOS Innovation

The evolution of conventional MOSFET technology has historically followed Moore's Law and Dennard scaling principles, achieving exponential performance improvements through dimensional scaling and supply voltage reduction. Over the past two decades, three key parameters—gate length, gate medium thickness, and junction depth—have all shrunk by about three orders of magnitude [1]. This technological breakthrough not only reflects the rapid development of the manufacturing process, but also directly promotes the substantial improvement of the power performance index. As Moore's Law continues to advance, chip manufacturers continue to reduce the size to improve integration and efficiency by optimizing transistor structures. For example, modern fin-type field-effect transistors (FinFETs), fully-depleted silicon-on-insulator (FD-SOI), and nanosheet transistors, are designed in response to this trend, which can effectively reduce leakage current and increase switching speed, thus achieving higher energy efficiency. In addition, advances in the field of materials science have also provided important support for these achievements, such as the

application of high dielectric constant materials that allow the gate dielectric layer to be thinner while still maintaining good insulation properties. In short, the rapid development of information technology depends on the joint advancement of interdisciplinary, including electrical and electronics, materials, theoretical physics, and even economics. These interdisciplinary research and development have jointly promoted the performance evolution and application development of commercial electronic equipment, laying a solid foundation for a more advanced information society in the future.

Most recently, although the iteration rate of commercial electronic devices is still fast, the impetus to continuously shrink in device dimension and power has been insufficient. Specifically, as device dimensions approach the sub-10 nm regime, three fundamental physical limitations have emerged. The first one is the power density crisis. At 5 nm technology nodes, static power dissipation from gate leakage and subthreshold conduction accounts for >40% of total power consumption. The International Roadmap for Devices and Systems (IRDS) projects that conventional CMOS scaling will lead to untenable power densities exceeding 500 W/cm^2 by 2030 [2]. Secondly, the short-channel effects (SCEs) proliferation is becoming a serious hindrance. Quantum tunneling through ultrathin gate dielectrics and drain-induced barrier lowering (DIBL) degrade switching characteristics, specifically the OFF-state current (I_{OFF}). For gate lengths below 12 nm, DIBL coefficients exceed 100 mV V^{-1}, causing unacceptable threshold voltage roll-off. The most direct way to solve these two problems is to continuously lower the supply voltage (V_{DD}); However, the third wall appears, and that is the thermodynamic barrier to subthreshold swing in MOSFET. In many studies, this wall has been described as "Boltzmann's tyranny" of thermionic emission, which mandates a minimum *SS* of 60 mV dec^{-1} at room temperature (RT) [3, 4]. This creates an exponential relationship between I_{OFF} and threshold voltage (V_{TH}), fundamentally limits MOSFET switching characteristics and severely constraining voltage scaling in advanced technology nodes. Therefore, the research for a steep slope transistor that can achieve RT *SS* well below 60 mV dec^{-1} has become the most critical pass to continue the Dennard scaling principles and Moore's Law; and specifically, the IRDS 2023 Edition has identified TFETs as the most promising "beyond CMOS" logic device with energy advantages that "moving close to the target" (Figure 1A).

1.2 | Development and Advantages of TFET Technology

The concept of band-to-band tunneling (BTBT) in semiconductor was proposed in the 1960s [5]. Early theoretical models established the *SS* advantage through Wentzel–Kramers–Brillouin (WKB) approximation [6]; Subsequently, a considerable amount of research on the subthreshold swing device physics has been deeply promoted. Further, the upsurge of research began with the experimental carbon nanotube TFET reported by Appenzeller et al. in 2004 [7]. A large number of studies have gradually mapped out a roadmap for the development of TFET, including material design and device structure development, as well as figures of merit for sub-Boltzmann-limit performance (Figure 1B–F). Detailed discussion of these aspects will be developed in the following sections. In short, material innovations including heterostructure engineering for broken-gap alignments, nanowire development for employing quantum confinement effects in ultrathin-body devices, novel 2D-material integration for interfacial, electrostatic, and band-alignment perfections, and so on were conducted in recent years to optimize the BTBT probability; at the same time, structure development, such as gate-all-around (GAA) structures for enhanced electrostatic control, negative-capacitance TFETs (NC-TFETs, using ferroelectric instead of conventional dielectric layers), and strain superlattices for efficient tunneling-barrier controls, was also promoted in pursuit of high-performance TFETs [8–13].

Early TFET research focused on three-dimensional (3D) bulk materials, such as Si, Ge, and III–V semiconductors, leveraging heterojunctions (e.g., InAs/GaSb, Ge/SiGe) to optimize tunneling efficiency. While these designs demonstrated improved *SS* values, they still faced critical limitations. For Si or Ge, their large effective carrier mass (m^*) and indirect bandgap reduce BTBT probability in related tunnel junctions, resulting in I_{ON} values orders of magnitude lower than the conventional MOSFETs. Several research have found that interface or lattice engineering may solve this problem to some extent [14, 15]; however, more research turned to develop III–V semiconductors, mainly based on the InAs family, with ultra-small m^* and ultra-narrow bandgap [16]. In this system, high tunneling probability can be easily demonstrated in theoretical physics model, but the practical experiment has suffered many obstacles. Firstly, InAs needs to be developed into heterojunctions because of its intrinsic narrow bandgap, but this brings problems of lattice mismatch at hetero-interface that introduces traps and degrading *SS* and current switching ratios. Secondly, nanoscale 3D material channels require additional techniques to improve gate control, such as thinning body-thickness and introducing GAA structures, but it may inadvertently increase bandgaps because of the quantum confinement effects, counteracting tunneling efficiency. These bottlenecks highlighted the need for innovative materials and structures beyond conventional 3D semiconductors.

The discovery of two-dimensional (2D) materials, such as graphene, transition metal dichalcogenides (TMDs), black phosphorus (BP), and indium selenide (InSe), has revolutionized TFET design. Their atomic thickness, pristine surfaces, and layer-dependent electronic properties offer unprecedented advantages [17, 18]. Firstly, 2D material enables superior electrostatic control. The quantum confinement inherent to atomically thin 2D semiconductors ensures that charge carriers are restricted to an ultrathin region, enabling uniform electrostatic modulation via the gate bias. These materials also exhibit inherently short screening (λ), a critical property for narrowing tunneling barriers and enhancing BTBT efficiency, which provides a direct consequence of steep subthreshold swing physics. Unlike conventional 3D systems (e.g., InAs heterostructures), the van der Waals (vdW) bonding between layers in 2D semiconductors eliminates interfacial dangling bonds and traps, preserving pristine heterojunction quality. Additionally, the layer-dependent bandgap tunability of these materials provides unparalleled flexibility in heterostructure band alignment engineering. Furthermore, the atomically precise thickness of 2D channels suppresses variations in layer uniformity, ensuring abrupt band edge transitions that sharpen the BTBT onset characteristics. Designing and fabricating 2D-material-based tunnel junctions seems to be an ideal solution for TFET development.

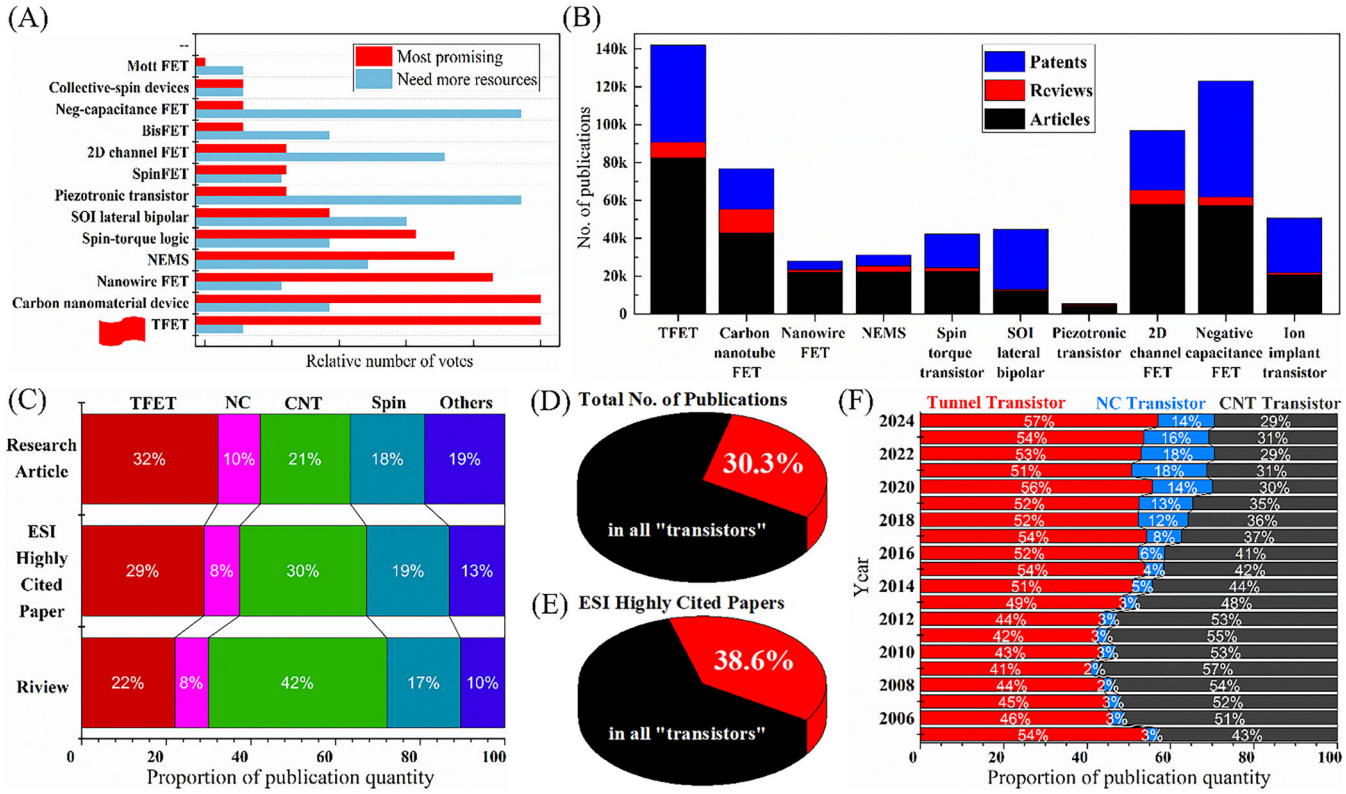

FIGURE 1 | A comparative analysis on the research value and attractiveness of TFET. (A) Vote results from the survey of Emerging Logic Devices in 2014 ERD Emerging Logic Workshop [2]. (B) Quantity of the publications, including research articles, reviews, and patents, regarding TFETs and other attractive beyond-CMOS transistors. KEY WORDS: "tunneling FET," "carbon nanotube FET," "nanowire FET -tunneling -carbon," "nano electro-mechanical switch," "spin torque transistor," "SOI lateral bipolar," "piezotronic transistor," "2D channel FET -tunneling," "negative capacitance FET -tunneling," "ion-implanted transistor." SEARCH ENGINE: Google Scholar. (C) Quantity proportion of specific papers, including research articles, reviews, and ESI highly cited papers, regarding TFETs and other attractive beyond-CMOS transistors. KEY WORDS: "tunneling transistor," "negative capacitance transistor," "carbon nanotube transistor," "spin transistor," "nano-electro-mechanical," "Mott transistor," "bilayer pseudospin," "ion implant transistor". The sum of search results for the last four keywords was used to analyze the term "others." SEARCH ENGINE: Web of Science. (D) Quantity proportion of publications, as well as (E) ESI highly cited papers, regarding beyond-CMOS transistors and all kinds of transistors. The KEY WORDS used for searching are the same as those in figure (C), but with the addition of "transistor" corresponding to all of its species. SEARCH ENGINE: Web of Science. (F) Annual statistics on the quantity proportion of publications regarding TFETs and two other most-attractive beyond-CMOS transistors. KEY WORDS: "tunneling transistor," "negative capacitance transistor," "carbon nanotube transistor." SEARCH ENGINE: Web of Science.

However, challenges still persist: (1) Controllable and large-scale growth of defect-free 2D layers and heterostructures remains elusive; (2) Contact resistance engineering at metal-2D interface is still a critical problem for every 2D-material-based device; (3) Last but most importantly, since 2D materials are not suitable for precise doping, finding reasonable heterostructures through material design and energy band engineering is the most critical step to achieve high-performance TFET based on 2D materials.

Although several published reviews have summarized the performance advantages of TFET and its development based on various material-systems, there is still a lack of systematic analysis and summary regarding the material design, device construction and architecture innovation of TFET that emphasizes the fundamental field of device physics. Therefore, we hope to provide a review to systematically analyze the evolution of advanced TFETs based on the subthreshold swing device physics, with a focus on design strategies, experimental milestones, and unresolved challenges. After the Introduction, we will devote a section to the device physics of TFET and the figures of merit in electrical performance, which is a key understanding for the design and development of TFET. Then, there will be two sections discussing the advanced research of high-performance TFET, focusing respectively on the traditional 3D-nanowire TFETs and the emerging 2D-material TFETs. At the end, there is a summary and outlook section, and the practical applications of TFET are further discussed. By bridging material innovation with device physics, we aim to provide a constructive development framework for realizing high-performance TFETs in the post-Moore era.

2 | Understanding and Design of High-Performance TFETs

2.1 | Subthreshold Swing Physics in MOSFETs

The fundamental performance constraints of conventional FETs originate from the inherent physics governing carrier injection mechanisms. In MOSFETs, the subthreshold current

transport is dominated by thermionic emission, where charge carriers (electrons or holes) must acquire sufficient thermal energy to surmount the energy barrier modulated by the gate voltage (V_g). This process adheres strictly to the Boltzmann statistics of carrier distribution, resulting in an exponential dependence of drain current (I_{DS}) on V_g in the subthreshold regime [19]:

$$I_{DS} \propto e^{\frac{qV_g}{nk_BT}}, \tag{1}$$

where q is the elementary charge, k_B is the Boltzmann constant, T is the absolute temperature, and n (ideality factor) represents the capacitive coupling efficiency between the gate and channel, defined as $n = 1 + C_{ox}C_d$. Here, C_{ox} is the gate oxide capacitance, and C_d accounts for depletion and interface trap capacitance. The *SS*, defined as the V_g required to increase the drain current by one decade, is derived from this exponential relationship [19]:

$$SS = \frac{dV_g}{d(\log I_{DS})} = \ln(10)\frac{nk_BT}{q}. \tag{2}$$

The theoretical minimum *SS* of 60 mV dec^{-1} (when $n = 1$) represents a thermodynamic limit imposed by the Fermi–Dirac distribution of carriers, a phenomenon often termed "Boltzmann tyranny." This constraint arises because the probability of carriers overcoming the channel barrier decreases exponentially with the barrier height, leading to an inherent trade-off between switching speed (steep *SS*) and leakage current (Figure 2A) [9].

Recently, the most advanced transistors are close to perfectly implementing $SS = 60$ mV dec^{-1}. While advanced transistor designs such as FinFETs and FD-SOI devices have improved electrostatic control by reducing SCEs and minimizing C_d, they remain fundamentally constrained by the Boltzmann limit [20]. For instance, FinFETs leverage 3D gate wrapping to enhance C_{ox}, thereby lowering n to near-ideal values (~1.0). Similarly, FD-SOI architectures employ ultra-thin body channels to suppress parasitic capacitance. However, as CMOS technology approaches the sub-5 nm regime, the Boltzmann limit becomes a critical bottleneck for power efficiency. Specifically, lowering V_{DD} below 0.5 V, which is a practical requirement that has been largely touched upon, severely compromises the I_{ON} and transistor drive capability, necessitating unrealistically steep *SS* values (<60 mV dec^{-1}) to preserve performance, that is, a feat unattainable with conventional thermionic switches. This mandates structural innovations in transistor design to circumvent the Boltzmann limit for future low-power electronics. While advanced architectures mitigate practical non-idealities, they cannot overcome the intrinsic 60 mV dec^{-1} *SS* limit, necessitating exploration of beyond-CMOS technologies for continued progress in semiconductor scaling (Figure 2B) [9].

2.2 | Subthreshold Swing Physics in TFETs

TFETs represent a paradigm shift in carrier injection physics by exploiting quantum mechanical BTBT to circumvent the Boltzmann limit inherent in conventional FETs. Unlike thermionic emission, where carriers require thermal energy to surmount a potential barrier, BTBT enables direct tunneling of carriers between energy bands under the influence of a strong electric field [21, 22]. This mechanism fundamentally decouples carrier statistics from the Boltzmann distribution, enabling *SS* values below 60 mV dec^{-1} at room temperature (Figure 2C,D).

Take a prototypical p-type TFET as an example, a p–i–n heterostructure is employed, where the source is heavily n-doped, the channel is intrinsic (or lightly doped), and the drain is heavily p-doped. Under reverse bias, the energy bands in the source and channel regions align to create a tunneling junction. The V_g modulates the channel potential, thereby controlling the tunneling window, that is, the energy overlap between the source valence band and the channel conduction band. The tunneling probability is governed by the WKB approximation [23, 24]:

$$T_{WKB} \approx \exp\left(-\frac{4\lambda \cdot \sqrt{2m_T^*} \cdot E_g^{\frac{3}{2}}}{3q\hbar F}\right), \tag{3}$$

where λ is the effective screening length, m_T^* is the effective carrier mass, E_g is the material bandgap, $\hbar$ is the reduced Planck's constant, F is the electric field across the tunneling junction. Specifically, $F = E_g + \Delta\varphi$, and $\Delta\varphi$ is the energy gap between the source valence-band-maxima (VBM) and the channel conduction-band-minima (CBM), that is, the BTBT energy window. Crucially, the BTBT process exhibits an exponential dependence on F and E_g, but only a weak temperature dependence, bypassing the thermal injection constraints of conventional FETs.

The subthreshold behavior of TFET is fundamentally governed by the BTBT mechanism, which displays a hyper exponential V_g dependence of tunneling probability as described by Equation (3). This characteristic arises from the energy band alignment optimization at the tunnel junction, where a bandgap configuration exceeding the valence band maximum decouples electron population in the source valence band from thermal Fermi–Dirac distribution tail. These phenomena collectively enable TFETs to surpass the Boltzmann limit, achieving sub-60 mV dec^{-1} *SS* through quantum mechanical carrier injection rather than thermionic emission. Nevertheless, a comprehensive *SS* analysis becomes imperative to establish design parameters for TFETs exhibiting sub-thermal swing characteristics of <60 mV dec^{-1}. To systematically analyze *SS* and establish design guidelines for sub-thermal TFETs, five critical approximations form the theoretical framework for nanoscale device modeling [25, 26]:

1. Structural Configuration: the prevalent double-gated n-channel architecture with intrinsic channel doping optimizes electrostatic control while minimizing interface-trap density D_{it}, a configuration validated in advanced FinFET and nanosheet TFET designs.
2. Transport Physics: current conduction follows Landauer's formalism under ballistic/quasi-ballistic conditions, essential for accurately modeling carrier injection in sub-100 nm channel devices where scattering events become negligible.

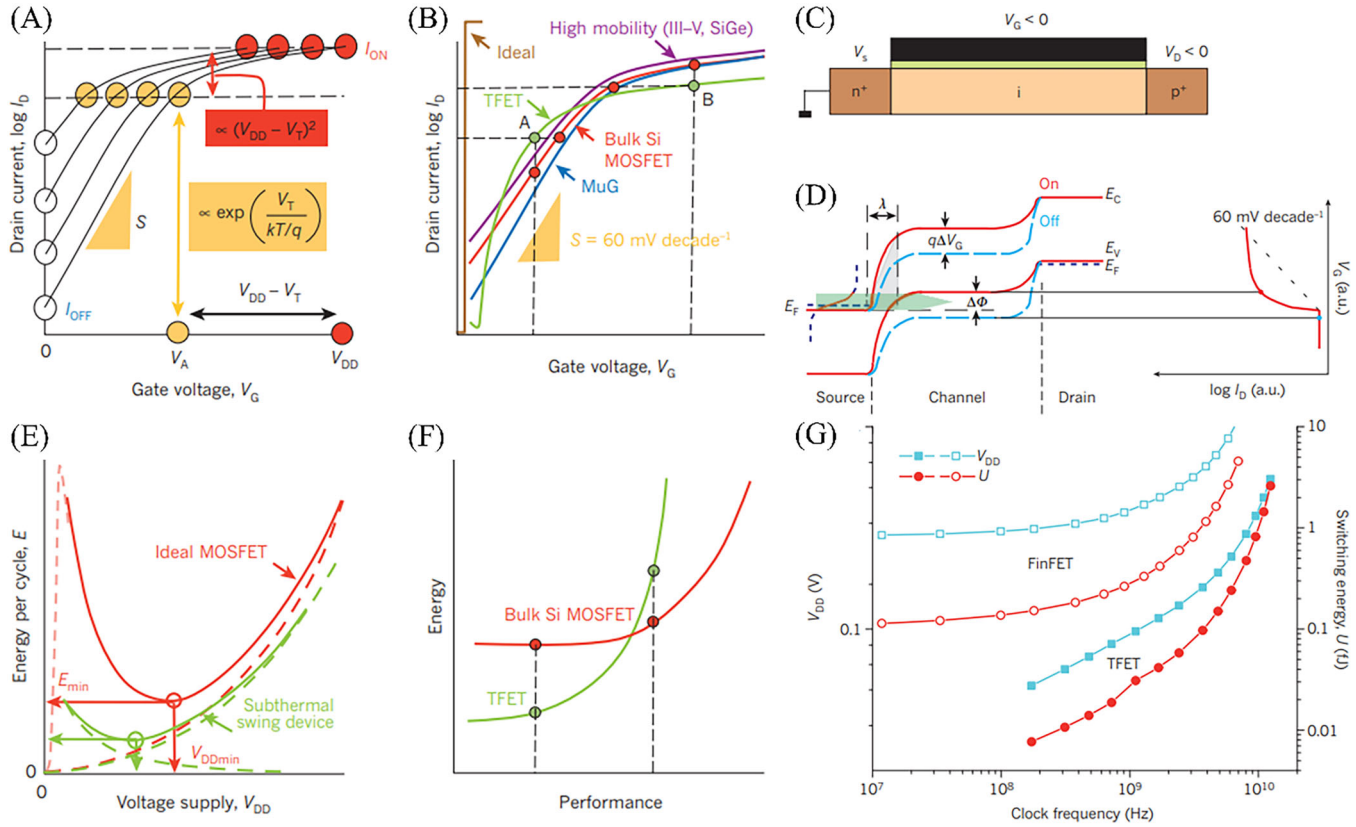

FIGURE 2 | TFET as a promising alternative to CMOS transistors: principle and characteristics. Reproduced with permission [9]. Copyright 2011, Springer Nature. (A) Transfer behavior of a MOSFET under voltage scaling reveals exponential I_{OFF} escalation due to fundamental *SS* limitations. Proportional reduction of V_{DD} and threshold voltage V_T preserves operational current (I_{ON}) through maintained overdrive potential (V_{DD}-V_T). (B) Comparative analysis of three MOSFET enhancement strategies: multi-gate architectures (blue) enhancing electrostatic control; high-carrier-mobility channels (purple) improving output level; and tunnel FETs (green) demonstrating abrupt switching transitions with minimized leakage currents. (C) Cross-sectional illustration of a p-TFET highlighting voltage-biased source (V_S), gate (V_G), and drain (V_D) terminals. (D) Energy band alignment diagrams contrasting OFF-state (dashed) and ON-state (solid) configurations in p-TFET operation. BTBT initiates when the gate-modulated energy window $\Delta\varphi$ (shaded region in green) enables charge injection across the barrier. Unlike conventional MOSFETs, TFET current characteristics exhibit nonlinear logarithmic dependence due to quantum tunneling probability and Fermi-level density-of-states constraints. The tunneling mechanism approximates to a triangular barrier model (gray overlay). (E) Minimum switching energy (E_{min}) versus optimized supply voltage (V_{DDmin},) comparison between theoretical TFET and MOSFET at equivalent I_{ON}/I_{OFF} current ratios. (F) Energy-performance comparative-analysis demonstrating TFET's superior efficiency at moderate throughput requirements versus MOSFET dominance in high-performance regimes. (G) System-level simulation of scaled InAlAs/GaAlSb TFET (solid markers) versus 20-nm FinFET (open markers) under power-constrained multi-core architecture (24 M transistors). Voltage-frequency co-optimization reveals TFET advantages through adaptive parameter tuning of V_{DD}, V_T, source Fermi level (V_e), and dimensional scaling while maximizing clock frequency under thermal budgets.

3. Tunneling Probability Homogeneity: the WKB tunneling probability remains approximately constant within narrow energy windows ($\Delta\varphi \approx$ few kT), valid for subthreshold operation where gate modulation primarily affects band alignment rather than tunneling path geometry.
4. Source-Drain Asymmetry: the Fermi–Dirac distribution contribution becomes insignificant in the tunneling window due to substantial drain-source potential differences (>0.1 V), enabling simplified current modeling focused on source-side injection characteristics.
5. Electrostatic Length Quantification: minimum tunneling length derivation employs one-dimensional (1D) Poisson solutions under Yan's parabolic potential approximation combined with Kane's two-band model, a methodology successfully applied in heterojunction TFET optimization.

When employing a fixed V_g, that is, a controlled $\Delta\varphi$, the tunnelling probability can be expressed based on Yan's parabolic approximation in FET compact modelling:

$$T_{\Delta\varphi} \approx \exp\left(-\pi \cdot \sqrt{2E_g m_T^*} \cdot W_{Tunn}/4q\hbar\right), \quad (4)$$

where W_{Tunn} is the minimum tunnelling width crossing the junction. Further, according to the Landauer's formalism, the tunnelling current density within the junction region can be defined as:

$$I_T = \frac{2q}{h} \cdot T_{\Delta\varphi} \cdot F_{Integral}, \quad (5)$$

where $F_{Integral}$ is the integral of the Fermi–Dirac distribution function of carriers:

$$F_{\text{Integral}} = k_B T \cdot \ln\left(\frac{1 + \exp\left[\frac{(E_{F,s} - E_{V,s} + \Delta\varphi)}{k_B T}\right]}{1 + \exp\left[\frac{(E_{F,s} - E_{V,s})}{k_B T}\right]}\right). \quad (6)$$

Here, $E_{F,s}$, $E_{V,s}$, are the Fermi level and VBM in source end, respectively. These approximations collectively define the *SS* through the relationship through a dual-component model expressed as:

$$SS = \left(\frac{d(\Delta\varphi/q)}{d\log_{10} I_T}\right) = [(SS_T)^{-1} + (SS_{FD})^{-1}]^{-1}, \quad (7)$$

where SS_T reflects V_g-induced band alignment modulation:

$$SS_T = \left(\frac{d(\Delta\varphi/q)}{d\log_{10} T_{\Delta\varphi}}\right) = \frac{(2\sqrt{2}\ln 10)\cdot\hbar}{-q\pi\cdot\sqrt{E_g m_T^*}}\cdot\frac{d\Delta\varphi}{dW_{\text{Tunn}}}, \quad (8)$$

and SS_{FD} arises from the energy separation between the $E_{V,s}$ and $E_{F,s}$:

$$SS_{FD} = \left(\frac{d(\Delta\varphi/q)}{d\log_{10} F_{\text{Integral}}}\right) = \frac{k_B T\cdot\ln 10}{q} \cdot(1 + \exp[(E_{V,s} - E_{F,s} - \Delta\varphi)/k_B T]) \cdot\ln\left(\frac{1 + \exp[(E_{F,s} - E_{V,s} + \Delta\varphi)/k_B T]}{1 + \exp[(E_{F,s} - E_{V,s})/k_B T]}\right). \quad (9)$$

The analytical framework established by Equations (3–9) provides a comprehensive methodology for evaluating *SS* in TFETs across both nanoscale bulk semiconductor and 2D material implementations [23]. At the tunneling initiation threshold ($\Delta\varphi \approx 0$), the $[SS]_{FD}$ component theoretically approaches near-zero values due to minimized Fermi–Dirac distribution broadening. However, practical device operation in this regime becomes fundamentally limited by extraneous conduction mechanisms, including reverse-bias junction leakage and trap-assisted tunneling (TAT) currents arising from interface defects [27]. Consequently, the effective *SS* minimum manifests at finite tunneling energy windows ($\Delta\varphi \approx kT$), where SS_T dominates through its dependence on gate-modulated band alignment.

The pursuit of optimal TFET performance has centered on reconciling two conflicting objectives: maximizing I_{ON} while minimizing *SS* across multiple decades of subthreshold operation [28]. The enhancement of I_{ON} in TFETs necessitates maximization of BTBT probability under minimal gate voltages, a requirement fundamentally governed by three parameters: effective tunneling mass m_T^*, energy bandgap E_g, and electrostatic screening length λ. A smaller λ represents superior gate control over tunneling junction electrostatics. Minimizing λ, that is, achieved through gate dielectric thickness scaling (<2 nm) or high-κ material integration (HfO_2, Al_2O_3), strengthens gate field penetration at the tunneling junction, enabling precise electrostatic control. Concurrent elevation of source doping concentration N_A induces degenerate band bending, further compressing λ through enhanced carrier confinement. m_T^* is determined by the geometric meaning of valence (m_V^*) and conduction (m_C^*) band effective masses, which can benefit from heterostructure engineering. In contrast, E_g optimization requires strategic source material selection, with narrow-bandgap semiconductors (Ge, InSb) reducing tunneling barrier heights while introducing challenges in off-state leakage management.

The inherent trade-off between *SS* minimization and I_{ON} enhancement in TFETs arises from competing physical dependencies in device operation as shown in Equations (3–9). For instance, while reduced E_g and m_T^* improve tunneling probability (T_{WKB}) to elevate I_{ON}, these modifications simultaneously amplify the gate sensitivity of band alignment modulation ($[SS]_T$), thereby degrading *SS*. Similarly, strategies to enhance electrostatic control through increased N_A and reduced λ shorten tunneling distance (W_{Tunn}) to boost T_{WKB} yet induce excessive band bending that strengthens electrostatic screening. This screening effect restricts the $\Delta\varphi$-dependent tunability of W_{Tunn}, ultimately compromising *SS* through diminished $\partial\Delta\varphi/\partial V_g$ response.

The intricate interdependence between electrostatic and material parameters in governing I_{ON} and *SS* necessitates balanced optimization strategies for TFETs. Achieving this equilibrium requires systematic co-engineering of device architecture and material properties, particularly focusing on three critical aspects: doping gradient precision at tunneling junctions, optimized gate dielectric configurations, and strategic selection of semiconductor materials with tailored electronic characteristics. While reduced carrier effective mass and narrow bandgap materials demonstrate potential for enhancing tunneling probability, their excessive minimization introduces detrimental tradeoffs.

Also, the ultra-low effective masses paradoxically diminish the density of available quantum states in both conduction and valence bands, potentially degrading the I_{ON}/I_{OFF} ratio through constrained tunneling pathways. Concurrently, extreme bandgap narrowing in source regions promotes significant BTBT leakage currents, exacerbating I_{OFF} degradation and consequently compromising subthreshold operational integrity. These phenomena collectively underscore the nontrivial nature of TFET performance optimization, where quantum mechanical transport mechanisms impose strict boundaries on material parameter selection. The design paradigm therefore emphasizes synergistic adjustments across multiple device domains rather than unilateral parameter optimization, requiring meticulous consideration of interdependencies between quantum confinement effects, band structure engineering, and electrostatic control methodologies.

2.3 | Figures of Merit in TFET Performance

The viability of high-performance TFETs hinges on optimizing four critical metrics:

1. *SS* Features: governs switching abruptness. Critical requirements include a minimum *SS* (SS_{min}) ≤ 40 mV dec^{-1}, as well as an average *SS* (SS_{avg}) ≤ 60 mV dec^{-1} across a rational range of subthreshold current span > 4 orders of magnitude

($I_{sub\text{-}ratio} > 10^4$). Superior switching necessitates sustained SS_{avg} performance rather than isolated SS_{min} improvements, as steep SS degradation nullifies subthreshold advantages despite low SS_{min}.

2. On-State Current (I_{ON}): determines operational speed. A subthreshold figure of merit, I_{60}, representing the BTBT current at which SS remains sub-60 mV dec^{-1} (@ 300 K), serves as a standardized metric. I_{60} exhibits saturation under moderate lateral fields (~1×10^5 V cm^{-1}) and correlates with SS_{avg} stability and high I_{ON}/I_{OFF} ratios. Competitiveness with MOSFETs mandates I_{60} to be at least within 1–10 μA/μm region (for low-power devices) or even higher (for high-output circuits), normalized to equivalent drain-field conditions ($V_{DS}/L_{ch} = 1 \times 10^5$ V cm^{-1}) to decouple drain-bias dependencies.

3. I_{ON}/I_{OFF} Ratio: essential for noise immunity. For low-power applications, normally a current-switching ratio over 10^5 is required. Unless TFET can raise the I_{ON} to the operating range of high-performance CMOS (HP-CMOS, perhaps greater than 10 mA μm^{-1}), it is necessary to demonstrate a considerable I_{ON}/I_{OFF} ratio.

4. Dynamic Performance: power-delay product (PDP, estimating the switching energy of transistor) and intrinsic delay (τ) are primarily governed by gate capacitance (C_g) and I_{ON} [29]:

$$\tau = \frac{C_g V_{DD}}{I_{ON}}, \tag{16}$$

$$PDP = C_g V_{DD}^2. \tag{17}$$

V_{DD} downscaling coupled with I_{ON} increasing and C_g lowering enables simultaneous power reduction and speed improvement. C_g minimization requires synergistic optimization of gate stack design (e.g., dielectric scaling, quantum capacitance modulation), drain doping gradients, and channel (or structural) material selection. Device engineering must therefore address both electrostatic control and quantum transport limitations to advance TFET circuit viability.

These criteria underscore the necessity for material-to-device interdisciplinary optimization to balance steep switching, current drive, leakage suppression, and dynamic efficiency in TFET designs. In Table 1, we summarize these important performance indicators and list the advanced results in various types of reported TFETs [30–37]. It should be noted that in the existing TFET studies, PDP and τ have not been widely valued; in the vast majority of reports, quantitative tests on these two indicators have not been conducted yet. Hence, we have not included these two indicators for the time being in Table 1.

2.4 | Benchmarking of TFET and Other Transistors

TFETs exhibit several advantages over traditional CMOS transistors. One of the most notable benefits is their ability to operate at significantly lower supply voltages. Unlike CMOS, which requires higher voltages to ensure sufficient turn-off of the transistor and suppress standby power dissipation, TFETs utilize BTBT to achieve efficient switching at low voltages, as summarized in Table 2 and Figure 2E–G [4, 9]. Additionally, TFETs exhibit a smaller gate capacitance due to gate-drain underlaps, contributing to faster switching times and lower power consumption. The negative differential resistance (NDR) characteristic of TFETs also provides unique advantages in designing low-power logic circuits, allowing for more flexible and efficient circuit designs.

In terms of circuit area, TFETs demonstrate competitive performance with CMOS. The area of a TFET inverter with a fan out of 4 is calculated to be comparable to that of a CMOS inverter, despite the additional complexity of the TFET structure. This is attributed to the smaller gate capacitance and the efficient use of space in TFET designs. For more complex circuits like 32-bit adders, the area overhead of TFETs remains manageable, making them suitable for integration into larger systems. The energy-delay product (EDP), a key metric for evaluating the efficiency of logic devices, is found to be significantly lower for TFETs compared to CMOS. This is primarily

TABLE 1 | Figures of merit of high-performance TFET and the advanced results in various types of tunnel junctions.

Junction	Type	SS_{min} (mV dec^{-1})	SS_{avg} (mV dec^{-1})[a]	I_{60} (μA/μm)[b]	I_{ON}/I_{OFF}	Ref.
—	Figures of merit	<< 40 Prefer Smaller	<< 60 Prefer Smaller	> 1 Prefer Higher	> 10^5 Prefer Lager	—
Si	3D nanowire	30	50	0.001	10^4	[30]
InAs/GaSb	3D heterojunction	50	59	~1	10^6	[31]
InGaAs/InAs	3D heterojunction	55	60	0.008	> 10^5	[32]
Ge/MoS_2	2D/3D mix-dimensional	~5	30	0.001	10^{10}	[33]
Si/InSe	2D/3D mix-dimensional	~5	10	~0.1	10^5	[34]
$MoTe_2$	2D homojunction	30	50	—	10^7	[35]
BP	Bulk-monolayer junction	20	30	~1	10^6	[36]
$WSe_2/SnSe_2$	2D heterojunction	20	60	—	> 10^5	[37]

[a]Calculated within the switching current range of more than three orders of magnitude.
[b]Normalized @ $V_{DD} = 1$ V.

TABLE 2 | Benchmarking on 32-b adders based on TFETs and conventional MOSFETs.

Parameter	TFETs	High-performance CMOS	Low-power CMOS
Supply Voltage (V_{DD})	0.2–0.4 V	0.73 V	0.3 V
Drive Current (I_{ON})	25–500 A/m	1805 A/m	2 A/m
Switching Energy	0.15–0.59 fJ	2.48 fJ	0.42 fJ
Switching Delay	138–1378 ps	84 ps	31,331 ps

TABLE 3 | Benchmarking on TFETs and other beyond-CMOS devices.

Device	Supply voltage (V)	32-bit Adder area (F^2)	Intrinsic delay (ps)	Switching energy (aJ)	Power density (W/cm^2)	Throughput ($PIOPS/cm^2$)
TFET Family						
HomJTFET	0.2	373,250	3.27	0.98	0.1	0.86
HetJTFET	0.4	373,250	0.33	3.93	5.1	8.64
gnrTFET	0.25	373,250	0.79	1.53	0.8	3.60
Other Beyond-CMOS Devices						
GpnJ	0.7	207,360	2.17	142.77	301.5	19.47
BisFET	0.6	454,900	1.36	22.10	5.8	1.92
SpinFET	0.7	279,940	1.02	30.08	18.0	5.63
STT/DW	0.01	30,240	1762.9	111.06	6.5	0.13
SMG	0.01/0.1	13,824	297.61	1.38	0.3	0.84
STTtriad	0.01	165,240	298.03	10.92	0.3	0.02
STOlogic	0.01	27,648	1000	351.60	23.5	0.23
SWD	0.01/0.1	9216	297.61	1.38	1.1	3.99
NML	0.01/0.1	4608	400	19.31	3.1	2.51
ASLD	0.01	9216	205.16	108.20	38.2	1.84

due to the reduced switching energy and faster switching times of TFETs at low supply voltages. For example, a 32-bit adder implemented with TFETs can achieve an EDP of approximately 20.7 fJ·ps, which is at least an order of magnitude lower than that of CMOS-based adders under similar operating conditions.

Moreover, TFET demonstrates distinct advantages and trade-offs when quantitatively compared to alternative beyond-CMOS logic devices, as evidenced by standardized metrics stated in Table 3 [4]. Homojunction TFETs (HomJTFET) and graphene-nanotube TFETs (gnrTFET) achieve the lowest switching energy among all evaluated devices at 0.2 V, outperforming graphene pn-junction (GpnJ) devices and approaching the energy efficiency of voltage-controlled spintronic devices like spin wave devices (SWD). However, TFETs suffer from area penalties due to doping isolation requirements, with 32-bit adder areas (373,250 F^2) nearly 1.8× larger than GpnJ and 12× larger than nanomagnetic logic (NML). Heterojunction TFETs (HetJTFET) address speed limitations of HomJTFET, reducing intrinsic delay from 3.27 ps to 0.33 ps at 0.4 V, rivaling CMOS HP (0.25 ps) but at the cost of higher energy (3.93 aJ vs. CMOS HP: 19.63 aJ).

Spintronic devices exhibit divergent performance profiles. While spintronic majority gate (SMG) and spin torque triads (STTtriad) achieve ultra-low energy, its delay renders it impractical for high-speed applications compared to HetJTFET. Spin-transfer torque domain wall (STT/DW), spin torque oscillator (STO) logic, and all-spin logic (ASLD) show moderate energy but suffer from latency exceedingly even HomJTFET's circuit-level delay. NML and SWD leverage voltage-controlled operation to minimize energy, yet their delays remain orders of magnitude higher than TFET variants. On the other hand, bilayer pseudospin FETs (BisFETs), though theoretically promising with 1.36 ps delay and 22.10 aJ energy, face unresolved scalability challenges, as their 32-bit adder area exceeds TFETs by 22%. Also, spinFETs, hybrid CMOS-magnetic devices, mimic conventional transistor speeds but incur higher energy than HetJTFET.

In summary, TFETs occupy a unique niche, combining near-CMOS speeds with ultralow energy consumption, albeit constrained by area inefficiencies. TFETs offer compelling advantages for low-power and low-voltage applications, with significant improvements in switching energy, delay, and EDP compared to traditional CMOS transistors. While spintronic alternatives excel in nonvolatility or functional density, their reliance on slow magnetization dynamics and peripheral circuitry limits competitiveness in conventional logic. Experimental validation of TFET heterostructures and doping techniques remains critical to closing

the performance gap with CMOS while retaining energy advantages. However, their adoption is tempered by manufacturing complexities and performance limitations in high-speed contexts. As research continues to advance material science and device physics, TFETs and other beyond-CMOS devices are expected to play increasingly important roles in the evolution of integrated circuits, potentially leading to new paradigms in computing technology. The ongoing optimization of TFETs, alongside the exploration of novel materials and architectures, is anticipated to address current limitations and further enhance their competitiveness in the nanoelectronics landscape.

2.5 | Designing High-Performance TFETs Based on Device Physics

The development of TFETs into mainstream semiconductor technology requires a systematic roadmap addressing material innovation, device architecture optimization, and fabrication advancements. Below, we will briefly draw a roadmap for the future development of TFET, and expand on these synergistic strategies, supported by recent breakthroughs and computational insights. A detailed discussion will be carried out in the following chapters. First of all, the most important part of TFET research is the design of efficient tunnel junctions. According to the subthreshold swing device physics we discussed in the early section, the most critical pass arises in the innovation on junction materials exhibiting ultra-low effective carrier mass (m^*), ultra-narrow bandgap, and high mobility. Carriers with low m^* exhibit higher tunneling probabilities due to reduced tunneling distance. On the other hand, the tunnel junction may be optimized through strain engineering, for example, the uniaxial tensile strain is suggested to reduce E_g and m^* simultaneously in some materials. Strain gradients may also suppress ambipolarity by selectively modulating band alignment at source/drain interfaces. In addition, emerging 2D materials may also provide effective assistance for the design of efficient tunneling junctions. Notably, what is referred to here is not the direct use of 2D materials for the construction of tunneling junctions, but the use of interlayer screening effects in vdW stacked 2D materials to achieve unprecedented electrostatic control. In this regard, challenges include interlayer contamination and thermal resistance at heterointerfaces. Initial attempts at van der Waals integration centered on depositing high-κ dielectrics onto sensitive channel materials to form interfaces with minimal chemical disorder and trap states, which are crucial for effective electrostatic gating [38]. This methodology extends beyond passive dielectric integration to enable active current-carrying junctions through lithographically patterned metal electrodes transferred onto two-dimensional semiconductors. Such interfaces achieve near-ideal characteristics: atomic cleanliness and Fermi-level pinning suppression allow operation approaching the Schottky-Mott theoretical limit, a benchmark challenging to attain in conventional metallization schemes [39]. These pinning-free van der Waals contacts can be harnessed to create highly efficient photodiodes with minimal interfacial recombination and near-perfect internal quantum efficiency, offering valuable insights into the development and application of emerging TFET devices [40].

In addition to material science, device physics is also an important optimization direction for TFETs. First, also derived from the understanding of the physical formula of step-slope devices, improving the control ability of the gate electrostatic field is the most critical step. Prominent structural schemes include the GAA structure, as well as multi-gate designs, in which the dual- or triple-gate architectures decouple control of tunneling and transport regions. On the other hand, innovative device theory or structure may further broaden the development path of TFET. Dirac-source (DS) configurations or NC integrations are admirable examples in this direction, but key challenges include minimizing hysteresis and ensuring ferroelectric phase stability under cycling. Further, the fabrication technologies of both materials and devices also play a significant role in demonstrating high-performance TFETs. Due to the limitations of 3D-InAs system in the development of TFET, the most widely concerned research direction has shifted to 2D materials. However, the large-scale preparation and stability of high-quality 2D materials and vdW heterostructures has not yet been effectively solved, and this will be one of the most important technical cornerstones. In addition, precise doping of 2D materials could also be a valuable technique. On the other hand, innovations on device fabrication are also required because the biggest disadvantage of TFETs is that the output current level is insufficient. Selective edge-bonded metal contacts may bypass Schottky barriers in 2D materials, which is conducive to the increase of currents. It should be noted that although TFET based on traditional 3D materials has encountered a relatively obvious development bottleneck, many innovative works are still emerging in an endless stream. On the other hand, although TFET based on novel 2D materials shows great development potential and theoretically ideal properties, practical experimental results have yet to demonstrate convincing performance. Therefore, in the next two sections, we will review the research reports of TFET based on the most advanced 3D nanowires, and TFET based on the emerging 2D materials, respectively, summarizing their development and prospects.

TFETs offer a compelling pathway to overcome the Boltzmann tyranny by leveraging quantum mechanical tunneling. While their sub-60 mV dec^{-1} *SS* and ultra-low I_{OFF} are transformative for energy-efficient electronics, practical adoption hinges on resolving material and design challenges. The subthreshold physics of TFETs underscores the interplay between quantum tunneling, material interfaces, and band structure engineering. Advances in low-dimensional materials and heterostructure design have enabled *SS* values approaching 25 mV dec^{-1}, yet practical deployment demands solutions to synthesis, variability, and integration challenges. The TFET roadmap highlights a codesign philosophy integrating novel materials, advanced device architecture, and atomic-scale fabrication. While Technology Computer Aided Design (TCAD) projections are promising, bridging the gap to commercialization demands solutions to variability, thermal stability, and integration complexity. Notably, machine learning may drive the design of TFETs: establishing the library of tunnel junctions will be helpful to further explore the optimal design strategy. With sustained innovation, TFETs could redefine energy-efficient computing, enabling sub-0.5 V operation for internet of things (IoT), artificial intelligence (AI), and future beyond-Moore technologies.

3 | Heteroepitaxial Nanowire TFETs

The earliest studies of TFET started from the homojunction of Si or Ge, which was controlled by doping to form the tunnel junction. However, despite structural advancements, Si-based TFET implementations exhibit generally compromised performance metrics. For example, an advanced Si-TFET with a 2-nm gate oxide and a 70-nm SOI layer still has an I_{ON}/I_{OFF} ratio significantly inferior to conventional MOSFETs. Researchers believe that reducing the thickness of the gate oxide and SOI layer, employing smaller bandgap channel materials, and engineering an abrupt source doping gradient are predicted to boost I_{ON}/I_{OFF}. In particular, steep source doping profiles can increase I_{ON} by reducing the tunneling barrier width [41]. Experimental implementations using SiGe/Ge sources and steep doping implants have yielded measurable improvements in SS and drive current [42]. However, these approaches still fall below the driving capability required for high-performance circuits. A large number of device physics studies have shown that the tunneling probability in TFETs depends exponentially on the sharpness of the doping profile at the source–channel interface [21, 22, 43]. The abrupt junction (doping gradient <3 nm dec^{-1}) concentrates the electric field (F) at the tunnel junction, maximizing the BTBT probability. Due to the transverse dispersion and segregation of dopants, it is difficult for conventional implantation or diffusion based doping techniques to achieve such abruptness. In this regard, heterojunctions can provide the perfect solution [44–46]. Therefore, in this review, we will skip the discussion of graded doping junction and start with the heterojunction systems based on heteroepitaxial nanowire that have become the most mainstream research direction in the past decade. Heteroepitaxial nanowire TFETs leverage atomic-level interface engineering to optimize tunneling efficiency through precise control of lattice matching and band alignment. Recent advancements in material systems and quantum confinement effects have enabled breakthroughs in both performance and scalability.

3.1 | Design of Material System: Epitaxial Lattice and Band Structure

InAs was discovered in the study of TFET architecture because it presents the optimal solution so far for the requirements of ultra-small m^* and ultra-narrow bandgap. At the same time, as a member of group III–V semiconductors, it can be built into high-quality heterostructures with many other lattice-matched semiconductors, such as GaSb, through a mature heteroepitaxy technology system, and show abrupt junctions for carrier tunneling (Figure 3A) [31]. InAs/GaSb nanowires with ultra-small lattice mismatch enables dislocation-free interfaces (small D_{it}) that critical for high tunneling probability. Notably, misfit dislocations still form in InAs on GaSb due to relaxation as a result of large strain from intermixed compositions (Figure 3B) [47]. On the other hand, these nanowire structures can be engaged with further structural and band engineering, such as strain modulation. Figure 3C,D show an example: biaxial stress perpendicular to the transport direction can remarkably improve the I_{OFF} versus I_{ON} tradeoff in InAs tunnel FETs and help open an I_{OFF} and V_{DD} window where tunnel FETs may outperform Si MOSFETs [48]. This model identifies stress configuration with great potential for high-performance InAs TFETs. A multi-layer structure with precisely controlled growth based on molecular beam epitaxy (MBE) technology is an experimental example: the output current is increased by orders of magnitude (Figure 3E–G) [49]. In addition to the lattice design of heterostructures, energy band engineering is also an important research topic. Currently, InAs-based heterostructures is the most stable and attractive system to achieve high performance TFET. InAs/GaSb axial superlattices exhibit type-III (broken-gap) alignment that creates a staggered overlap between the source valence band and channel conduction band, eliminating the need for carriers to tunnel through the entire bandgap. Further, multiple heterogeneous layers were designed to pursue more optimized structures with near-zero effective E_g as well as abrupt junction [46, 50]. In addition, the construction of nanowires is a key step in this system, because the quantum confinement effect shows a significant influence on the energy band regulation of group III–V semiconductors.

Although the InAs-related heterostructures are currently the most promising system for TFETs, it still faces insurmountable obstacles, especially on experiments. First, as with all 3D heterojunctions, the problem of interfacial defects prevents further performance improvements in InAs-related TFETs [50–52]. In addition, junction gradients at junction interface also degrade I_{ON} and SS [32, 53, 54]. Although this problem has been blamed more in earlier Si- or Ge-based tunnel junctions, it also needs further optimization in InAs-based TFETs. In this regard, the main means of optimization is to effectively control the nanowire growth stage. Technologies such as MBE and selected area epitaxy (SAE) are effective solutions (Figure 4) [55–57]. This technique leverages precursor flux modulation to suppress defect formation. The result shows that optimization on the tunnel-junction abruptness and pursue of defect-less interface is meaningful. Secondly, group III–V semiconductors generally show narrow bandgaps, which makes the designed TFET unable to effectively suppress I_{OFF}, and the application prospect of related devices is compressed from the side. In addition, the research progress of large-scale preparation strategy is also very important. Breakthrough has been made in the wafer-scale growth of III–V nanowire arrays through SAE with <5% diameter variation, but further application in the preparation and development of large-scale tunnel-junction arrays remains to be studied.

3.2 | Electrostatic Gate-Control Performance: A Bottleneck

The electrostatic control of tunneling junctions in nanowire-based TFETs remains a critical challenge, despite advancements in material properties and device architectures. Below, we expand on the key bottlenecks and emerging solutions, supported by experimental and computational insights. First of all, one major problem faced by nanowire transistors is the diameter-dependent screening effect, because the reduced surface-to-volume ratio in ultra-scaled nanowires degrades gate coupling efficiency. For sub-20-nm-diameter nanowires, the gate coupling efficiency significantly drops due to weakened electrostatic field penetration. To address this, researchers developed GAA architecture that enhanced field penetration by surrounding the nanowire with dielectric and gate metals, greatly improving the output

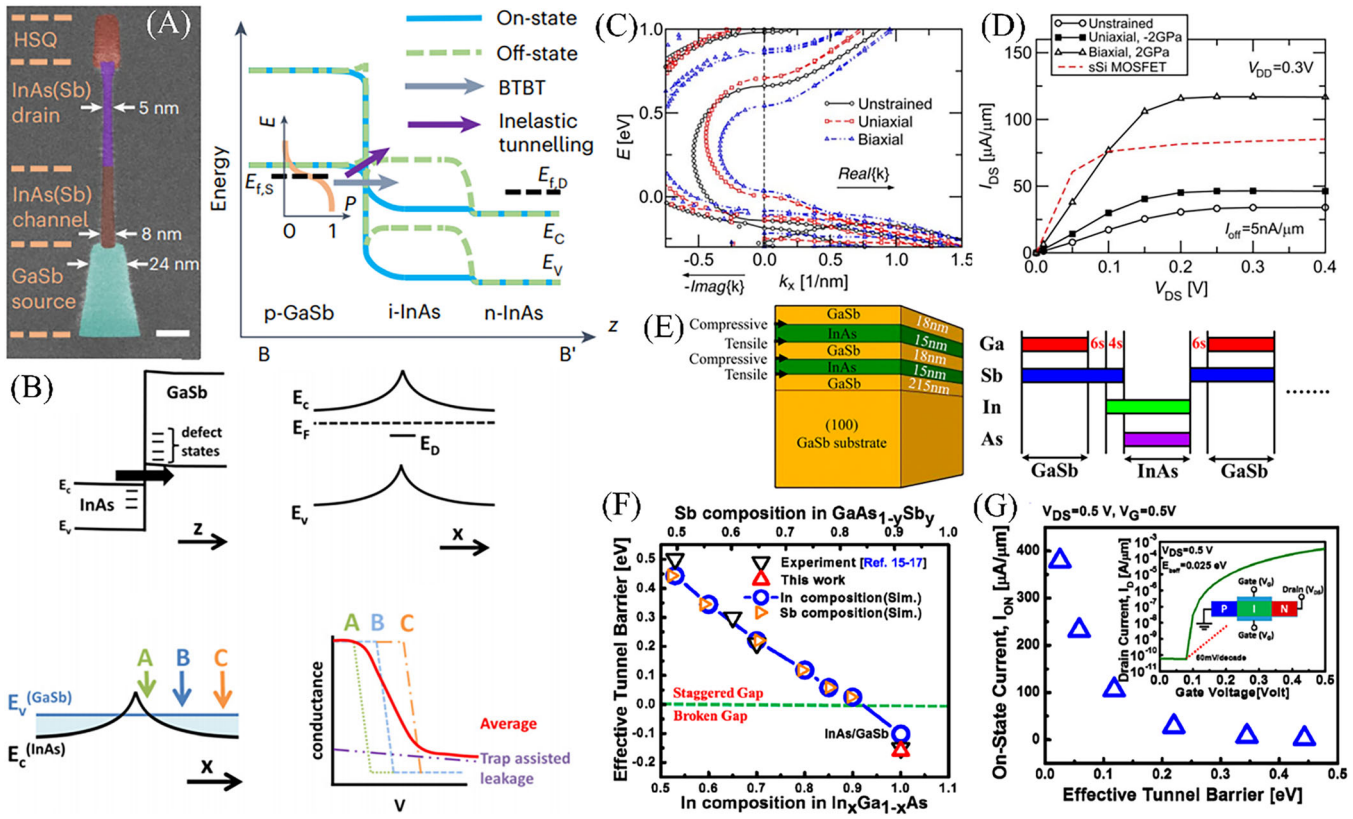

FIGURE 3 | Lattice engineering in nanowire TFETs. (A) Architecture of an Esaki diode based on a nanowire heterojunction, accompanied by illustrated energy band profiles for a vertical nanowire transistor. Critical parameters include the lowest conduction subband (E_c), highest valence subband (E_v), and Fermi level of source ($E_{f,S}$) and drain ($E_{f,D}$). Inset: temperature-dependent Fermi–Dirac distribution within the source, with energy (E) and occupation probability (P) axes labeled. Scale bars: 20 nm. Reproduced with permission [31]. Copyright 2012, Springer Nature. (B) InAs/GaSb heterojunction band alignment, indicating electron tunneling direction (arrow) and interface defect states (E_D) contributing to trap-assisted conduction. Three interfacial valence band configurations (A, B, C) correlate with distinct conductance–voltage characteristics. Experimental conductance (in red) demonstrates reduced slope from combined tunneling mechanisms and leakage pathways. Reproduced with permission [47]. Copyright 2014, AIP Publishing LLC. (C) Comparative energy dispersion analysis for InAs nanowires (5×5 nm cross-section) under three mechanical states: unstrained, uniaxial compression (applying T_{xx}), and biaxial tension (applying $T_{yy} = T_{zz}$). Potential energy reference set at wire interior. (D) Comparative current–voltage characteristics between InAs tunnel FET and Si MOSFET at equivalent gate overdrive ($V_{GS} = V_{GS,\ off} + V_{DD}$ $V_{DD} = 0.3$ V, $I_{OFF} = 5$ nA μm^{-1}). (C, D) Reproduced with permission [48]. Copyright 2012, IEEE. (E) Multilayer InAs/GaSb heterostructure schematic with MBE growth sequence detailing InSb interfacial layers and Sb surface treatments. Stress states at substrate interfaces: tensile at InAs/GaSb, compressive at GaSb/InAs. (F) Experimental versus simulated effective barrier heights (E_{eff}) across $GaAs_{1-y}Sb_y/In_xGa_{1-x}As$ compositional variations, demonstrating theoretical consistency. (G) Simulation results showing I_{ON} dependence on effective tunneling barrier height. (E–G) Reproduced with permission [49]. Copyright 2015, American Chemical Society.

performance of TFETs [58–62]. On the other hand, the parasitic capacitance (C_{gd}) trade-off is also a critical problem because C_{gd} between gate and drain limits switching speed and energy efficiency [63]. On this regard, high-κ (or low-κ) spacers (or dielectric pockets) may provide a good help [64–67]. Moreover, engaging ferroelectrics seems to be another useful option. Pb(Zr, Ti)O_3 or Si-doped HfO_2 dielectric integrated into nanowires induces NC effects, offering dual advantages for TFETs: (i) substantial improvements in device performance, such as ultra-steep switching and expanded steep-slope region attributed to the voltage-amplification effect of NC, and (ii) reduction on I_{OFF} and effective suppression on ambipolar behavior facilitated by voltage-pinning effect from ferroelectrics [68, 69]. In summary, electrostatic control remains a pivotal challenge for TFET scalability. Innovations in GAA architectures, SAE growth, and high-κ/ferroelectric integration offer promising pathways to overcome these limitations [70]. Future breakthroughs in strain engineering and hybrid material systems could further push the boundaries of sub-60 mV dec^{-1} operation, positioning TFETs as a cornerstone of post-Moore electronics.

3.3 | Innovations and Prospects

Heteroepitaxial nanowire TFETs represent a frontier in post-Moore electronics, with lattice engineering and band structure tailoring enabling sub-60 mV dec^{-1} operation. In recent years, the research enthusiasm about InAs-related TFET has begun to decline, which may be due to the fact that it has been difficult to obtain substantial breakthroughs in device performance under the existing structure. Therefore, in this review, we look forward to several innovative directions of device structure development, hoping to further promote the continued evolution of related TFET. Firstly, it might be a promising direction to develop hybrid

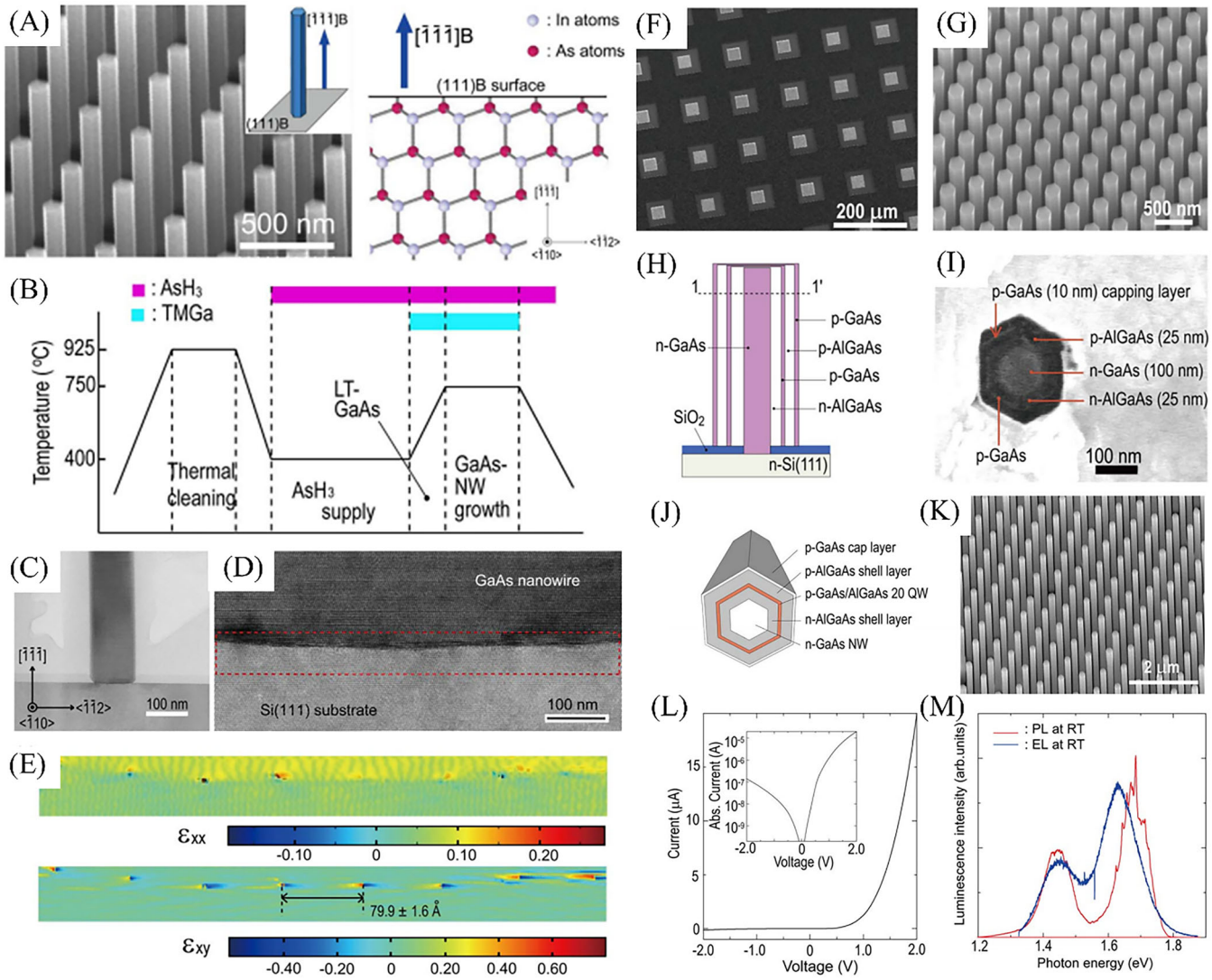

FIGURE 4 | SAE-processed nanowire for advanced TFET applications. Reproduced with permission [55]. Copyright 2011, IEEE. (A) Scanning electron microscope (SEM) micrograph illustrating InAs nanowire arrays grown epitaxially on InAs(111)B substrates, with structural schematic of the substrate. Cyan arrow indicates nanowire synthesis orientation. (B) Epitaxial growth protocol for GaAs nanowires on Si(111), highlighting low-temperature nucleation phase. (C) Low-resolution transmission electron microscope micrograph depicting GaAs/Si(111) interfacial region with electron beam aligned along <−110> zone axis. (D) High-magnification transmission electron microscopy (TEM) view corresponding to panel C. (E) Strain field analysis (ε_{xx} and ε_{xy} components) derived from geometric phase analysis of red-dashed region in D. (F) Topographic overview of patterned substrate supporting core-multi-shell (CMS) nanowire arrays. (G) Oblique-view (30° tilt) SEM characterization of CMS nanowire morphology. (H) 3D schematic representation of CMS architecture. (I) Cross-sectional SEM image obtained along H′s dashed profile (1–1′). (J) Structural schematic detailing AlGaAs/20-quantum-well/AlGaAs confinement layers in CMS cross-section. (K) Crystallographic analysis of CMS nanowire growth outcomes. (L) Current–voltage characteristics of CMS devices, with inset displaying semi-logarithmic transport behavior. (M) Comparative optoelectronic spectra demonstrating electroluminescence (EL, azure) and photoluminescence (PL, crimson) emission from CMS nanostructures. Compared with those based on novel 2D materials, TFETs based on nanowire heterostructure possess a relatively mature and stable technology for material preparation and device fabrication.

dimensional designs, that is, to further develop functional layers at the contact periphery of the nanowires, providing functional modulations with specific benefits. For example, combining DS materials with nanowires may leverage both steep switching and high mobility [71, 72]. Secondly, strain-programmable TFETs, realizing through piezoelectric actuators integrated with nanowires, can be employed for real-time E_g and *SS* tuning, which may be a potential scheme for harmonizing multiple conflicting parameters in TFET device physics [73–75]. In summary, these prospects highlight the potential of heteroepitaxial nanowire TFETs to transcend Boltzmann limits and promote its further compatibility and even replacement of current CMOS transistors while addressing scalability and energy efficiency demands for post-Moore electronics.

4 | Novel Tunnel Junctions Based on 2D Materials

The exceptional electronic characteristics of low-dimensional semiconductors have positioned them as pivotal components in advancing transistor technologies, particularly TFETs, over the

past decade. 2D materials offer distinct advantages over conventional 3D semiconductors, including atomic-scale thickness, tunable layer-dependent band structures, and superior charge carrier transport properties [76]. These attributes directly address fundamental limitations inherent to bulk semiconductor devices. The crystalline lattice of layered materials features robust in-plane covalent bonding contrasted by weak interlayer vdW interactions, enabling mechanical exfoliation of atomically thin sheets while preserving intrinsic electronic qualities. Crucially, the energy–momentum dispersion relations exhibit significant variation across monolayer, few-layer, and bulk configurations, permitting precise modulation of electronic behavior through external stimuli such as electric fields, strain, or magnetic fields.

The atomic confinement of charge carriers within 2D channels enhances electrostatic gate control by minimizing body thickness (t_{body}), thereby suppressing SCEs through geometric screening length (λ) reduction. This scaling parameter λ, inversely proportional to both equivalent oxide thickness (EOT) and t_{body}, governs critical performance metrics: it dictates the minimum viable gate length (L_g) for maintaining electrostatic integrity, influences Schottky barrier formation at metal–semiconductor interfaces, and modulates BTBT probabilities. The vdW heterostructure architecture eliminates interfacial defects common in conventional semiconductors, circumventing mobility degradation from dangling bonds while ensuring atomic-level thickness uniformity for abrupt band edge transitions essential for efficient tunneling.

These intrinsic properties collectively address two persistent challenges in 3D TFET implementations: achieving atomically sharp tunneling junctions and maintaining gate dominance in aggressively scaled devices [77, 78]. Material diversity within the 2D family enables tailored device engineering through heterojunction design—including homojunctions, mixed-dimensional hybrids, and all-2D vertical stacks—with performance metrics dictated by specific material parameters such as bandgap magnitude, carrier effective mass, and dielectric screening. Strategic band structure engineering combined with advanced fabrication techniques facilitates optimized tunneling efficiency, potentially realizing steep *SS* below the Boltzmann limit alongside high drive currents [79]. Current research focuses on exploiting these material-specific properties through innovative device architectures and contact engineering to overcome remaining challenges in contact resistance and tunneling probability optimization [80].

4.1 | 2D-Material Homojunctions: Obstacles and Opportunities

At the very beginning, thanks to the outstanding electrostatic performance of 2D materials, homojunctions based on single 2D materials like graphene and MoS_2 were designed and constructed through a segmented gate-voltage modulation strategy. Unfortunately, homogeneous tunneling junctions based on single 2D material cannot meet the requirements on all key parameters for constructing a high-performance TFET. For example, 2D semiconductors with flexible band-controllability such as TMDs do not have competitive ultra-low m^*, and graphene that can meet the m^* requirement is difficult to achieve uniform and efficient bandgap regulation. As a result, the experimental performance of TFETs in this category generally needs more significant improvement. Therefore, in this section, we will focus on the innovative structure research of relevant tunneling junctions: they are either based on device model simulation, or they are slightly deformed structures, which are not strictly homogeneous junctions. We still believe that this kind of TFET has great development potential, because the homojunction can naturally show a defect-free tunnel junction, which is one of the necessary factors for high-performance TFETs.

Initial explorations of 2D material-based TFETs leveraged the superior electrostatic integrity of homojunction architectures employing materials like graphene and TMDs. These mono-material-based tunneling configurations, however, face intrinsic material limitations in simultaneously achieving critical performance metrics. Graphene's exceptional carrier mobility stems from its remarkably low effective mass ($m^* \approx 0.033m_0$), a critical parameter for high-performance tunnel junctions [81, 82]. While graphene benefits from its massless Dirac fermion behavior near the *K*-point offers exceptional transport characteristics, its inherent zero bandgap fundamentally restricts tunneling efficiency. Conversely, TMDs demonstrate gate-tunable bandgaps but suffer from comparatively higher m^* values that limit tunneling probability [83, 84]. This material-level tradeoff has driven innovations in structural engineering to circumvent inherent limitations. For example, symmetry-breaking mechanisms under vertical bias have emerged as critical enablers for graphene-based TFETs. Bilayer graphene exhibits electrically tunable bandgap opening through controlled interlayer potential asymmetry, achieved via dual-gate architectures with spatially separated gate electrodes (Figure 5A) [85]. Computational studies demonstrate that differential biasing of partially overlapping top and bottom gates induces both channel bandgap modulation and doping gradient formation across source–channel–drain regions (Figure 5B–D). This configuration enables simultaneous optimization of tunneling window and carrier injection efficiency [87]. Experimental implementations further enhance this asymmetry through surface charge transfer doping, where physisorbed F_4TCNQ molecules create interlayer charge imbalance, amplifying the vertical electric field's bandgap-opening effect (Figure 5D) [85]. Contact engineering through work-function-tailored electrodes complements this approach by enabling Fermi level alignment without conventional impurity doping [88]. The design of effective contact structures in 2D materials often involves both the edge and top surface due to the significant surface-to-edge area ratio of the contact [89]. In addition to enhancing edge contacts, overall contact performance can be improved by reducing the tunnel barriers specifically at the top surface. This can be effectively realized through the hybridization of interfacial metal atoms (e.g., Ti) [90] or emerging 2D semimetals (e.g., graphene) [91] with the surface atoms of 2D semiconductors. Prior research provides a well-established framework for achieving low-resistance Ohmic contacts on 2D semiconducting surfaces using this surface hybridization approach.

Beyond graphene, materials with balanced m^* and bandgap characteristics show promise. TFETs based on $MoTe_2$ demonstrates enhanced performance in hetero-stack configurations combining few-layer channels with graphene gate electrodes and hexagonal

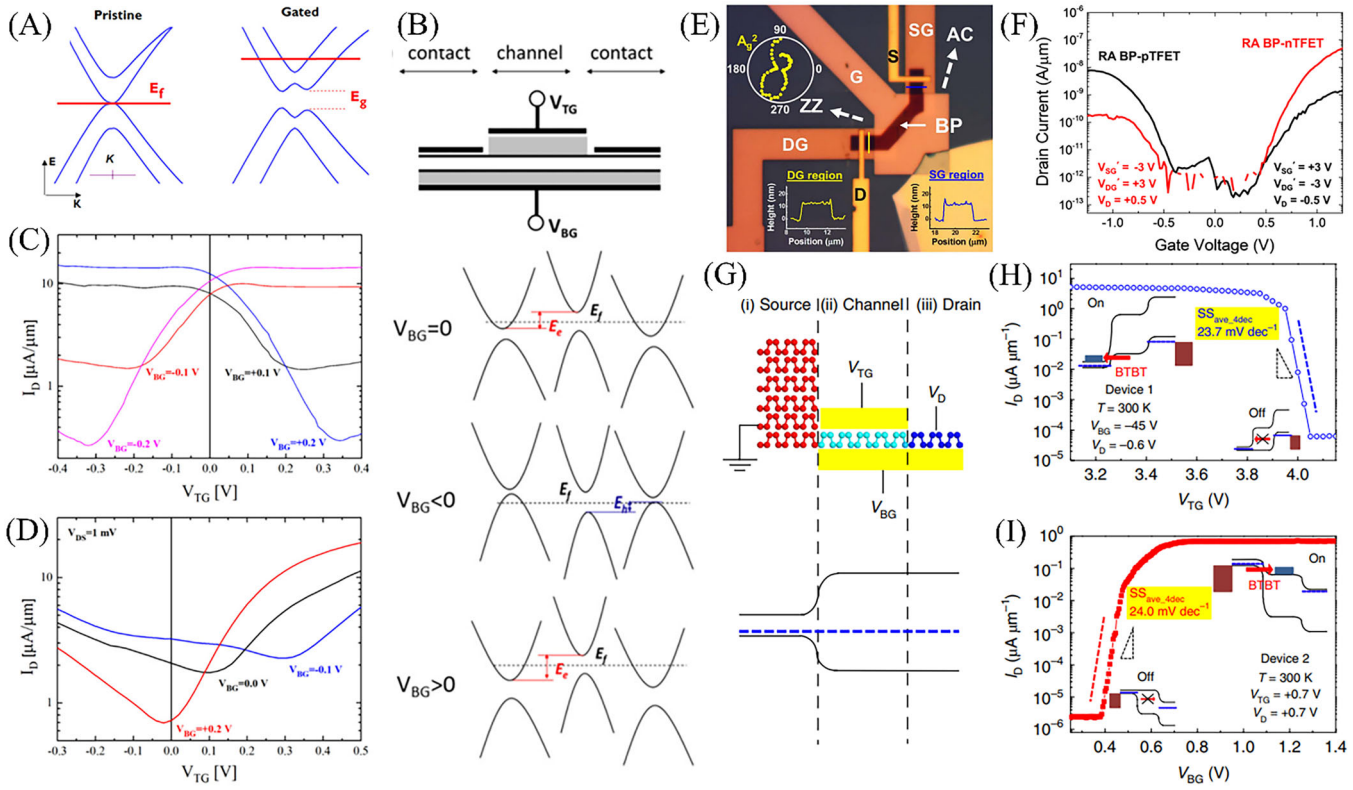

FIGURE 5 | Transport engineering in homo-junctional 2D TFETs. (A) Energy dispersion relations of intrinsic graphene under neutral conditions versus electrostatically gated configurations. (B) Architectural schematic and equilibrium/nonequilibrium band alignment for dual-gated graphene FET incorporating doped source/drain electrodes. (C) Modulated transfer characteristics for undoped devices with back-gate potential swept between −0.2 and +0.2 V. (D) Modulated transfer characteristics under surface charge transfer doping via F_4TCNQ molecular layers, demonstrating gate-tunable behavior at back-gate voltage (V_{BG}) = +0.2, 0, and −0.1 V, respectively. (A–D) Reproduced with permission [85]. Copyright 2014, IOP Publishing. (E) Planar microscopy visualization of right-angle BP tunneling FET architecture, accompanied by topographic atomic force microscopy line profiles at charge injection interfaces and polarization-dependent Raman spectroscopy signatures. (F) Ambipolar transport characteristics for p-type (black) and n-type (red) BP-TFET operation under symmetric source-drain bias configurations ($V_{DD} = \pm 5$ V). (E, F) Reproduced with permission [86]. Copyright 2019, IEEE. (G) Hetero-structured BP tunnel junction illustrating layer-dependent band alignment across three functional zones: (i) heavily doped source, (ii) electrostatically modulated channel, and (iii) drain with field-induced band-shift. Color gradients represent doping concentration variations. (H) p-channel switching characteristics at $V_{DD} = -0.6$ V exhibiting 0.15 V threshold gate swing for current modulation. (I) n-channel operation at $V_{DD} = +0.7$ V requiring 0.2 V back-gate actuation for ON/OFF transition. Inset: band engineering through coordinated V_{BG}, V_{TG} (top-gate voltage), and V_{DD} manipulation enables precise control over inter-band tunneling conditions ($\Delta\varphi > 0$ for BTBT activation vs. blockade in off-state). (G–I) Reproduced with permission [36]. Copyright 2020, Springer Nature.

boron nitride (*h*-BN) dielectrics [35]. These devices achieve sub-60 mV dec^{-1} switching characteristics through optimized band alignment and reduced D_{it}. In addition to $MoTe_2$, BP emerges as a particularly versatile candidate due to its thickness-dependent direct bandgap (0.3–2 eV) and anisotropic effective mass ($m^*_{T\_armchair} \approx 0.1m_0$ vs. $m^*_{T\_zigzag} \approx 0.15m_0$) [92–94]. According to this characteristic, researchers designed in-plane biaxial TFET, which shows good application potential (Figure 5E,F) [86]. Such advance also positions anisotropic 2D materials as viable platforms for post-CMOS steep-slope devices. On the other hand, a monolayer-to-bulk BP TFET architecture exemplifies another flexibility: bulk BP in the source region enhances band-to-band tunneling efficiency, while monolayer BP in the channel/drain regions suppresses ambipolar conduction through widened bandgaps (Figure 5G) [36]. As a result, vertical BP TFETs achieve sub-thermal switching (26 mV dec^{-1} over 5 current decades) by decoupling source doping control from channel electrostatics via independent dual-gate addressing (Figure 5H,I). These architectural innovations highlight two key design principles: (1) Spatial separation of bandgap engineering and carrier transport pathways enables independent optimization of tunneling probability and electrostatic control. (2) Anisotropy engineering through crystallographic alignment and thickness grading allows access to favorable transport directions and effective mass minimization [95–97]. While current experimental implementations still face challenges in achieving simultaneously high I_{60} (as least 1 μA μm^{-1} is required) and sub-60 mV dec^{-1} operation across wide current ranges of more than 4 orders of magnitudes, the fundamental compatibility of these designs with scalable vdW integration suggests substantial potential for performance scaling through multilayer stacking and contact resistance reduction strategies.

4.2 | Vertical vdW Heterojunctions: Great Potential

Vertical vdW heterostructures present transformative opportunities for tunneling device engineering through atomic-scale

interfacial sharpness and programmable band structure manipulation [98]. The weak interlayer bonding inherent to vdW systems permits heterogeneous integration of disparate dimensional materials—combining another 3D, 2D, or even 1D materials—while maintaining pristine interfaces free from dangling bonds. Such architecture enables precise control over band alignment geometries critical for TFETs, particularly type-II or type-III heterojunctions where conduction and valence band extrema reside in separate material layers (Figure 6) [13, 99–104]. In addition to the band structure of the reference material, the subthreshold swing device physics also emphasizes the importance of the m^* in investigated materials (as summarized in Table 4) [16, 105]. Optimal vdW-TFET design requires strategic material pairing to simultaneously achieve narrow tunneling barriers and suppressed off-state leakage. This necessitates source regions with wider bandgaps to limit thermionic emission while implementing staggered band offsets at the heterointerface to reduce effective barrier heights. The atomic thickness of constituent layers creates sub-nm tunneling paths orthogonal to gate fields, eliminating parasitic lateral tunneling pathways. This vertical transport mechanism enables strong gate modulation of interlayer band overlaps, crucial for achieving steep subthreshold characteristics. A prototypical implementation employs MoS_2/WTe_2 heterostructures, where lattice mismatch-induced biaxial strain engineering modifies both bandgap and carrier effective masses (Figure 7A–C) [78]. The 4.2% compressive strain in WTe_2 and corresponding tensile strain in MoS_2 synergistically reduce the heterojunction's effective bandgap to 135 meV while maintaining moderate hole (WTe_2 VBM) and electron (MoS_2 CBM) effective masses of $0.36m_0$ and $0.45m_0$ respectively. This engineered pseudo-direct gap configuration enhances tunneling probability without excessive carrier mass penalties, enabling sub-thermal switching behavior. On the other hand, BP also exhibits great potential in constructing high-performance tunnel junctions based on vdW heterostructures. Here, two notable advantages worthy of affirmation are: (1) Characteristic of small m^* and promising tunneling performance had been demonstrated in bare-BP tunnel junctions, and (2) large-scale growth methods and transfer techniques of BP had been developed for flexible design and fabrication of a series of vdW heterostructures and further the transistor arrays [106, 107], which have laid a solid foundation for the design and development of TFET based on BP heterojunction.

The inherent limitations of wide-bandgap 2D semiconductors in achieving sufficient BTBT probability have driven innovative heterostructure engineering strategies. Computational studies reveal that hybrid architecture combining narrow-gap 3D materials with atomically thin channels can circumvent this challenge while preserving electrostatic control. A seminal

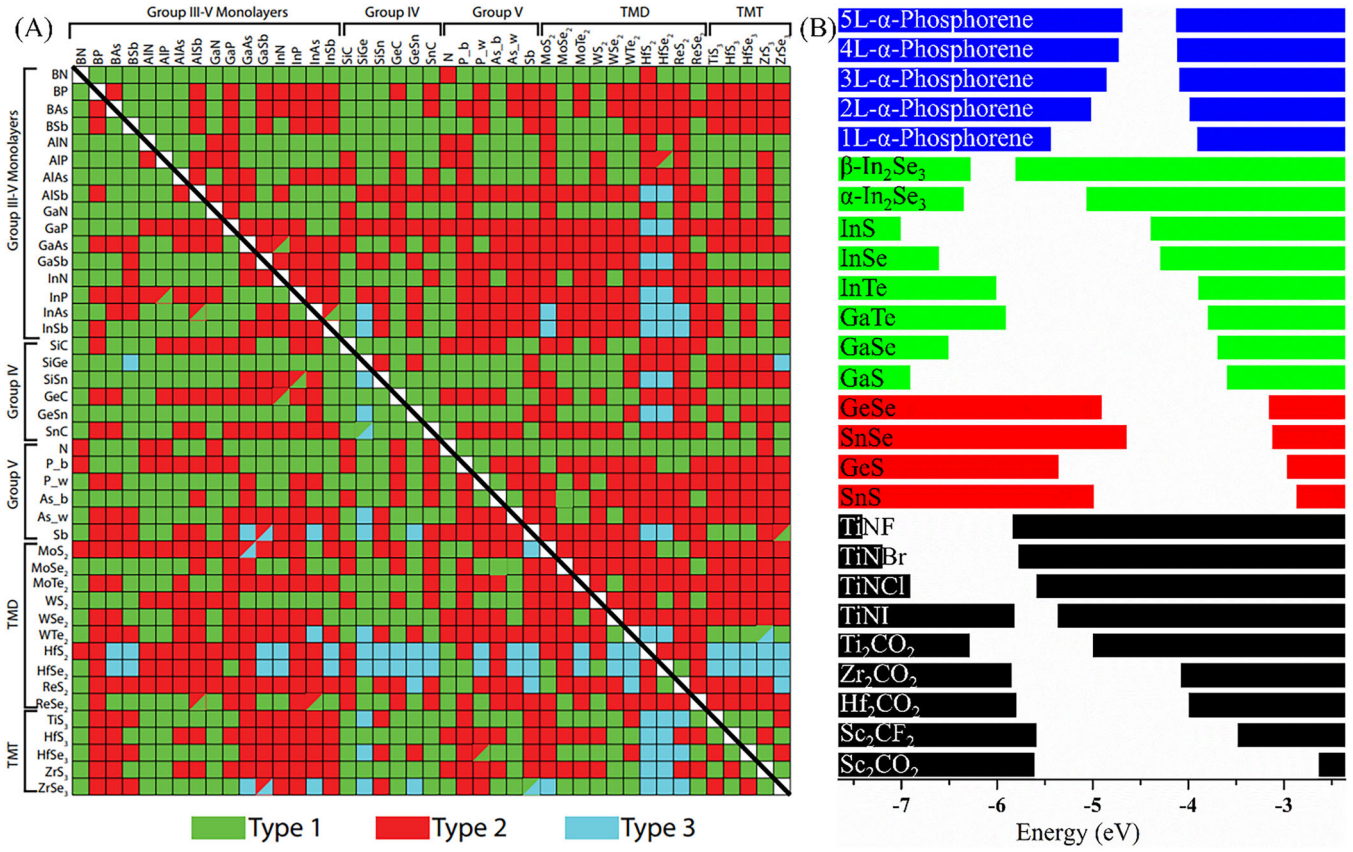

FIGURE 6 | A library of comparative band alignments of potential semiconductors for TFET design. (A) Periodic table of potential heterojunctions for TFET design. Green, red, and blue means the band alignments in Type I, II, and III, respectively. With the black diagonal line as the boundary, the results below and above represent calculations from Perdew–Burke–Ernzerhof functional and Heyd–Scuseria–Ernzerhof-06 (HSE-06) hybrid functional, respectively. Reproduced with permission [99]. Copyright 2016, American Physical Society. (B) As a supplement to A, we list some emerging 2D materials, including few-layer BP (blue), group III–VI (green), group IV–VI (red), and transition metal carbides or nitrides (MXenes, black) as potential candidates for tunneling junction design and presenting their band alignments calculated from HSE06.

TABLE 4 | A library of calculated values of E_g and m^* in potential source-end materials for heterojunction-based TFET design.

Material	E_g (eV)	m^*_e (m_0)	m^*_h (m_0)
InP	1.42	0.08	0.121
InAs	0.42	0.026	0.027
InSb	0.24	0.014	0.015
GaAs	1.52	0.067	0.09
GaSb	0.81	0.039	0.044
WTe_2	0.92	0.28	0.39
$HfSe_2$	0.76	0.19	0.14
$AlLiTe_2$	0.91	0.15	0.36
As	0.81	0.08	0.08
Bi	0.55	0.04	0.03
SnTe	0.73	0.09	0.10
TiNBr	0.63	0.18	0.17
TiNCl	0.58	0.18	0.17
1L-BP	1.61	0.17	0.16
2L-BP	1.09	0.18	0.16
3L-BP	0.79	0.16	0.14
$MoTe_2$-SnS_2	0.19	0.25	0.6

demonstration employed p-doped germanium as a high-carrier-density source interfaced with CVD-grown bilayer MoS_2 transferred via polymer-mediated techniques onto the substrate (Figure 7D–F) [33]. This mixed-dimensional vdW junction spatially confines tunneling events to the vertically aligned Ge/MoS_2 overlap region, suppressing parasitic lateral transport through geometric isolation. Critical design parameters include the staggered type-III band alignment at the interface, which creates a pseudo-direct tunneling path with reduced effective barrier height (~0.5 eV) compared to homogeneous 2D systems. The atomic-scale separation between Ge and MoS_2 (0.3–0.4 nm) establishes an ultrathin tunneling barrier, while gate-field parallelism to the vertical transport direction enhances gate modulation efficiency. Under bias, the gate-tunable band overlap between Ge's valence states and MoS_2's conduction states generates a sharply defined tunneling window, producing record-low *SS* values of 3.9 mV dec^{-1} (minimum) and 31.1 mV dec^{-1} (average) across four current decades, coupled with 10 μA μm^{-1} on-state currents at room temperature. Similar studies on mixed-dimensional heterojunction TFET have also been carried out on various structures. One result with promising performance is the Si/InSe tunnel junction (Figure 7G–K) [34]. While such 3D/2D hybrids demonstrate performance metrics surpassing all-2D counterparts, interfacial oxidation from 3D materials during fabrication introduces unintended tunneling barriers. Native oxide formation at Ge or Si surfaces disrupts designed band alignments, necessitating advanced encapsulation techniques or in situ heteroepitaxial growth methods to preserve interface quality. Ongoing research focuses on developing oxidation-resistant contact metallurgies and alternative narrow-gap 3D materials to maintain the tunneling probability enhancements demonstrated in mix-dimensional tunnel-junction systems.

The advancement of TFETs based on 2D materials hinges critically on the strategic integration of vdW heterostructures with optimized band alignment and vertical transport mechanisms. Recent theoretical and experimental investigations emphasize that vertically stacked all-2D heterojunctions leveraging BTBT as the dominant conduction mechanism offer a viable pathway to overcome the performance limitations of conventional 2D-TFET designs. This approach combines the inherent benefits of mixed-dimensional heterojunctions—such as atomically sharp interfaces and minimized defect-mediated recombination—with enhanced electrostatic control through optimized layer doping and band engineering.

Among various material combinations, the WSe_2/$SnSe_2$ heterostructure has emerged as particularly promising due to its favorable electronic properties (Figure 8A–C) [37, 110]. The as-synthesized $SnSe_2$ exhibits exceptionally high intrinsic electron concentration, surpassing other n-type 2D semiconductors like $PtSe_2$ [111], which directly translates to steeper *SS* characteristics in device operation. Complementary to this, WSe_2 demonstrates moderate p-type doping with lower carrier density, enabling efficient gate-field modulation of band bending at the tunnel junction [112]. Experimental implementations employing these materials on HfO_2 substrates have demonstrated broken-gap alignment configurations, achieving sub-60 mV dec^{-1} switching behavior with a minimum *SS* of 35 mV dec^{-1} at room temperature. Notably, such devices exhibit comparable drive currents (I_{ON}) to conventional WSe_2 MOSFETs while reducing I_{OFF} by three orders of magnitude, marking significant progress in balancing switching steepness with current drive capability.

Device architecture innovations further enhance performance metrics. The integration of ferroelectric Si-doped HfO_2 in gate dielectric stacks introduces NC effects, experimentally demonstrating sub-thermionic switching with minimum *SS* values below 15 mV dec^{-1} and average *SS* of 20 mV dec^{-1} across two current decades [108]. This improvement occurs alongside maintained I_{ON} levels of 0.1 μA μm^{-1}, validating the compatibility of vdW heterostructures with established CMOS optimization techniques (Figure 8D,E). Critical design parameters include precise alignment of gate electrodes relative to the tunnel junction and careful tuning of doping profiles through selection of intrinsically doped 2D materials. These developments collectively highlight the potential of engineered vdW interfaces combined with advanced electrostatic control strategies to overcome fundamental performance trade-offs in steep-slope transistor technologies.

4.3 | Challenges and Prospects

The vdW heterostructures exhibit unique advantages in tailoring heterointerfaces with engineered band alignment properties for TFETs. The strategic integration of 2D materials enables precise modulation of tunneling barriers through optimized band edge effective masses and reduced barrier heights. The interlayer vdW separation creates an atomically thin barrier dimension at the heterojunction, while the vertically aligned lattice structures enhance tunneling cross-sectional areas. This geometric configuration allows direct electrostatic control of carrier injection via gate fields aligned parallel to the tunneling direction, collectively enhancing quantum mechanical

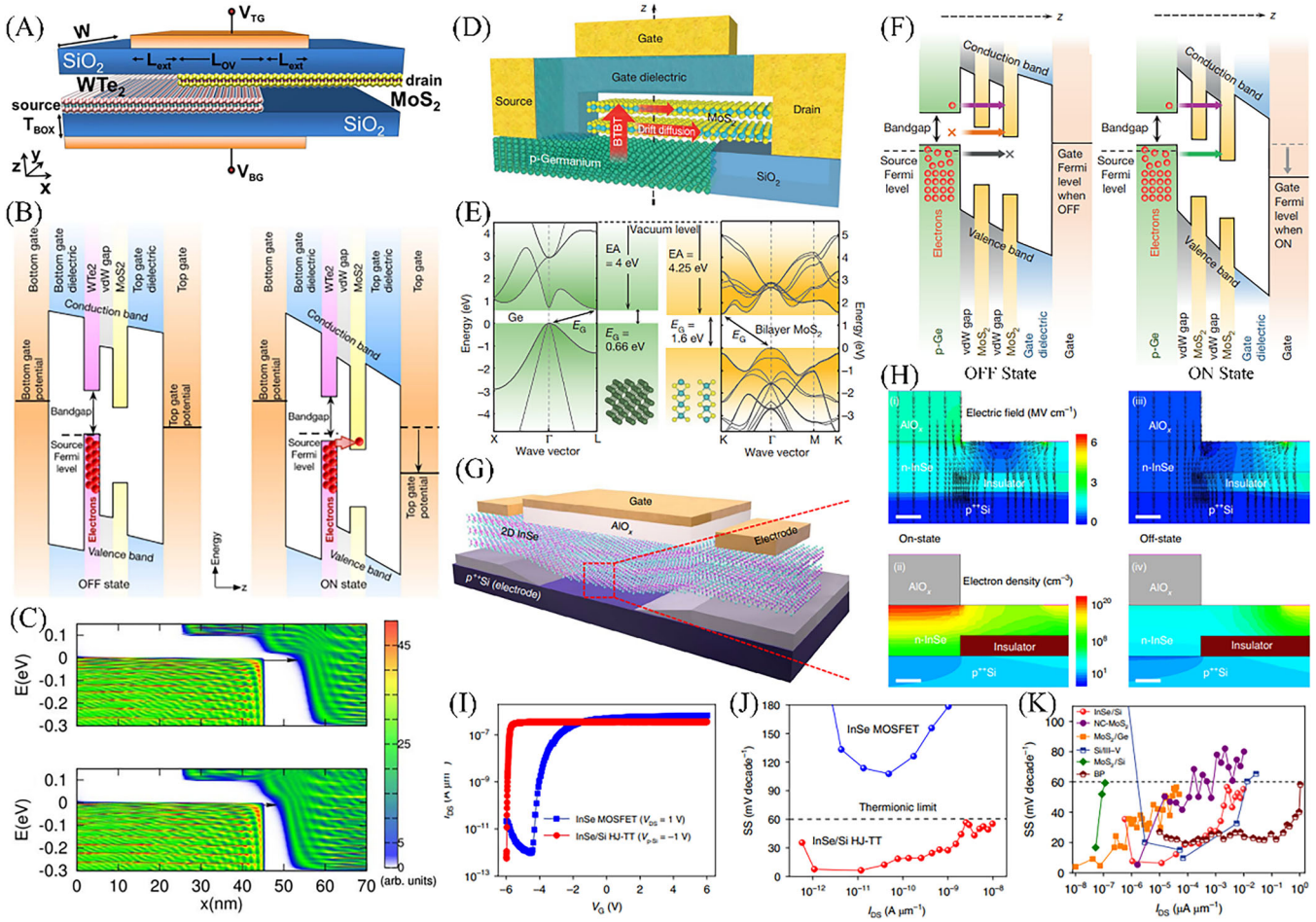

FIGURE 7 | Demonstrations of vdW-heterostructure TFETs. (A) Schematic of the MoS_2/WTe_2 vdW-TFET architecture, defining key geometric parameters: L_{ov} (heterojunction overlap length), L_{ext} (top-gate extension beyond L_{ov}), and L_{TG} (total gate length = L_{ov} + $2L_{ext}$). (B) Energy band alignment across the heterointerface (z-axis) under operational conditions. Top-gate biasing enables CBM and VBM overlap in the ON-state, facilitating vertical interlayer BTBT. (C) y-axis integrated local density of states (DOS) within the active region for L_{ext} = 10 nm (upper panel) and 5 nm (lower panel), with arrows indicating dominant tunneling pathways. Simulation parameters: $L_{ov} = W = 20$ nm, $T_{BOX} = 1$ nm; $V_{DD} = 0.3$ V, $V_{TG} = -0.2$ V. Energy levels referenced to source Fermi level ($E_{F,S} = 0$ eV) and drain Fermi level ($E_{F,D} = -0.3$ eV). (A–C) Reproduced with permission [78]. Copyright 2016, IEEE. (D) Cross-sectional view of Ge/MoS_2 heterojunction TFET illustrating hybrid transport mechanisms: vertical BTBT from the Ge source to MoS_2 followed by lateral drift-diffusion through the channel (red arrows). (E) Band offset diagram comparing electron affinities and E_g of Ge and bilayer MoS_2, demonstrating staggered alignment. Crystal structures and electronic band diagrams are inset. (F) Simulated energy band profiles along the vertical transport path in OFF (left) and ON (right) states, with white regions denoting bandgap-induced zero DOS. (D–F) Reproduced with permission [33]. Copyright 2015, Springer Nature. (G) Schematic of n-InSe/p^{++}-Si mix-dimensional heterojunction TFET. (H) TCAD simulations showing electric field distribution (i, ON; iii, OFF) and electron concentration profiles (ii, ON; iv, OFF) during switching. Scale bar: 2.5 nm. (I) Comparative transfer characteristics and (J) SS between InSe MOSFETs and InSe/Si TFETs, with dashed line indicating Boltzmann limit (60 mV dec^{-1}). (K) Benchmarking of SS performance across various sub-60 mV dec^{-1} devices. Red data points highlight InSe/Si TFET achieving $SS_{min} = 6.4$ mV dec^{-1} with sustained sub-thermal switching over five current decades. (G–K). Reproduced with permission [34]. Copyright 2022, Springer Nature.

transmission probabilities beyond conventional lateral junction devices. Notably, experimental demonstrations of 2D TFETs achieving sub-60 mV dec^{-1} SS at ambient conditions predominantly utilize vdW heterostructures, underscoring their superiority in electrostatic control. Nevertheless, performance scalability faces intrinsic challenges from fabrication-induced variability. Substrate imperfections, mechanical deformations in ultrathin layers, and angular misalignment during stacking introduce spatial fluctuations in interlayer separation. Such nonuniform vdW gaps critically degrade tunneling current densities and subthreshold linearity due to the exponential sensitivity of tunneling probability to barrier width (Figure 8F,G) [29]. Process refinement for atomic-level gap uniformity remains imperative for reliable device characteristics.

Material-specific limitations further constrain performance potential. Anisotropic carrier effective masses in layered crystals, particularly heavier out-of-plane mass components, inherently suppress vertical tunneling currents [113]. This imposes fundamental trade-offs between achieving high on-state currents and maintaining optimal I_{ON}/I_{OFF} ratios, necessitating band structure engineering through heterostructure design and strain modulation [114]. Additionally, stochastic domain orientations in CVD-grown TMDs and transfer-induced

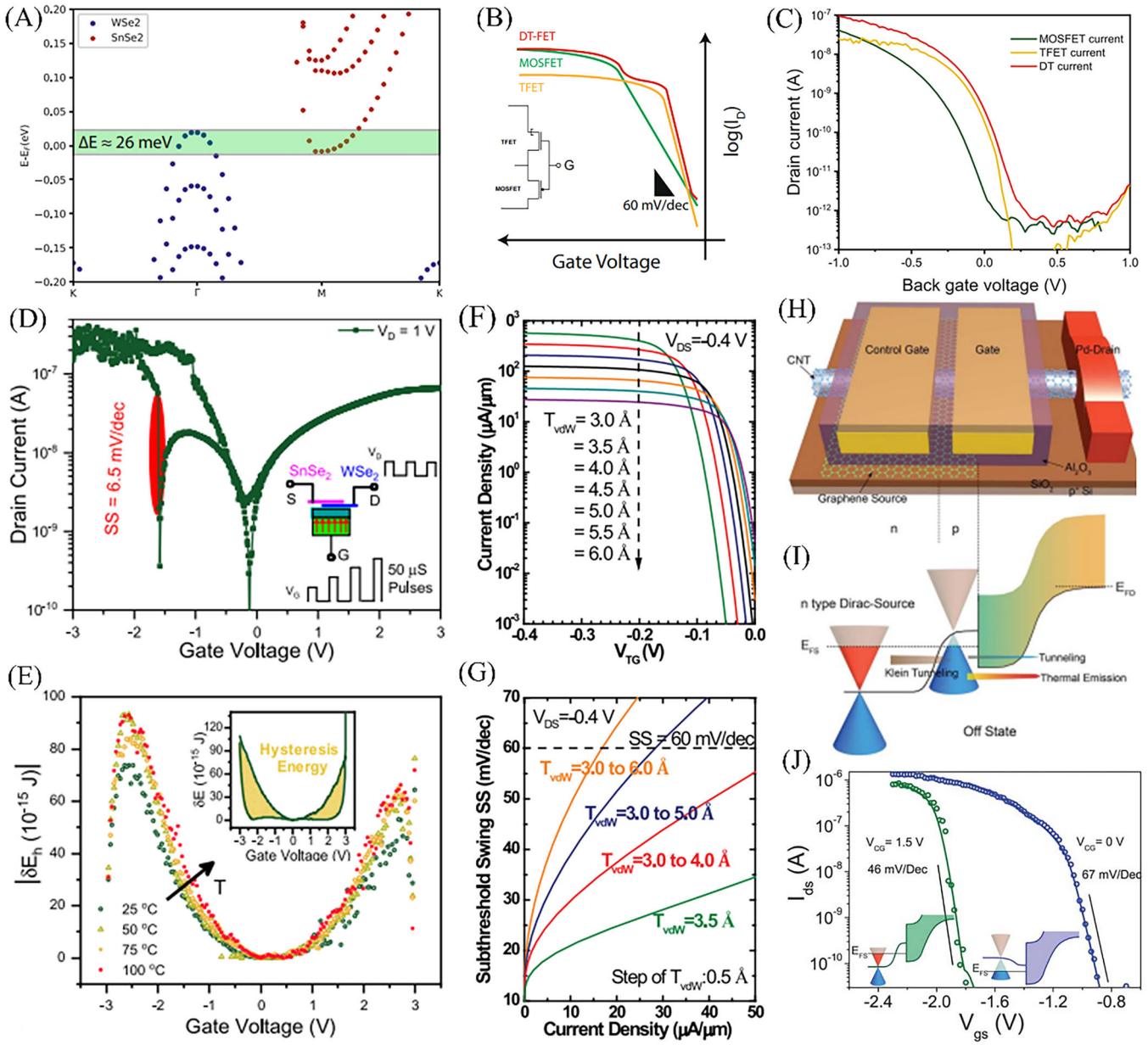

FIGURE 8 | Innovative research on TFET architecture. (A) Calculated band alignment at the $WSe_2/SnSe_2$ heterointerface: DFT reveals a 26 meV energy overlap between the valence band maxima of WSe_2 and the CBM of $SnSe_2$. (B) Conceptual transfer behavior of a dual-transport (DT) steep-slope FET, combining the abrupt switching of a TFET with high I_{ON} of a WSe_2 MOSFET. Ideal DT operation follows the TFET's steep subthreshold regime before transitioning to MOSFET-dominated thermionic transport at higher gate biases and output currents. (C) Experimentally optimized transfer characteristic curves for standalone WSe_2 FETs and $WSe_2/SnSe_2$ TFETs, engineered to satisfy $V_{Th,\ TFET} > V_{Th,\ MOSFET}$. The hybrid DT characteristic merges with the sub-60 mV dec^{-1} switching of TFETs with the MOSFET's current drive. Measurements performed at $V_{DD} = 0.5$ V. (A–C). Reproduced under terms of the CC-BY license [37]. Copyright 2020, Oliva et al., published by Springer Nature. (D) Subthreshold characteristics of a NC-TFET demonstrating record-low *SS* over two current decades. Inset: pulsed-measure methodology for suppressing self-heating artifacts. (E) Hysteretic energy dissipation in gate dielectric capacitors during bidirectional voltage sweeps. (D, E) Reproduced under terms of the CC-BY license [108]. Copyright 2021, Kamaei et al., published by Springer Nature. (F) Interlayer tunneling current density versus V_{TG} for varying vdW gap thicknesses (T_{vdW}). (G) Differential *SS* features versus current density, statistically modeled for T_{vdW} variations within specified bounds. (F, G) Reproduced under terms of the CC-BY license [29]. Copyright 2015, Li et al., published by IEEE. (H) Device schematic of a DS-TFET incorporating a secondary control gate (CG) for band profile modulation. (I) Energy band diagram of DS-FET in OFF-state, highlighting carrier-blocking mechanisms. (J) Transfer characteristics of DS-FET under CG biases ($V_{CG} = 0$, 1.5 V). Experimental data (circles) align with simulated curves (lines), with insets showing band diagrams for each operational mode. Green (blue) traces correspond to V_{CG} = 1.5 V (0 V) configurations. (H–J) Reproduced with permission [109]. Copyright 2018, American Association for the Advancement of Science.

interface contaminants hinder reproducible hetero-stack formation. While vdW integration circumvents lattice mismatch constraints of conventional epitaxy, the current absence of standardized fabrication protocols for multi-stack alignment and defect minimization delays technological maturation. Addressing these material synthesis and integration challenges remains crucial for transitioning vdW-TFET concepts into CMOS-compatible manufacturing frameworks.

In addition to the pursuit of optimization in material design, energy band engineering, material synthesis, device preparation technology, and other aspects, innovations on device structure design and device physical model research and development are also worthy of attention and expectations. Here, we hope to enumerate some interesting research to promote innovation in this field. For example, the innovations on the contact layers and the peripheral structures, such as NC-layer (Figure 8D,E) [108] or DS-layer integration (Figure 8H–J) [109], multiple-gate designs, and so on, are remarkable. Moreover, the development of high-throughput computational screening database based on machine learning will be conducive to further optimization of the system and structure by identifying direct momentum-matching configurations in vdW hetero-stacks, eliminating phonon-assisted tunneling and achieving near-ideal *SS* [115–117]. In summary, the future of 2D TFETs hinges on transcending material synthesis bottlenecks, advancing atomic-scale process control, and reimagining system architectures for quantum-era computing. The synthesis of vertical or lateral vdW heterojunctions is inherently facilitated in materials like graphene, *h*-BN, and TMDs due to their stable monolayer isolation capabilities, predictable polymorphism, and fixed stoichiometric compositions [118, 119]. These characteristics enable reliable fabrication through either mechanical stacking or bottom-up growth techniques [120]. In contrast, layered crystals exhibiting compositional versatility demonstrate significant synthesis variability through distinct polymorphic phases, particularly for group IV chalcogenides with tunable chalcogen content (*e.g.,* tin/germanium sulfides, SnS_2, Sn_2S_3, SnS, etc.) [121]. Such stoichiometric diversity creates opportunities for engineering unconventional heterostructures with tailored electronic and optical properties inaccessible in conventional systems. While challenges in uniformity, reliability, and cost persist, synergistic innovations in machine learning-guided growth, defect engineering, and 3D integration herald a new era of ultra-low-power electronics. Realizing this vision demands concerted collaboration across academia, industry, and government to accelerate the transition from lab-scale curiosities to foundational post-Moore technologies.

5 | Summary and Outlooks

The relentless pursuit of energy-efficient electronics in the post-Moore era has positioned TFETs as a transformative alternative to conventional CMOS technology. By exploiting BTBT rather than thermionic emission, TFETs circumvent the Boltzmann tyranny of *SS* and achieved outstanding values well below 60 mV dec^{-1}, enabling ultra-low-power operation with steep switching characteristics. This review systematically delineates the device physics, material innovations, and architectural advancements driving TFET development. Experimental demonstrations for *SS* features well below 60 mV dec^{-1} in vertical 2D heterojunctions (e.g., MoS_2/WTe_2) and heteroepitaxial nanowires (e.g., InAs/GaSb) underscore the potential for TFETs to achieve performance metrics unattainable by traditional MOSFETs [122]. Breakthroughs most worthy of further attention include the integration of 2D materials and vdW heterostructures, which offer atomic-scale thickness, pristine interfaces, and tunable band alignment to enhance tunneling efficiency. In the preparation process of 3D heterojunctions, pulsed laser deposition (PLD) has been proven to be an efficient solution for preparing large-scale samples. However, in the emerging 2D heterojunction preparation process, the current main reports still focus on mechanical exfoliation and CVD schemes, and the obtained sample sizes are relatively small. PLD has several advantages that make it suitable for growing complex material films. These include the precise transfer of material composition from the target to the substrate, the generation of high-energy species, strong interactions between ablated cations and the surrounding gas in the plasma, and adaptability to a wide range of background pressures ranging from ultrahigh vacuum to 1 Torr [14]. Notably, PLD also allows for the deposition of multicomponent films by using either single stoichiometric targets or multiple targets for individual elements. Recent advances have confirmed PLD's capability for wafer-scale 2D material synthesis and device array fabrication [123], positioning it as a promising methodology for scalable production of van der Waals heterojunctions essential for next-generation TFETs. In addition to the preparation process, computational frameworks, such as NEGF simulations, have further accelerated device optimization by resolving quantum transport phenomena and guiding material-structure codesign. However, critical challenges persist. Material synthesis limitations, such as defect control in 2D hetero-stacks and doping abruptness in III–V nanowires, hinder reproducible device performance. Contact resistance, ambipolar conduction, and scalability issues remain unresolved bottlenecks. Moreover, the trade-off between I_{ON} and *SS* necessitates balanced engineering of bandgap, effective mass, and electrostatic control. While NC integration and strain engineering have shown promise in mitigating these trade-offs, their practical implementation requires further refinement.

The future of TFET technology hinges on interdisciplinary innovations spanning materials science, device physics, and fabrication engineering. Strategic directions to focus on include: (1) material research and heterostructure design, such as investigating novel 2D materials with tailored bandgaps and anisotropic effective masses, exploring mixed-dimensional heterojunctions to combine the high carrier density of bulk materials with the electrostatic control of atomically thin channels, and developing machine learning-guided screening of vdW heterostructures for direct bandgap alignment and momentum-matched tunneling pathways [99, 124, 125]; (2) advance in device architectures, such as designing novel contact-layers integration like DS or phase-change materials configurations to introduce valuable regulatory mechanisms, and developing hybrid systems engaged with novel device mechanisms like NC or spintronics [68, 71, 108, 126]; (3) manufacturing and scalability developments, such as advances in wafer-scale synthesis of 2D materials to ensure uniformity and defect control, atomic-level doping techniques for abrupt junction profiles in nanowires or 2D channels, and 3D integration strategies for TFETs with CMOS-compatible processes to enable monolithic circuits for IoT and edge-computing applications [59, 106, 127, 128]; (4) fundamental physics and modeling, such as first-principles quantum transport simulations to resolve interfacial defect states and phonon-assisted tunneling mechanisms, and exploration of correlated electron effects (e.g., Mott transitions) in strongly interacting 2D systems for voltage-gated tunneling control [105, 117]; (5) system-level optimization, such as codesign of TFETs with non-von Neumann architectures to exploit their ultra-low leakage and steep *SS*, and integration with

energy-harvesting systems for self-powered nanodevices in wearable and biomedical applications [129–133].

While significant hurdles remain, the convergence of materials innovation, atomic-scale fabrication, and quantum-engineered device architectures positions TFETs as a cornerstone of next-generation electronics. Realizing their full potential demands sustained collaboration across academia and industry, with a focus on translating lab-scale breakthroughs into manufacturable technologies. As synthesis techniques mature and device physics is further unraveled, TFETs could redefine the energy landscape of computing, enabling sustainable growth in the AI-driven, hyperconnected world. In fact, TFET has been used in some commercial electronic devices, such as the current mode logic (CML) style light-weight ciphers [134], multi-valued logic (MVL) devices [135, 136], and so forth, making TFET far ahead of other beyond-CMOS devices in application prospects. In summary, this review not only consolidates the current state of TFET research but also charts a roadmap for overcoming existing barriers, ultimately paving the way for their adoption in mainstream semiconductor technology. The journey from Boltzmann-limited switches to quantum-tunneling-enabled ultra-efficient electronics is poised to reshape the future of information technology.

Author Contributions

All authors contributed to the literature search and writing of the manuscript.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The authors declare that the data supporting this study are available within the paper.

References

1. M. M. Waldrop, "The Chips Are Down for Moore's Law," *Nature* 530, no. 7589 (2016): 144–147.

2. International Roadmap for Devices and Systems (IRDS™) 2023 Update (IEEE, 2023), https://irds.ieee.org/editions/2023.

3. S. Cristoloveanu, J. Wan, and A. Zaslavsky, "A Review of Sharp-Switching Devices for Ultra-Low Power Applications," *IEEE Journal of the Electron Devices Society* 4, no. 5 (2016): 215–226.

4. D. E. Nikonov and I. A. Young, "Overview of Beyond-CMOS Devices and a Uniform Methodology for Their Benchmarking," *Proceedings of the IEEE* 101, no. 12 (2013): 2498–2533.

5. E. O. Kane, "Zener Tunneling in Semiconductors," *Journal of Physics and Chemistry of Solids* 12, no. 2 (1960): 181–188.

6. M. Luisier and G. Klimeck, "Simulation of Nanowire Tunneling Transistors: From the Wentzel–Kramers–Brillouin Approximation to Full-Band Phonon-Assisted Tunneling," *Journal of Applied Physics* 107, no. 8 (2010): 084507.

7. J. Appenzeller, Y. M. Lin, J. Knoch, and P. Avouris, "Band-To-Band Tunneling in Carbon Nanotube Field-Effect Transistors," *Physical Review Letters* 93, no. 19 (2004): 196805.

8. H. Lu and A. Seabaugh, "Tunnel Field-Effect Transistors: State-Of-The-Art," *IEEE Journal of the Electron Devices Society* 2, no. 4 (2014): 44–49.

9. A. M. Ionescu and H. Riel, "Tunnel Field-Effect Transistors as Energy-Efficient Electronic Switches," *Nature* 479, no. 7373 (2011): 329–337.

10. U. E. Avci, D. H. Morris, and I. A. Young, "Tunnel Field-Effect Transistors: Prospects and Challenges," *IEEE Journal of the Electron Devices Society* 3, no. 3 (2015): 88–95.

11. D. Esseni, M. Pala, P. Palestri, C. Alper, and T. Rollo, "A Review of Selected Topics in Physics Based Modeling for Tunnel Field-Effect Transistors," *Semiconductor Science and Technology* 32, no. 8 (2017): 083005.

12. G. Nazir, A. Rehman, and S.-J. Park, "Energy-Efficient Tunneling Field-Effect Transistors for Low-Power Device Applications: Challenges and Opportunities," *ACS Applied Materials & Interfaces* 12, no. 42 (2020): 47127–47163.

13. S. Kanungo, G. Ahmad, P. Sahatiya, A. Mukhopadhyay, and S. Chattopadhyay, "2D Materials-Based Nanoscale Tunneling Field Effect Transistors: Current Developments and Future Prospects," *npj 2D Materials and Applications* 6, no. 1 (2022): 83.

14. A. H. Bayani, J. Voves, and D. Dideban, "Effective Mass Approximation Versus Full Atomistic Model to Calculate the Output Characteristics of a Gate-All-Around Germanium Nanowire Field Effect Transistor (GAA-GeNW-FET)," *Superlattices and Microstructures* 113 (2018): 769–776.

15. J. L. P. J. van der Steen, D. Esseni, P. Palestri, L. Selmi, and R. J. E. Hueting, "Validity of the Parabolic Effective Mass Approximation in Silicon and Germanium n-MOSFETs With Different Crystal Orientations," *IEEE Transactions on Electron Devices* 54, no. 8 (2007): 1843–1851.

16. Y.-S. Kim, M. Marsman, G. Kresse, F. Tran, and P. Blaha, "Towards Efficient Band Structure and Effective Mass Calculations for III–V Direct Band-Gap Semiconductors," *Physical Review B* 82, no. 20 (2010): 205212.

17. M. Chhowalla, D. Jena, and H. Zhang, "Two-Dimensional Semiconductors for Transistors," *Nature Reviews Materials* 1, no. 11 (2016): 16052.

18. P. Miró, M. Audiffred, and T. Heine, "An Atlas of Two-Dimensional Materials," *Chemical Society Reviews* 43, no. 18 (2014): 6537–6554.

19. M. Rudan, *Physics of Semiconductor Devices* (Springer, 2015).

20. A. Beckers, F. Jazaeri, and C. Enz, "Theoretical Limit of Low Temperature Subthreshold Swing in Field-Effect Transistors," *IEEE Electron Device Letters* 41, no. 2 (2020): 276–279.

21. S. Sahay and M. J. Kumar, "Insight Into Lateral Band-To-Band-Tunneling in Nanowire Junctionless FETs," *IEEE Transactions on Electron Devices* 63, no. 10 (2016): 4138–4142.

22. F. Chen, H. Ilatikhameneh, Y. Tan, G. Klimeck, and R. Rahman, "Switching Mechanism and the Scalability of Vertical-TFETs," *IEEE Transactions on Electron Devices* 65, no. 7 (2018): 3065–3068.

23. W. Cao, D. Sarkar, Y. Khatami, J. Kang, and K. Banerjee, "Subthreshold-Swing Physics of Tunnel Field-Effect Transistors," *AIP Advances* 4, no. 6 (2014): 067141.

24. W. M. Weber and T. Mikolajick, "Silicon and Germanium Nanowire Electronics: Physics of Conventional and Unconventional Transistors," *Reports on Progress in Physics* 80, no. 6 (2017): 066502.

25. M. U. Haque and P. Vimala, "Boosting ON-current in tunnel FETs (TFETs): A Review," 2022 6th International Conference on Devices, Circuits and Systems (ICDCS) (2022): 294–298.

26. S. Mookerjea, R. Krishnan, S. Datta, and V. Narayanan, "Effective Capacitance and Drive Current for Tunnel FET (TFET) CV/I Estimation," *IEEE Transactions on Electron Devices* 56, no. 9 (2009): 2092–2098.

27. R. N. Sajjad, W. Chern, J. L. Hoyt, and D. A. Antoniadis, "Trap Assisted Tunneling and Its Effect on Subthreshold Swing of Tunnel FETs," *IEEE Transactions on Electron Devices* 63, no. 11 (2016): 4380–4387.

28. W. G. Vandenberghe, A. S. Verhulst, B. Sorée, et al., "Figure of Merit for and Identification of Sub-60 mV/Decade Devices," *Applied Physics Letters* 102, no. 1 (2013): 013510.

29. M. O. Li, D. Esseni, J. J. Nahas, D. Jena, and H. G. Xing, "Two-Dimensional Heterojunction Interlayer Tunneling Field Effect Transistors (Thin-TFETs)," *IEEE Journal of the Electron Devices Society* 3, no. 3 (2015): 200–207.

30. R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, "Vertical Si-Nanowire n-Type Tunneling FETs With Low Subthreshold Swing (≤ 50 mV/decade) at Room Temperature," *IEEE Electron Device Letters* 32, no. 4 (2011): 437–439.

31. Y. Shao, M. Pala, H. Tang, et al., "Scaled Vertical-Nanowire Heterojunction Tunnelling Transistors With Extreme Quantum Confinement," *Nature Electronics* 8, no. 2 (2025): 157–167.

32. X. Zhao, A. Vardi, and J. A. del Alamo, "Sub-Thermal Subthreshold Characteristics in Top–Down InGaAs/InAs Heterojunction Vertical Nanowire Tunnel FETs," *IEEE Electron Device Letters* 38, no. 7 (2017): 855–858.

33. D. Sarkar, X. Xie, W. Liu, et al., "A Subthermionic Tunnel Field-Effect Transistor With an Atomically Thin Channel," *Nature* 526, no. 7571 (2015): 91–95.

34. J. Miao, C. Leblanc, J. Wang, et al., "Heterojunction Tunnel Triodes Based on Two-Dimensional Metal Selenide and Three-Dimensional Silicon," *Nature Electronics* 5, no. 11 (2022): 744–751.

35. N. T. Duong, C. Park, D. H. Nguyen, et al., "Gate-Controlled $MoTe_2$ Homojunction for Sub-Thermionic Subthreshold Swing Tunnel Field-Effect Transistor," *Nano Today* 40 (2021): 101263.

36. S. Kim, G. Myeong, W. Shin, et al., "Thickness-Controlled Black Phosphorus Tunnel Field-Effect Transistor for Low-Power Switches," *Nature Nanotechnology* 15, no. 3 (2020): 203–206.

37. N. Oliva, J. Backman, L. Capua, M. Cavalieri, M. Luisier, and A. M. Ionescu, "$WSe_2/SnSe_2$ vdW Heterojunction Tunnel Fet With Subthermionic Characteristic and MOSFET Co-Integrated on Same WSe_2 Flake," *npj 2D Materials and Applications* 4, no. 1 (2020): 5.

38. L. Liao, Y.-C. Lin, M. Bao, et al., "High-Speed Graphene Transistors With a Self-Aligned Nanowire Gate," *Nature* 467, no. 7313 (2010): 305–308.

39. Y. Liu, J. Guo, E. Zhu, et al., "Approaching the Schottky–Mott Limit in van der Waals Metal–Semiconductor Junctions," *Nature* 557, no. 7707 (2018): 696–700.

40. P. Chen, T. L. Atallah, Z. Lin, et al., "Approaching the Intrinsic Exciton Physics Limit in Two-Dimensional Semiconductor Diodes," *Nature* 599, no. 7885 (2021): 404–410.

41. C. Woo Young Choi, P. Byung-Gook Park, L. Jong Duk Lee, and L. Tsu-Jae King Liu, "Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec," *IEEE Electron Device Letters* 28, no. 8 (2007): 743–745.

42. Y.-C. Yeo, G. Han, Y. Yang, and P. Guo, "Invited Strain Engineering and Junction Design for Tunnel Field-Effect Transistor," *ECS Transactions* 33, no. 6 (2010): 77–87.

43. K. Tomioka, M. Yoshimura, and T. Fukui, "Steep-Slope Tunnel Field-Effect Transistors Using III–V Nanowire/Si Heterojunction," 2012 Symposium on VLSI Technology (VLSIT) (2012), 47–48.

44. L. Lattanzio, L. De Michielis, and A. M. Ionescu, "The Electron–Hole Bilayer Tunnel FET," *Solid-State Electronics* 74 (2012): 85–90.

45. B. Ganjipour, A. W. Dey, B. M. Borg, et al., "High Current Density Esaki Tunnel Diodes Based on GaSb-InAsSb Heterostructure Nanowires," *Nano Letters* 11, no. 10 (2011): 4222–4226.

46. E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L. E. Wernersson, "Vertical InAs/GaAsSb/GaSb Tunneling Field-Effect Transistor on Si With S = 48 mV/decade and I_{on} = 10 μA/μm for I_{off} = 1 nA/μm at V_{ds} = 0.3 V," 2016 IEEE International Electron Devices Meeting (IEDM) (2016): 19.1.1–19.1.4.

47. R. M. Iutzi and E. A. Fitzgerald, "Microstructure and Conductance-Slope of InAs/GaSb Tunnel Diodes," *Journal of Applied Physics* 115, no. 23 (2014): 234503.

48. F. Conzatti, M. G. Pala, D. Esseni, E. Bano, and L. Selmi, "Strain-Induced Performance Improvements in InAs Nanowire Tunnel FETs," *IEEE Transactions on Electron Devices* 59, no. 8 (2012): 2085–2092.

49. J.-S. Liu, Y. Zhu, P. S. Goley, and M. K. Hudait, "Heterointerface Engineering of Broken-Gap InAs/GaSb Multilayer Structures," *ACS Applied Materials & Interfaces* 7, no. 4 (2015): 2512–2517.

50. E. Memisevic, M. Hellenbrand, E. Lind, et al., "Individual Defects in InAs/InGaAsSb/GaSb Nanowire Tunnel Field-Effect Transistors Operating Below 60 mV/Decade," *Nano Letters* 17, no. 7 (2017): 4373–4380.

51. J. Madan and R. Chaujar, "Interfacial Charge Analysis of Heterogeneous Gate Dielectric-Gate All Around-Tunnel FET for Improved Device Reliability," *IEEE Transactions on Device and Materials Reliability* 16, no. 2 (2016): 227–234.

52. D. Das and C. K. Pandey, "Interfacial Trap Charge and Self-Heating Effect Based Reliability Analysis of a Dual-Drain Vertical Tunnel FET," *Microelectronics Reliability* 146 (2023): 115024.

53. G. Dewey, B. Chu-Kung, J. Boardman, et al., "Fabrication, Characterization, and Physics of III–V Heterojunction Tunneling Field Effect Transistors (H-TFET) for Steep Sub-Threshold Swing," 2011 International Electron Devices Meeting (2011): 33.6.1–33.6.4.

54. E. Ko, H. Lee, J. D. Park, and C. Shin, "Vertical Tunnel FET: Design Optimization With Triple Metal-Gate Layers," *IEEE Transactions on Electron Devices* 63, no. 12 (2016): 5030–5035.

55. K. Tomioka, T. Tanaka, S. Hara, K. Hiruma, and T. Fukui, "III–V Nanowires on Si Substrate: Selective-Area Growth and Device Applications," *IEEE Journal of Selected Topics in Quantum Electronics* 17, no. 4 (2011): 1112–1129.

56. A. Kikuchi, R. Bannai, K. Kishino, C.-M. Lee, and J.-I. Chyi, "AlN/GaN Double-Barrier Resonant Tunneling Diodes Grown by RF-Plasma-Assisted Molecular-Beam Epitaxy," *Applied Physics Letters* 81, no. 9 (2002): 1729–1731.

57. K. Ploog, "Delta- (δ-) Doping in MBE-Grown GaAs: Concept and Device Application," *Journal of Crystal Growth* 81, no. 1 (1987): 304–313.

58. A. S. Verhulst, B. Sorée, D. Leonelli, W. G. Vandenberghe, and G. Groeseneken, "Modeling the Single-Gate, Double-Gate, and Gate-All-Around Tunnel Field-Effect Transistor," *Journal of Applied Physics* 107, no. 2 (2010): 024518.

59. R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, "CMOS-Compatible Vertical-Silicon-Nanowire Gate-All-Around p-Type Tunneling FETs With ≤50-mV/decade Subthreshold Swing," *IEEE Electron Device Letters* 32, no. 11 (2011): 1504–1506.

60. N. Kumar, U. Mushtaq, S. I. Amin, and S. Anand, "Design and Performance Analysis of Dual-Gate All Around Core-Shell Nanotube TFET," *Superlattices and Microstructures* 125 (2019): 356–364.

61. Y. Xu, B. Shen, D. Wang, et al. "Study of Synthetic Electric Field Effects and Quantum Confinement Effects in Extremely Scaled Gate-all-Around Tunnel FET," 2022 IEEE 16th International Conference on Solid-State & Integrated Circuit Technology (ICSICT) (2022): 1–3.

62. A. N. Hanna, H. M. Fahad, and M. M. Hussain, "InAs/Si Hetero-Junction Nanotube Tunnel Transistors," *Scientific Reports* 5, no. 1 (2015): 9843.

63. Y. Yue Yang, T. Xin Tong, Y. Li-Tao yang, G. Peng-Fei guo, F. Lu Fan, and Y. Yee-Chia yeo, "Tunneling Field-Effect Transistor:

Capacitance Components and Modeling," *IEEE Electron Device Letters* 31, no. 7 (2010): 752–754.

64. A. Chattopadhyay and A. Mallik, "Impact of a Spacer Dielectric and a Gate Overlap/Underlap on the Device Performance of a Tunnel Field-Effect Transistor," *IEEE Transactions on Electron Devices* 58, no. 3 (2011): 677–683.

65. A. Chauhan, G. Saini, and P. K. Yerur, "Improving the Performance of Dual-*k* Spacer Underlap Double Gate TFET," *Superlattices and Microstructures* 124 (2018): 79–91.

66. C. K. Pandey, D. Dash, and S. Chaudhury, "Approach to Suppress Ambipolar Conduction in Tunnel FET Using Dielectric Pocket," *Micro & Nano Letters* 14, no. 1 (2019): 86–90.

67. H. Ilatikhameneh, T. A. Ameen, G. Klimeck, J. Appenzeller, and R. Rahman, "Dielectric Engineered Tunnel Field-Effect Transistor," *IEEE Electron Device Letters* 36, no. 10 (2015): 1097–1100.

68. A. Saeidi, T. Rosca, E. Memisevic, et al., "Nanowire Tunnel FET With Simultaneously Reduced Subthermionic Subthreshold Swing and Off-Current Due to Negative Capacitance and Voltage Pinning Effects," *Nano Letters* 20, no. 5 (2020): 3255–3262.

69. H. Liu, X. Zhou, P. Li, et al., "A Symmetric Heterogate Dopingless Electron-Hole Bilayer TFET With Ferroelectric and Barrier Layers," *Physica Scripta* 99, no. 8 (2024): 085007.

70. A. A. M. Mazumder, K. Hosen, M. S. Islam, and J. Park, "Numerical Investigations of Nanowire Gate-All-Around Negative Capacitance GaAs/InN Tunnel FET," *IEEE Access* 10 (2022): 30323–30334.

71. P. Wu and J. Appenzeller, "Design Considerations for 2-D Dirac-Source FETs—Part II: Nonidealities and Benchmarking," *IEEE Transactions on Electron Devices* 69, no. 8 (2022): 4681–4685.

72. W. Gan, K. Luo, G. Qi, et al., "A Multiscale Simulation Framework for Steep-Slope Si Nanowire Cold Source FET," *IEEE Transactions on Electron Devices* 68, no. 11 (2021): 5455–5461.

73. G. Peng-Fei guo, Y. Li-Tao yang, Y. Yue Yang, et al., "Tunneling Field-Effect Transistor: Effect of Strain and Temperature on Tunneling Current," *IEEE Electron Device Letters* 30, no. 9 (2009): 981–983.

74. T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With Record High Drive Currents and ≪60 mV/dec Subthreshold Slope," 2008 IEEE International Electron Devices Meeting (2008): 1–3.

75. A. Villalon, C. L. Royer, M. Cassé, et al. "Strained Tunnel FETs With Record ION: First Demonstration of ETSOI TFETs With SiGe Channel and RSD," 2012 Symposium on VLSI Technology (VLSIT) (2012): 49–50.

76. M. Velický and P. S. Toth, "From Two-Dimensional Materials to Their Heterostructures: An Electrochemist's Perspective," *Applied Materials Today* 8 (2017): 68–103.

77. S.-C. Lu, M. Mohamed, and W. Zhu, "Novel Vertical Hetero- and Homo-Junction Tunnel Field-Effect Transistors Based on Multi-Layer 2D Crystals," *2D Materials* 3, no. 1 (2016): 011010.

78. J. Cao, D. Logoteta, S. Ozkaya, et al., "Operation and Design of van der Waals Tunnel Transistors: A 3-D Quantum Transport Study," *IEEE Transactions on Electron Devices* 63, no. 11 (2016): 4388–4394.

79. H. Ilatikhameneh, G. Klimeck, J. Appenzeller, and R. Rahman, "Design Rules for High Performance Tunnel Transistors From 2-D Materials," *IEEE Journal of the Electron Devices Society* 4, no. 5 (2016): 260–265.

80. T. Agarwal, G. Fiori, B. Soree, I. Radu, M. Heyns, and W. Dehaene, "Material-Device-Circuit Co-Design of 2-D Materials-Based Lateral Tunnel FETs," *IEEE Journal of the Electron Devices Society* 6 (2018): 979–986.

81. T. K. Agarwal, A. Nourbakhsh, P. Raghavan, et al., "Bilayer Graphene Tunneling FET for sub-0.2 V Digital CMOS Logic Applications," *IEEE Electron Device Letters* 35, no. 12 (2014): 1308–1310.

82. G. Fiori and G. Iannaccone, "Ultralow-Voltage Bilayer Graphene Tunnel FET," *IEEE Electron Device Letters* 30, no. 10 (2009): 1096–1098.

83. H. Ilatikhameneh, Y. Tan, B. Novakovic, G. Klimeck, R. Rahman, and J. Appenzeller, "Tunnel Field-Effect Transistors in 2-D Transition Metal Dichalcogenide Materials," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits* 1 (2015): 12–18.

84. X.-W. Jiang and S.-S. Li, "Performance Limits of Tunnel Transistors Based on Mono-Layer Transition-Metal Dichalcogenides," *Applied Physics Letters* 104, no. 19 (2014): 193510.

85. A. Nourbakhsh, T. K. Agarwal, A. Klekachev, et al., "Chemically Enhanced Double-Gate Bilayer Graphene Field-Effect Transistor With Neutral Channel for Logic Applications," *Nanotechnology* 25, no. 34 (2014): 345203.

86. M. C. Robbins, P. Golani, and S. J. Koester, "Right-Angle Black Phosphorus Tunneling Field Effect Transistor," *IEEE Electron Device Letters* 40, no. 12 (2019): 1988–1991.

87. F. W. Chen, H. Ilatikhameneh, G. Klimeck, Z. Chen, and R. Rahman, "Configurable Electrostatically Doped High Performance Bilayer Graphene Tunnel FET," *IEEE Journal of the Electron Devices Society* 4, no. 3 (2016): 124–128.

88. Y. Wang and M. Chhowalla, "Making Clean Electrical Contacts on 2D Transition Metal Dichalcogenides," *Nature Reviews Physics* 4, no. 2 (2022): 101–112.

89. P. V. Pham, S. C. Bodepudi, K. Shehzad, et al., "2D Heterostructures for Ubiquitous Electronics and Optoelectronics: Principles, Opportunities, and Challenges," *Chemical Reviews* 122, no. 6 (2022): 6514–6613.

90. I. Popov, G. Seifert, and D. Tománek, "Designing Electrical Contacts to MoS_2 Monolayers: A Computational Study," *Physical Review Letters* 108, no. 15 (2012): 156802.

91. L. Britnell, R. M. Ribeiro, A. Eckmann, et al., "Strong Light-Matter Interactions in Heterostructures of Atomically Thin Films," *Science* 340, no. 6138 (2013): 1311–1314.

92. C. Xi Cao and G. Jing Guo, "Simulation of Phosphorene Field-Effect Transistor at the Scaling Limit," *IEEE Transactions on Electron Devices* 62, no. 2 (2015): 659–665.

93. T. A. Ameen, H. Ilatikhameneh, G. Klimeck, and R. Rahman, "Few-Layer Phosphorene: An Ideal 2D Material for Tunnel Transistors," *Scientific Reports* 6, no. 1 (2016): 28515.

94. J. Seo, S. Jung, and M. Shin, "The Performance of Uniaxially Strained Phosphorene Tunneling Field-Effect Transistors," *IEEE Electron Device Letters* 38, no. 8 (2017): 1150–1152.

95. F. Liu, Q. Shi, J. Wang, and H. Guo, "Device Performance Simulations of Multilayer Black Phosphorus Tunneling Transistors," *Applied Physics Letters* 107, no. 20 (2015): 203501.

96. P. Wu, T. Ameen, H. Zhang, et al., "Complementary Black Phosphorus Tunneling Field-Effect Transistors," *ACS Nano* 13, no. 1 (2019): 377–385.

97. P. Wu and J. Appenzeller, "Reconfigurable Black Phosphorus Vertical Tunneling Field-Effect Transistor With Record High On-Currents," *IEEE Electron Device Letters* 40, no. 6 (2019): 981–984.

98. C. Gong, H. Zhang, W. Wang, L. Colombo, R. M. Wallace, and K. Cho, "Band Alignment of Two-Dimensional Transition Metal Dichalcogenides: Application in Tunnel Field Effect Transistors," *Applied Physics Letters* 103, no. 5 (2013): 053513.

99. V. O. Özçelik, J. G. Azadani, C. Yang, S. J. Koester, and T. Low, "Band Alignment of Two-Dimensional Semiconductors for Designing Heterostructures With Momentum Space Matching," *Physical Review B* 94, no. 3 (2016): 035125.

100. Y. Cai, G. Zhang, and Y.-W. Zhang, "Layer-Dependent Band Alignment and Work Function of Few-Layer Phosphorene," *Scientific Reports* 4, no. 1 (2014): 6677.

101. K. Cheng, Y. Guo, N. Han, Y. Su, J. Zhang, and J. Zhao, "Lateral Heterostructures of Monolayer Group-IV Monochalcogenides: Band Alignment and Electronic Properties," *Journal of Materials Chemistry C* 5, no. 15 (2017): 3788–3795.

102. Z. Guo, J. Zhou, L. Zhu, and Z. Sun, "MXene: A Promising Photocatalyst for Water Splitting," *Journal of Materials Chemistry A* 4, no. 29 (2016): 11446–11452.

103. Y. Liang, Y. Dai, Y. Ma, L. Ju, W. Wei, and B. Huang, "Novel Titanium Nitride Halide TiNX (X = F, Cl, Br) Monolayers: Potential Materials for Highly Efficient Excitonic Solar Cells," *Journal of Materials Chemistry A* 6, no. 5 (2018): 2073–2080.

104. W. Li, F. P. Sabino, F. Crasto de Lima, T. Wang, R. H. Miwa, and A. Janotti, "Large Disparity Between Optical and Fundamental Band Gaps in Layered In_2Se_3," *Physical Review B* 98, no. 16 (2018): 165134.

105. A. Szabo, C. Klinkert, D. Campi, C. Stieger, N. Marzari, and M. Luisier, "Ab Initio Simulation of Band-to-Band Tunneling FETs With Single- and Few-Layer 2-D Materials as Channels," *IEEE Transactions on Electron Devices* 65, no. 10 (2018): 4180–4187.

106. Z. Wu, Y. Lyu, Y. Zhang, et al., "Large-Scale Growth of Few-Layer Two-Dimensional Black Phosphorus," *Nature Materials* 20, no. 9 (2021): 1203–1209.

107. Y. Zhao, J. Mao, Z. Wu, et al., "A Clean Transfer Approach to Prepare Centimetre-Scale Black Phosphorus Crystalline Multilayers on Silicon Substrates for Field-Effect Transistors," *Nature Communications* 15, no. 1 (2024): 6795.

108. S. Kamaei, A. Saeidi, C. Gastaldi, et al., "Gate Energy Efficiency and Negative Capacitance in Ferroelectric 2D/2D TFET From Cryogenic to High Temperatures," *npj 2D Materials and Applications* 5, no. 1 (2021): 76.

109. C. Qiu, F. Liu, L. Xu, et al., "Dirac-Source Field-Effect Transistors as Energy-Efficient, High-Performance Electronic Switches," *Science* 361, no. 6400 (2018): 387–392.

110. X. Yan, C. Liu, C. Li, et al., "Tunable $SnSe_2/WSe_2$ Heterostructure Tunneling Field Effect Transistor," *Small* 13, no. 34 (2017): 1701478.

111. Y. Sato, T. Nishimura, D. Duanfei, et al., "Intrinsic Electronic Transport Properties and Carrier Densities in PtS_2 and $SnSe_2$: Exploration of n^+-Source for 2D Tunnel FETs," *Advanced Electronic Materials* 7, no. 12 (2021): 2100292.

112. J. He, N. Fang, K. Nakamura, et al., "2D Tunnel Field Effect Transistors (FETs) With a Stable Charge-Transfer-Type P^+-WSe_2 Source," *Advanced Electronic Materials* 4, no. 7 (2018): 1800207.

113. X. Jiang, X. Shi, M. Zhang, et al., "A Symmetric Tunnel Field-Effect Transistor Based on MoS_2/Black Phosphorus/MoS_2 Nanolayered Heterostructures," *ACS Applied Nano Materials* 2, no. 9 (2019): 5674–5680.

114. H. Zhang, W. Cao, J. Kang, and K. Banerjee, "Effect of Band-tails on the Subthreshold Performance of 2D Tunnel-FETs." 2016 IEEE International Electron Devices Meeting (IEDM) (2016): 30.3.1–30.3.4.

115. Q. Zhang, Y. Xiong, Y. Gao, J. Chen, W. Hu, and J. Yang, "First-Principles High-Throughput Inverse Design of Direct Momentum-Matching Band Alignment van der Waals Heterostructures Utilizing Two-Dimensional Indirect Semiconductors," *Nano Letters* 24, no. 12 (2024): 3710–3718.

116. Y.-J. Zhang, Y.-T. Ren, X.-H. Lv, et al., "Momentum Matching and Band-Alignment Type in van der Waals Heterostructures: Interfacial Effects and Materials Screening," *Physical Review B* 107, no. 23 (2023): 235420.

117. W. Zhou, H. Qu, S. Guo, et al., "Dependence of Tunneling Mechanism on Two-Dimensional Material Parameters: A High-Throughput Study," *Physical Review Applied* 17, no. 6 (2022): 064053.

118. C. Huang, S. Wu, A. M. Sanchez, et al., "Lateral Heterojunctions Within Monolayer $MoSe_2$–WSe_2 Semiconductors," *Nature Materials* 13, no. 12 (2014): 1096–1101.

119. X. Duan, C. Wang, J. C. Shaw, et al., "Lateral Epitaxial Growth of Two-Dimensional Layered Semiconductor Heterojunctions," *Nature Nanotechnology* 9, no. 12 (2014): 1024–1030.

120. H. Bergeron, D. Lebedev, and M. C. Hersam, "Polymorphism in Post-Dichalcogenide Two-Dimensional Materials," *Chemical Reviews* 121, no. 4 (2021): 2713–2775.

121. J. Yu, C.-Y. Xu, F.-X. Ma, S.-P. Hu, Y.-W. Zhang, and L. Zhen, "Monodisperse SnS_2 Nanosheets for High-Performance Photocatalytic Hydrogen Generation," *ACS Applied Materials & Interfaces* 6, no. 24 (2014): 22370–22377.

122. P. G. D. Agopian, J. A. Martino, A. Vandooren, et al., "Study of Line-TFET Analog Performance Comparing With Other TFET and MOSFET Architectures," *Solid-State Electronics* 128 (2017): 43–47.

123. J. Yu, W. Han, A. A. Suleiman, S. Han, N. Miao, and F. C.-C. Ling, "Recent Advances on Pulsed Laser Deposition of Large-Scale Thin Films," *Small Methods* 8, no. 7 (2024): 2301282.

124. P. M. Campbell, J. K. Smith, W. J. Ready, and E. M. Vogel, "Material Constraints and Scaling of 2-D Vertical Heterostructure Interlayer Tunnel Field-Effect Transistors," *IEEE Transactions on Electron Devices* 64, no. 6 (2017): 2714–2720.

125. J. Cao, D. Logoteta, M. G. Pala, and A. Cresti, "Impact of Momentum Mismatch on 2D van der Waals Tunnel Field-Effect Transistors," *Journal of Physics D: Applied Physics* 51, no. 5 (2018): 055102.

126. H. Li, P. Xu, L. Xu, Z. Zhang, and J. Lu, "Negative Capacitance Tunneling Field Effect Transistors Based on Monolayer Arsenene, Antimonene, and Bismuthene," *Semiconductor Science and Technology* 34, no. 8 (2019): 085006.

127. W. Gonçalez Filho, E. Simoen, R. Rooyackers, et al., "Analog Design With Line-TFET Device Experimental Data: From Device to Circuit Level," *Semiconductor Science and Technology* 35, no. 5 (2020): 055025.

128. Z. Yang, Z. Wu, Y. Lyu, and J. Hao, "Centimeter-Scale Growth of Two-Dimensional Layered High-Mobility Bismuth Films by Pulsed Laser Deposition," *InfoMat* 1, no. 1 (2019): 98–107.

129. B. Rawat and R. Paily, "Analysis of Graphene Tunnel Field-Effect Transistors for Analog/RF Applications," *IEEE Transactions on Electron Devices* 62, no. 8 (2015): 2663–2669.

130. G. Alymov, V. Vyurkov, V. Ryzhii, and D. Svintsov, "Abrupt Current Switching in Graphene Bilayer Tunnel Transistors Enabled by van Hove Singularities," *Scientific Reports* 6, no. 1 (2016): 24654.

131. Q. Zhang, G. Iannaccone, and G. Fiori, "Two-Dimensional Tunnel Transistors Based on Bi_2Se_3 Thin Film," *IEEE Electron Device Letters* 35, no. 1 (2014): 129–131.

132. G. V. Resta, A. Leonhardt, Y. Balaji, S. De Gendt, P. E. Gaillardon, and G. De Micheli, "Devices and Circuits Using Novel 2-D Materials: A Perspective for Future VLSI Systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 27, no. 7 (2019): 1486–1503.

133. J. Chang, L. F. Register, and S. K. Banerjee, "Possible Applications of Topological Insulator Thin Films for Tunnel FETs," in *70th Device Research Conference* (IEEE, 2012), 31–32.

134. Y. Bi, K. Shamsi, J. S. Yuan, Y. Jin, M. Niemier, and X. S. Hu, "Tunnel FET Current Mode Logic for DPA-Resilient Circuit Designs," *IEEE Transactions on Emerging Topics in Computing* 5, no. 3 (F2017): 340–352.

135. A. Nourbakhsh, A. Zubair, M. S. Dresselhaus, and T. Palacios, "Transport Properties of a MoS_2/WSe_2 Heterojunction Transistor and Its Potential for Application," *Nano Letters* 16, no. 2 (2016): 1359–1366.

136. J. Shim, S. Oh, D.-H. Kang, et al., "Phosphorene/Rhenium Disulfide Heterojunction-Based Negative Differential Resistance Device for Multi-Valued Logic," *Nature Communications* 7, no. 1 (2016): 13413.