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# Digital Current Control for Permanent Magnet Synchronous Machine Drives with Fractional-Step Computation Delay

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***Abstract*—This paper proposes a digital current controller for permanent magnet synchronous machine (PMSM) drives, specifically addressing scenarios where the computation delay is a fraction of the sampling period. The fractional-step computation delay introduces a transmission zero in the discrete-time PMSM model, causing undesirable coupling between dq-axes currents. The proposed controller employs complementary zero assignment to ensure decoupled current dynamics and incorporates a dual-update strategy to enhance transient performance. Active resistance is also utilized to improve disturbance rejection. The controller integrates seamlessly with asymmetrical regular-sampled pulse-width modulation and supports operation at lower sampling frequencies without compromising performance, thereby reducing computational burden. This makes it particularly suitable for transportation electrification applications demanding high switching frequencies and precise current regulation. Experimental results from a laboratory-based PMSM test setup validate the effectiveness of the proposed method.**

***Index Terms*—Digital control, discrete-time, decoupling, PMSM.**

## NOMENCLATURE

| | |
|---|---|
| $i_{dq} = [i_d, i_q]^T$ | $dq$-axes currents |
| $u_{dq} = [u_d, u_q]^T$ | $dq$-axes voltages |
| $e_{dq} = [e_d, e_q]^T$ | $dq$-axes back-EMF voltages |
| $u^*_{dq} = [u^*_d, u^*_q]^T$ | $dq$-axes voltage commands for controller |
| $R_s$ | Stator resistance per phase |
| $L_d, L_q$ | $dq$-axes inductances |
| $\omega_e, \theta_e$ | Electrical rotational speed and position |
| $T_s, f_s$ | Sampling period and frequency |
| $T_{sw}, f_{sw}$ | Switching period and frequency |
| $T_h = T_s/n$ | Sub-control period, $n$ is an integer |
| $T_c = mT_h$ | Computation delay, $m$ is an integer |
| $I$ | Unit matrix |

This paper denotes $J = \begin{bmatrix}0 & -1\\ 1 & 0\end{bmatrix}$ and the matrix exponential $e^{J\alpha}$ gives $e^{J\alpha} = \begin{bmatrix}\cos\alpha & -\sin\alpha\\ \sin\alpha & \cos\alpha\end{bmatrix}$. The variable at the time instant $(k + i/n)T_s$ is denoted by a fractional index $k + i/n$, $i = 0, 1, ..., n-1$, e.g., $u_{dq}(k + i/n)$.

## I. INTRODUCTION

CURRENT control is critical to the overall performance of electric drives, particularly in transportation electrification applications demanding precise torque regulation, high efficiency, and high power density, and continues to receive significant attention from academia and industry [1], [2]. In terms of feedback control characteristics, the digital delay in motor drives limits the bandwidth and stability margin of the current loop, encompassing both modulation and computation delays [3]. The computation delay arises from the non-zero time required to execute control algorithms, while the modulation delay results from the volt-second contribution of the pulse-width modulation (PWM) process.

Various strategies have been pursued to mitigate digital delay and enhance current control performance. For a given switching frequency, increasing the sampling frequency is a direct way. Traditional single-sampling (SS) and dual-sampling (DS) schemes lead to a computation delay of one sampling period $T_s$, with DS offering a higher sampling rate. Multi-sampling (MS) techniques have further advanced current control dynamics [4], but they often face challenges related to aliasing and switching noise, particularly in three-phase systems [5]. Model predictive control with finite control sets allows for a much higher sampling frequency than the switching frequency [6]. Alternatively, optimizing the PWM updating sequence can minimize delay. Real-time PWM methods that update immediately after sampling can eliminate computation delay [7], while they demand very fast sensing and suffer from limited PWM duty ranges, potentially restricting voltage output capability. In practical motor drives, the aforementioned methods may be inapplicable due to insufficient computational resources or specific topologies. Some low-cost inverters sample currents through shunt resistors at intervals determined by the PWM waveform [8]. In this configuration, only the SS scheme can be used, and a minimum half-step computation delay is achievable.

With the widespread adoption of wide-bandgap semiconductors, the switching frequency of motor drives can reach

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hundreds of kHz or even MHz [9], [10]. While multi-core microcontroller unit (MCU) or field-programmable gate array (FPGA) can manage the computational burden associated with higher frequencies, they increase cost and complexity [11]. Multi-rate or single-sampling-multiple-updating (SSMU) schemes, which combine multiple switching periods into one control period, may offer a practical solution to alleviate the computational load [12]. Given that MCUs must reserve time for lower-priority tasks such as communication and diagnosis, the actual time available for executing the control algorithm is less than the sampling period. Consequently, the computation delay in SSMU schemes can be shortened to a fraction of the sampling period due to multiple update opportunities. This fractional-step computation delay (FSCD) presents unique challenges for high-performance control.

In the current control of permanent magnet synchronous machines (PMSMs) and synchronous reluctance machines (SynRMs), discrete-time current regulators have demonstrated superiority over their continuous-time counterparts, exhibiting higher bandwidth, better decoupling between $d$- and $q$-axes, and stronger stability over a wide speed range [13]–[21]. However, most existing current control methods are developed for a computation delay equal to $T_s$, including PI control [14]–[18], deadbeat control [19], model predictive control [20], and disturbance observer-based control [21]. These methods can achieve zero steady-state error, fast response, and decoupled $dq$-axes current dynamics over a wide speed range under the assumption of integer-step delay.

For the FSCD that may exist in SSMU or conventional SS schemes, very few studies address current control in the discrete-time domain. FSCD leads to a transmission zero in the discrete-time PMSM drive model, resulting in undesirable coupling between the $d$- and $q$-axes currents, which degrades torque control accuracy and dynamic performance [22]. Since this transmission zero cannot be shifted by feedback control strategies such as pole placement, it poses a fundamental challenge. For the half-step computation delay (HSCD), [23] proposes a single-sampling-dual-updating scheme that can decouple $dq$-axes current dynamics even when the ratio of sampling to fundamental frequency is as low as 6. [24] discusses damped current control with HSCD and error-free feedback acquisition. The work in [25] designs a general current controller for FSCD; however, the zero issue and its detrimental impact on decoupling performance are overlooked, and $dq$-axes interaction is observed in experiments.

To overcome these limitations and provide a robust solution for high-performance PMSM drives operating under FSCD, particularly relevant for modern transportation electrification systems utilizing high switching frequencies or facing computational constraints, this paper proposes a digital current control specifically designed for PMSM drives with FSCD and presents the following contributions:

- A decoupling approach effective across arbitrary FSCD scenarios and various voltage update patterns discussed herein, even at low sampling frequencies.
- Seamless integration with asymmetrical regular-sampled PWM to achieve an optimized spectrum, even when the sampling frequency is lower than the switching frequency.
- Flexibility to reduce the computational burden for PMSM drives operating at high switching frequencies without compromising control performance due to FSCD.

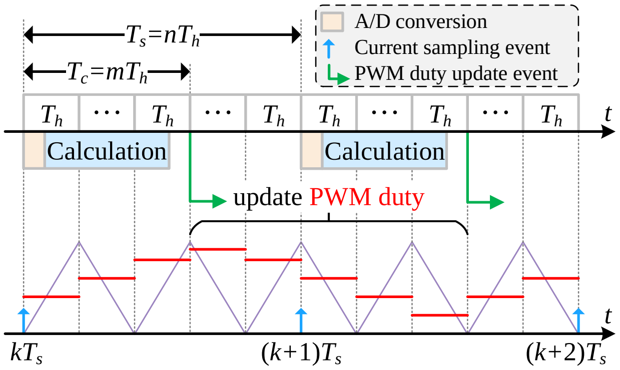


Fig. 1. Conceptual voltage update scheme. The sampling period $T_s$ is divided into $n$ sub-control periods $T_h$. Each $T_h$ can be assigned an independent duty cycle for modulation. After current sampling, the A/D conversion and calculation are completed within the computation delay $T_c = mT_h$. Then, $n$ duty references are updated for the following $n$ sub-control periods.

The rest of this paper is organized as follows. Section II models PMSM drives with FSCD. Section III details the design of the proposed digital current control. Section IV discusses implementation considerations. Section V validates the proposed method through experimental results. Finally, Section VI concludes the paper.

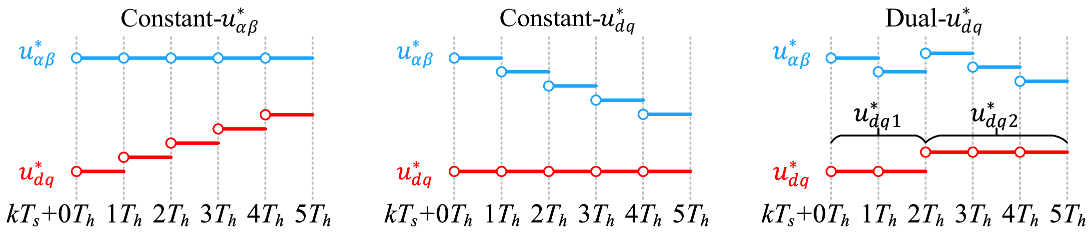
## II. MODELING OF PMSM DRIVES

### A. Time Sequence and Digital Delay Considerations

In PWM-controlled PMSM drives, current sampling is typically synchronized with the carrier peak and/or valley to minimize aliasing. To allow sufficient time for analog-to-digital (A/D) conversion and control algorithm execution, the PWM reference update is delayed, resulting in the computation delay. This computation delay, $T_c$, combined with the modulation delay, constitutes the total digital delay, $T_d$.

The computation delay depends on the PWM updating scheme. This paper focuses on scenarios where the computation delay $T_c$ is a fraction of the sampling period $T_s$. Fig. 1 illustrates the conceptual scheme for updating voltage references. The sampling period $T_s$ is divided into $n$ sub-control periods ($T_s = nT_h$), where $T_h$ equals one or half of the switching period $T_{sw}$. During each $T_h$, modulation is modeled as a zero-order hold (ZOH) voltage latch. Independent voltage references can be assigned to each sub-control periods.

The sampling and calculation process is assumed to complete within the computation delay $T_c = mT_h$, where $m$ is an integer and $m \leq n$. The parameter $m$ is selected to ensure the execution of the control algorithm within the allowable time for definitive real-time performance. A lower $m$ reflects a shorter computation delay and consequently a higher stability margin while requires stronger computational resources. Once the calculations are completed at the time instant $kT_s+T_c$, the $n$ voltage references for the subsequent $n$ sub-control periods, spanning from $kT_s + T_c$ to $(k + 1)T_s + T_c$, are updated. Consequently, the computation delay is modeled as a pure



(a) (b) (c)

Fig. 2. Voltage reference patterns in a control period. This is an example for $n = 5$ and $m = 3$. (a) Constant-$u^*_{\alpha\beta}$. (b) Constant-$u^*_{dq}$. (c) Dual-$u^*_{dq}$. For simplicity, $u^*_{\alpha\beta}$ or $u^*_{dq}$ in a sub-period is represented by a single line starting with a circle. Noting that actual voltage $u_{\alpha\beta}$ lags $u^*_{\alpha\beta}$ by $mT_h$.

delay between the $\alpha\beta$-axes voltage reference $u^*_{\alpha\beta}$ and the actual voltage $u_{\alpha\beta}$, expressed as:

$$u_{\alpha\beta}\left(k+\frac{i}{n}\right) = u^*_{\alpha\beta}\left(k+\frac{i-m}{n}\right). \tag{1}$$

Noting that the conventional voltage update scheme ($T_c = T_s$) is a special case of this study with $n = m = 1$.

### B. Voltage Reference Pattern Allocation

Within a control period, the method of allocating voltage references to the inverter over the $n$ sub-control periods impacts the PWM spectrum and current dynamics. This paper considers the following three patterns for allocating the voltage references.

1) Constant-$u^*_{\alpha\beta}$ pattern: In this pattern, the $\alpha\beta$-axes voltage reference $u^*_{\alpha\beta}$ is held constant over the entire control period (i.e., $n$ sub-control periods):

$$u^*_{\alpha\beta}\left(k+\frac{i}{n}\right) \equiv u^*_{\alpha\beta}(k), \quad i = 0, 1, ..., n-1. \tag{2a}$$

This pattern is conceptually simple to implement. Here, the $dq$-axes voltage reference satisfies $u^*_{dq}\left(k+i/n\right) = e^{-J\omega_e T_h i/n} u^*_{dq}(k)$.

2) Constant-$u^*_{dq}$ pattern: This pattern maintains the $dq$-axes voltage reference $u^*_{dq}$ constant over a control period:

$$u^*_{dq}\left(k+\frac{i}{n}\right) \equiv u^*_{dq}(k), \quad i = 0, 1, ..., n-1. \tag{2b}$$

This pattern can achieve a better spectrum for the PWM waveforms compared to the constant-$u^*_{\alpha\beta}$ pattern. If $T_h = 0.5T_{sw}$, this pattern actually implements the asymmetrical PWM strategy. Here, the $\alpha\beta$-axes voltage reference satisfies $u^*_{\alpha\beta}\left(k+i/n\right) = e^{J\omega_e T_h i/n} u^*_{\alpha\beta}(k)$.

3) Dual-$u^*_{dq}$ pattern: Designed specifically to address the FSCD, this pattern allows for two distinct $dq$-axes voltage references, $u^*_{dq1}$ and $u^*_{dq2}$, within a control period:

$$u^*_{dq}\left(k+\frac{i}{n}\right) = \begin{cases} u^*_{dq1}(k), & 0 \le i < n-m \\ u^*_{dq2}(k), & n-m \le i < n \end{cases} \tag{2c}$$

The constant-$u^*_{dq}$ pattern is a specific case of the dual-$u^*_{dq}$ pattern when $u^*_{dq1} = u^*_{dq2}$ or $m = n$. Both patterns produce identical PWM waveforms at steady states; however, the dual-$u^*_{dq}$ pattern leverages additional flexibility to enhance transient performance. Fig. 2 illustrates the three voltage patterns.

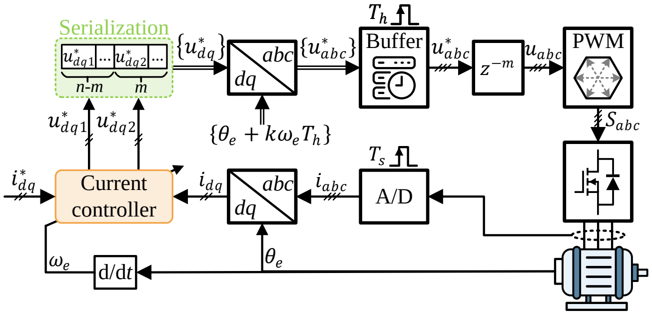


Fig. 3. Block diagram of the current control system. {} represents an array. In the constant-$u^*_{dq}$ and dual-$u^*_{dq}$ patterns, $\{\theta_e + k\omega_e T_h\}$ represents angle sequence ($k = m, m+1, ..., m+n-1$) for coordinate transformation. In the constant-$u^*_{\alpha\beta}$ pattern, the serialization part is omitted, and only $u^*_{dq}$ is output from the current controller and converted to $u_{abc}$ with angle $\theta_e + m\omega_e T_h$.

Fig. 3 shows the block diagram of the current control system, primarily designed for the dual-$u^*_{dq}$ pattern but adaptable to the other two patterns with minor adjustments. The serialization block organizes the voltage references into an $n$-element array $\{u^*_{dq}\}$ for the subsequent $n$ sub-periods: for the constant-$u^*_{dq}$ pattern, it generates an array where the first $n-m$ elements are $u^*_{dq1}$ and the last $m$ elements are $u^*_{dq2}$; for the other two patterns, it generates an array where all elements are $u^*_{dq}$. Then, for the constant-$u^*_{dq}$ and dual-$u^*_{dq}$ patterns, the $k$-th element in $\{u^*_{dq}\}$ is transformed to the abc-frame using the angle $\theta_e + (m+k)\omega_e T_h$, while the transformation angle remains $\theta_e + m\omega_e T_h$ for all elements under the constant-$u^*_{\alpha\beta}$ pattern. The buffer block sequentially sends the unpacked $u^*_{abc}$ for modulation every $T_h$, while the delay $z^{-m}$ represents the computation delay.

### C. Discrete-time Modeling of PMSM Drives with FSCD

Considering the current equation of a PMSM in real vector form:

$$\frac{\mathrm{d}}{\mathrm{d}t} i_{dq} = L^{-1}_{dq} A_0 L_{dq} i_{dq} + L^{-1}_{dq}(u_{dq} - e_{dq}). \tag{3}$$

where $L_{dq} = \mathrm{diag}([L_d, L_q])$ and $A_0 = -(R_s L^{-1}_{dq} + \omega_e J)$. If $L_d = L_q$, this model represents a surface PMSM. If $e_{dq} = 0$, the model of a SynRM is obtained.

Assuming the electrical frequency $\omega_e$ and the back-EMF $e_{dq}$ remain constant within a sampling period due to the typically slower mechanical dynamics, and considering the ZOH assumption for the $\alpha\beta$-frame voltage, $u_{dq}$ satisfies:

$$u_{dq}\left((k+\tfrac{i}{n})T_s+t\right) = e^{-J\omega_e t}u_{dq}\left((k+\tfrac{i}{n})T_s\right),\ 0 \le t < T_h. \tag{4}$$

Substituting (4) into (3) and integrating from $kT_s$ to $(k+1)T_s$ yields:

$$\begin{aligned} i_{dq}(k+1) &= L_{dq}^{-1}GL_{dq}i_{dq}(k) \\ &+ L_{dq}^{-1}\sum_{i=0}^{n-1}G_1^{n-1-i}H_1u_{dq}\left(k+\frac{i}{n}\right)+d(k), \end{aligned} \tag{5}$$

where the matrix coefficients are defined as $G = e^{A_0T_s}$, $G_1 = e^{A_0T_h}$, and $H_1 = \int_0^{T_h} e^{A_0\tau}e^{-J\omega_e(T_h-\tau)}\mathrm{d}\tau$. The term $d(k)$ accounts for the effects of back-EMF and other unmodeled disturbances, such as inverter nonlinearity.

In (5), the instantaneous $dq$-axes voltage $u_{dq}$ at each $T_h$ is used. To facilitate the design of the digital current controller, this expression is rewritten in terms of the voltage reference $u_{dq}^*$. Considering the computation delay in (1) and the voltage patterns in (2c), (5) becomes:

$$\begin{aligned} i_{dq}(k+1) &= L_{dq}^{-1}GL_{dq}i_{dq}(k) \\ &+ L_{dq}^{-1}(\Phi_1u_{dq1}^*(k)+\Phi_2u_{dq2}^*(k-1))+d(k), \end{aligned} \tag{6}$$

where $u_{dq1}^* = u_{dq2}^* = u_{dq}^*$ shall be used for the constant-$u_{\alpha\beta}^*$ and constant-$u_{dq}^*$ patterns. $\Phi_1$ and $\Phi_2$ are given by:

$$\Phi_1 = \sum_{i=m}^{n-1}G_1^{n-1-i}H_1T_i^{-m}, \quad \Phi_2 = \sum_{i=0}^{m-1}G_1^{n-1-i}H_1T_i^{-m+n}, \tag{7}$$

where $T_i = e^{-J\omega_eT_hi/n}$ for the constant-$u_{\alpha\beta}^*$ pattern, or $T_i = I$ for the constant-$u_{dq}^*$ and dual-$u_{dq}^*$ patterns. While the expressions for $\Phi_1$ and $\Phi_2$ in (7) are not immediately intuitive, simpler approximations are provided in the Appendix.

Taking the z-transform of (6) yields:

$$\begin{aligned} i_{dq}(z) &= L_{dq}^{-1}(zI-G)^{-1}\cdot \\ &\left(\Phi_1u_{dq1}^*(z)+z^{-1}\Phi_2u_{dq2}^*(z)+L_{dq}d(z)\right), \end{aligned} \tag{8}$$

where $z$ is the z-transform operator. For the constant-$u_{\alpha\beta}^*$ and constant-$u_{dq}^*$ patterns, where $u_{dq1}^* = u_{dq2}^* = u_{dq}^*$, the transfer matrix from $u_{dq}^*(z)$ to $i_{dq}(z)$, denoted as $P(z)$, is:

$$P(z) = L_{dq}^{-1}z^{-1}(zI-G)^{-1}(z\Phi_1+\Phi_2). \tag{9}$$

### *D. Analysis of the Discrete-time Plant Zeros*

For non-salient machines with $L_d = L_q$, complex vector tools can be used for analysis [26]. In a symmetrical system, vector signals and matrix parameters can be converted to complex form using the mapping relations shown in the following two equations, respectively:

$$[a,b]^T \leftrightarrow a+bj \tag{10a}$$

$$aI+bJ \leftrightarrow a+bj \tag{10b}$$

where $a$ and $b$ are arbitrary real numbers.

The complex vector representation simplifies the analysis for non-salient machines, offering intuitive insight into the system's dynamic behavior. The transfer matrix $P(z)$ in (9) then reduces to a complex transfer function. For $0 < m < n$, $P(z)$ exhibits a complex zero at $z = -\Phi_1^{-1}\Phi_2$, which approximates to $-\frac{n-m}{m}e^{-Jn\omega_eT_h/2}$ under the constant-$u_{dq}^*$ pattern, and $-\frac{n-m}{m}e^{-Jn\omega_eT_h}$ under the constant-$u_{\alpha\beta}^*$ pattern (considering $T_h$ is small enough).

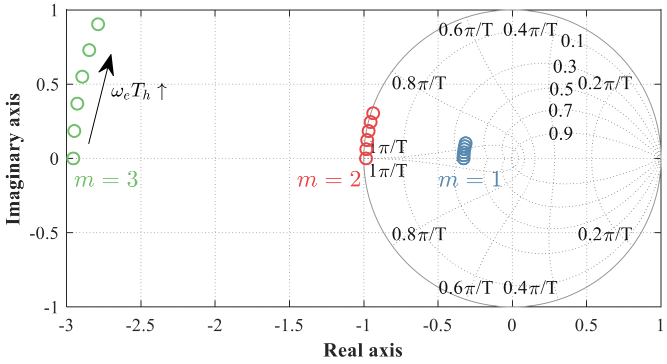


Fig. 4. Zero of P(z) with $n = 4$ and $m = 1, 2$ or 3 when $\omega_eT_h$ increases from 0 to $0.05\pi$ rad in steps of $0.01\pi$ rad under the constant-$u_{dq}^*$ pattern. Motor parameters listed in Table I are used, similarly hereinafter.

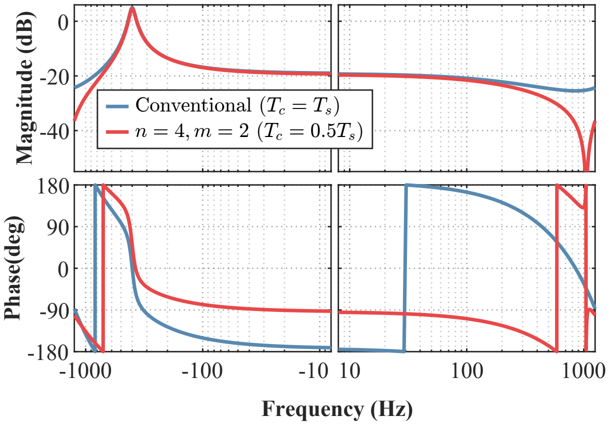


Fig. 5. Comparison of the frequency responses between $P(z)$ with $(n, m) = (4, 2)$ and the conventional model (i.e., $m = n = 1$) under the same sampling frequency. Conditions: $n = 4$, $T_h = 100$ $\mu$s, $\omega_e = 800\pi$ rad/s.

Fig. 4 shows the trajectory of the zero with $n = 4$ and various $m$ under constant-$u_{dq}^*$ pattern. This complex zero signifies coupling between $dq$-axes currents, raising a primary challenge in current control under FSCD. As the plant zeros are invariant under feedback control, this coupling persists, and pole-zero cancellation at this location may introduce unstable or oscillatory modes into the system due to parameter mismatch. Salient machines face similar issues.

Fig. 5 contrasts the frequency response of $P(z)$ with FSCD ($n = 4$, $m = 2$) against the conventional model ($m = n = 1$) under the same sampling frequency. The FSCD-induced zero markedly alters the frequency response. The phase responses differ due to the distinct inherent delays associated with each case. Furthermore, the magnitude responses deviate in the high-frequency region, particularly near the frequency $f_s/2 - f_e$ (as the zero of the $m = 2$ case in Fig. 4 approaches the unit circle, indicating a characteristic notch). Consequently, conventional current controllers would be inadequate for systems with FSCD, especially at high fundamental frequencies.

## III. PROPOSED DIGITAL CURRENT CONTROL

### A. 1-DOF Design

To simplify the analysis, the proposed digital current control is first introduced in its one-degree-of-freedom (1-DOF) version. The control law for three voltage patterns is given by:

$$u_{dq1}^*(z) = \underbrace{\left(((1-x)z^{-1}+x)\Phi_1^* + \Phi_2^* z^{-1}\right)}_{Y_1(z)} \cdot v_0(z), \tag{11a}$$

$$u_{dq2}^*(z) = \underbrace{\left(\Phi_1^* + \Phi_2^*((1-y)z^{-1}+y)\right)}_{Y_2(z)} \cdot v_0(z), \tag{11b}$$

$$v_0(z) = \frac{K}{\beta}\frac{zI-G}{z-1}L_{dq}\varepsilon_i(z), \tag{11c}$$

where $\varepsilon_i = i_{dq}^* - i_{dq}$ is the current tracking error, $K$ is the controller gain, $\beta$ is a normalization coefficient, and $x$ and $y$ are scalar parameters. $\Phi_1^*$ and $\Phi_2^*$ are the adjoint matrices of $\Phi_1$ and $\Phi_2$, respectively.

The following properties of $2\times 2$ adjoint matrices[1] are used to achieve exact decoupling of the $dq$-axes current response:

$$\Phi_1^*\Phi_1 = |\Phi_1|^2 I, \quad \Phi_2^*\Phi_2 = |\Phi_2|^2 I, \tag{12a}$$

$$\Phi_1^*\Phi_2 + \Phi_2^*\Phi_1 = 2\mathrm{tr}(\Phi_1\Phi_2)I, \tag{12b}$$

where $\mathrm{tr}(\cdot)$ denotes the trace of a matrix. Note that all matrices on the right-hand side of (12) are scalar matrices.

Based on (8), (11), and (12), the open-loop transfer matrix from $\varepsilon_i(z)$ to $i_{dq}(z)$, denoted as $L(z)$, is derived as:

$$\begin{aligned} L(z) = \big(&z^2 x|\Phi_1|^2 + z\left((1-x)|\Phi_1|^2 + y|\Phi_2|^2 + 2\mathrm{tr}(\Phi_1\Phi_2)\right) \\ &+(1-y)|\Phi_2|^2\big)\frac{K}{\beta}\frac{1}{z^2(z-1)}I. \end{aligned} \tag{13}$$

It is evident that $L(z)$ is diagonal, ensuring that the command-tracking response $G_{yr}(z) = [I+L(z)]^{-1}L(z)$ is also diagonal. Consequently, the coupling issues caused by the plant zeros are resolved without relying on pole-zero cancellation, achieving decoupled $dq$-axes responses.

The coefficient $\beta$ is determined by evaluating the following limit of $L(z)$:

$$\lim_{z\to 1}(z-1)L(z) = \frac{K}{\beta}(|\Phi_1|^2 + |\Phi_2|^2 + 2\mathrm{tr}(\Phi_1\Phi_2))I.$$

Thus, $\beta$ is selected as:

$$\beta = |\Phi_1|^2 + |\Phi_2|^2 + 2\mathrm{tr}(\Phi_1\Phi_2), \tag{14}$$

ensuring that $K$ solely adjusts the magnitude of $L(z)$ at lower frequencies.

**Remark 1:** $Y_1(z)$ and $Y_2(z)$ share the same DC gain, i.e.,

$$\lim_{z\to 1} Y_1(z) = \lim_{z\to 1} Y_2(z) = \Phi_1^* + \Phi_2^*, \tag{15}$$

ensuring that $u_{dq1}^*$ and $u_{dq2}^*$ are identical at steady states. This eliminates any imbalance between the two outputs, which is crucial for maximizing the modulation index in the proposed scheme that divides the control period into multiple sub-periods. Additionally, $u_{dq1}^*$ and $u_{dq2}^*$ are derived from a shared integrator in (11c), further preventing discrepancies between the two voltages due to numerical computation errors.

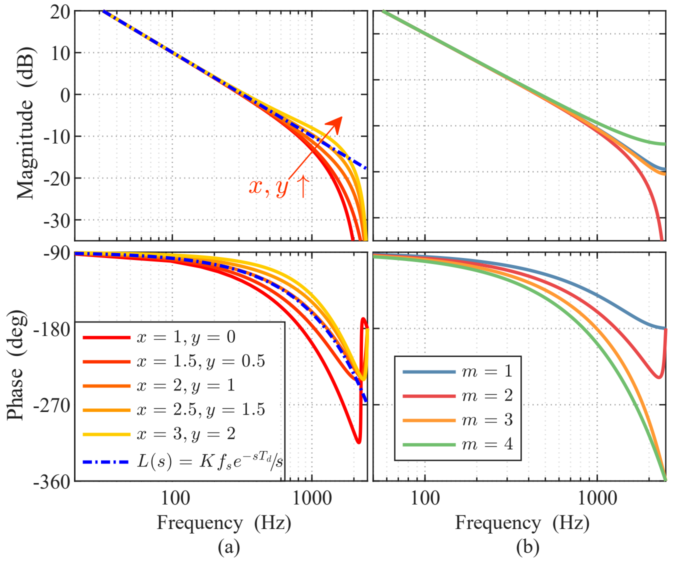


Fig. 6. Bode diagram of the open-loop system. (a) $m=2$ with various $(x,y)$. (b) Various $m$ with $x=1+m/(n-m)$ and $y=1$. Conditions: $n=4$, $T_s=200$ $\mu$s, $\omega_e=1000\pi$ rad/s, $K=0.4$.

**Remark 2:** To ensure balanced magnitudes of $u_{dq1}^*$ and $u_{dq2}^*$ during transient states, the feedthrough gain[2] of $Y_1(z)$ should approximately match that of $Y_2(z)$, i.e., $x\Phi_1^* \approx \Phi_1^* + y\Phi_2^*$. From (7), a rough approximation $\Phi_1 \approx \frac{n-m}{m}\Phi_2$ holds for $\omega_e T_h \ll 1$. Thus, $x$ and $y$ should satisfy:

$$x = 1 + y\cdot m/(n-m). \tag{16}$$

In this manner, $x$ is determined once $y$ is selected.

Since the open-loop system $L(z)$ has been a scalar matrix, its frequency response can be represented along a single axis. Fig. 6 shows an example with $n=4$ with $(x,y)$ satisfying (16). In Fig. 6 (a), various combinations of $(x,y)$ are compared, all exhibiting similar cutoff frequencies. As $x$ and $y$ increase, the phase margin improves. An $s$-domain transfer function $L(s) = Kf_s e^{-sT_d}/s$ with bandwidth $Kf_s$ and delay $T_d = (m+n/2)T_h$ is also shown in Fig. 6 (a). The pair $(x,y)=(2,1)$ aligns best with the phase response of $L(s)$. Fig. 6 (b) compares the frequency response for various $m$. A lower $m$, indicating a shorter computation delay, results in a higher phase margin.

**Remark 3:** The pair $(x,y)=(1,0)$ results in $Y_1(z) = Y_2(z)$, leading to $u_{dq1}^* = u_{dq2}^*$. Consequently, the controller in (11) is also applicable to the constant-$u_{\alpha\beta}^*$ and constant-$u_{dq}^*$ patterns. Theoretically the two patterns exhibit identical open-loop responses at sampling instants. For non-salient machines, the controller introduces a zero at $z = -(\Phi_1^*)^{-1}\Phi_2^*$, which is the complex conjugate of the plant zero $z = -\Phi_1^{-1}\Phi_2$. However, the term $\Phi_1^* + \Phi_2^* z^{-1}$ of the controller introduces phase lag, which becomes more pronounced when $m > n/2$.

---

[1] For a $2\times 2$ matrix $M = \begin{bmatrix} a & b \\ c & d \end{bmatrix}$, its adjoint matrix is $M^* = \begin{bmatrix} d & -b \\ -c & a \end{bmatrix}$. In a symmetrical system, the adjoint matrix is analogous to the complex conjugate, e.g., $M = aI + bJ \Rightarrow M^* = aI - bJ$.

[2] The feedthrough gain $\bar{g}$ of a transfer function/matrix $G(z)$ is defined such that $G(z) - \bar{g}$ is strictly proper.

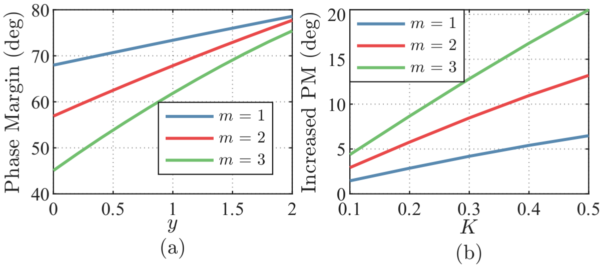


Fig. 7. (a) Phase margin of the open-loop system with $y$ varying and $K = 0.4$. (b) Increased phase margin (PM) with the dual-$u^*_{dq}$ pattern compared the other two patterns with $K$ varying. Conditions: $n = 4$, $T_s = 200\ \mu$s, $\omega_e = 1000\pi$ rad/s.

In such cases, additional loop filtering may be required to compensate for the reduced phase margin.

**Remark 4:** In (11a), the parameter $x$ sets the weight of $(1-x)z^{-1}+x$ in $Y_1(z)$; analogously, $y$ plays the same role in $Y_2(z)$ of (11b). The dual-$u^*_{dq}$ pattern leverages these degrees of freedom to shape the loop phase. Increasing $x$ or $y$ advances the phase and improves the phase margin (see Fig. 6), but overly large values amplify high-frequency noise. Fig. 7 (a) quantifies the phase-margin variation with $y$, and Fig. 7 (b) shows that the dual-$u^*_{dq}$ pattern ($y = 1$) consistently achieves a higher phase margin than the other two patterns ($y = 0$), because the dual update more effectively compensates the coupling induced by the plant zero.

In this paper, we set $y = 1$ for the dual-$u^*_{dq}$ pattern and choose $x$ from (16). This gives $Y_2(z) = \Phi_1^* + \Phi_2^*$ and, under the approximation $\Phi_1 \approx \frac{n-m}{m}\Phi_2$ for $\omega_e T_h \ll 1$, yields an analogous constant-gain form for $Y_1(z)$. The resulting open-loop response closely matches the $s$-domain model $L(s)$ over a range of $m$, facilitating quick evaluation. For constant-$u^*_{\alpha\beta}$ and constant-$u^*_{dq}$ patterns, $(x, y) = (1, 0)$ is fixed by definition.

### *B. 2-DOF Design*

The concept of active resistance (AR) is employed in the 2-DOF design to enhance disturbance rejection near the synchronous frequency and reduce current error during rapid rotor speed changes . By defining $u^*_{dq1}(z) = u'_{dq1}(z) - R_A i_{dq}(z)$ and $u^*_{dq2}(z) = u'_{dq2}(z) - R_A i_{dq}(z)$, where $R_A$ represents the AR, (8) is reformulated as:

$$\begin{aligned} i_{dq}(z) = {} & [z^2 I + (\Phi_1 R_A - G)z + \Phi_2 R_A]^{-1} \\ & \cdot [z\Phi_1 u'_{dq1}(z) + \Phi_2 u'_{dq2}(z) + d(z)]. \end{aligned} \tag{17}$$

Based on (17), the control law in (11) is modified as:

$$u^*_{dq1}(z) = Y_1(z)v_0(z) - R_A i_{dq}(z), \tag{18a}$$

$$u^*_{dq2}(z) = Y_2(z)v_0(z) - R_A i_{dq}(z), \tag{18b}$$

$$v_0(z) = \frac{K}{\beta}\frac{z^2 I + (\Phi_1 R_A - G)z + \Phi_2 R_A}{z(z-1)} L_{dq}\varepsilon_i(z). \tag{18c}$$

From (17) and (18c), the closed-loop current response is:

$$i_{dq}(z) = G_{yr}(z)i^*_{dq}(z) + S_C(z)S_A(z)P_A(z)d(z), \tag{19}$$

where $S_A(z) = (I + P(z)R_A)^{-1}$ and $S_C(z) = (I + L(z))^{-1}$ are the sensitivity matrices of the inner loop with AR and the outer loop with the regulator, respectively. $P_A(z) = L_{dq}^{-1}(zI - G)^{-1}L_{dq}$ is the transfer matrix from $d(z)$ to $i_{dq}(z)$ [see (8)]. The term $S_A(z)$ reflects the impact of AR on disturbance rejection in the current control system.

In this paper, the AR is defined as a constant matrix:

$$R_A = \alpha_A e^{J\eta\omega_e T_h} L_{dq}, \tag{20}$$

where $\alpha_A$ scales the AR, and $\eta$ compensates for the angle. These coefficients are discussed below. While higher-order forms of $R_A(z)$, as explored in [17], [27], can further refine control performance, they are not considered here. The formulation in (20) is derived based on the following criteria:

1) The AR should be proportional to the $dq$-axes inductance to ensure balanced gain margins [23].
2) The state-feedback path with $R_A$ should avoid introducing a rotational factor to maintain balanced phase margins.

Criterion 1) is straightforward, as the inner loop with AR essentially acts as proportional control. The formulation in (20) ensures consistent open-loop magnitude responses for the $d$- and $q$-axes, which is particularly important for machines with high saliency. Alternatively, replacing $L_{dq}$ in (20) with a scalar gain, such as a fraction of the stator resistance $R_s$, is also a common approach. The choice between these options depends on whether the disturbance of interest should be attenuated relatively or absolutely.

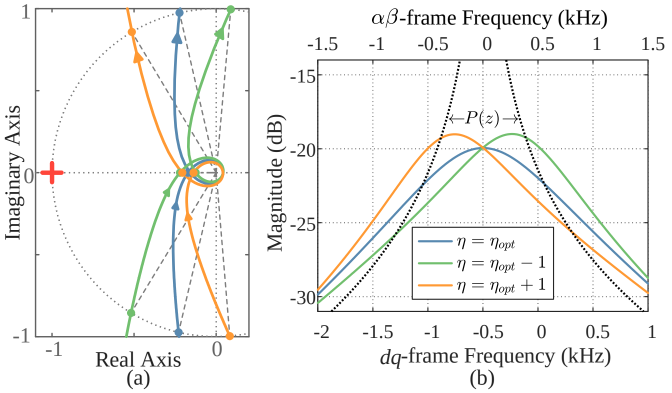
Criterion 2) emphasizes that AR should emulate the effect of real resistance to enhance damping. This can be achieved in the $\alpha\beta$-frame or abc-frame when no digital delay is present. In some studies, the deviation of the output voltage angle caused by delay is implicitly compensated in the inverse Park transform, introducing an additional rotational factor to the actual AR when viewed from the $\alpha\beta$-frame. For instance, in the case of an SPMSM, the Nyquist diagram of the inner loop with AR, represented by the open-loop transfer function $L_A = P(z)R_A$, is shown in Fig. 8(a). An improper rotational factor results in an asymmetrical trace near the critical point, reducing the stability margin. Fig. 8(b) illustrates the magnitude responses of $S_A(z)P_A(z)$, with the response of $P_A(z)$ shown as a dotted line for reference. When $\eta = \eta_{opt}$, the trace of $S_A(z)P_A(z)$ exhibits a more symmetrical position and deeper attenuation compared to other cases.

To satisfy criterion 2), (20) introduces a factor $e^{J\eta\omega_e T_h}$, where $\eta$ is a real number dependent on the voltage update pattern. The optimal value of $\eta$ is determined by canceling the phase advance introduced by the rotational transform, yielding:

$$\eta_{opt} = \begin{cases} -(n + 2m - 1)/2, & \text{constant-}u^*_{dq} \\ -m, & \text{constant-}u^*_{\alpha\beta} \end{cases} \tag{21}$$

It is important to note that $\eta$ should be adjusted based on whether phase compensation of the output voltage angle has been applied in the inverse Park transformation.

Although the proposed control law is developed for a rational ratio $T_c/T_s = m/n$, it can be extended to arbitrary real fractions by directly calculating $\Phi_1$ and $\Phi_2$.



(a) (b)

Fig. 8. Impact of the rotational factor in AR. (a) Nyquist diagram of the inner current loop $L_A = P(z)R_A$. (b) Magnitude response of disturbance rejection $S_A(z)P_A(z)$.

## IV. IMPLEMENTATION ISSUES

### A. Anti-windup and Incremental Structure

Due to the limited dc-bus voltage, control saturation may occur when machine operates at high-speed range or with high bandwidth [28]. To address this issue, an anti-windup mechanism is incorporated into the proposed current controller. Without this mechanism, continuous integration of the control error after saturation can cause the output to deviate from the desired value, leading to overshoots and prolonged dynamic responses. The anti-windup mechanism also ensures smooth transitions when switching from other controllers or control modes.

The control law in (18) is modified as follows:

$$v_0'(z) = \frac{K}{\beta}\frac{z^2 I + (\Phi_1 R_A - G)z + \Phi_2 R_A}{z^2} L_{dq}\varepsilon_i(z), \qquad (22a)$$

$$u_{dq1}^*(z) = \frac{z}{z-1}\underbrace{Y_1(z)v_0'(z)}_{v_1(z)} - R_A i_{dq}(z), \qquad (22b)$$

$$u_{dq2}^*(z) = \frac{z}{z-1}\underbrace{Y_2(z)v_0'(z)}_{v_2(z)} - R_A i_{dq}(z). \qquad (22c)$$

Based on (22c), the difference equation for the integration process, is given by:

$$u_{dq2}^*(k) = u_{dq2}^*(k-1) + v_2(k) - R_A[i_{dq}(k) - i_{dq}(k-1)]. \quad (23)$$

When saturation occurs, the saturated voltage $\bar{u}_{dq2}^* \triangleq \text{sat}\{u_{dq2}^*\}$ should be used in the integration, resulting in:

$$u_{dq2}^*(k) = \bar{u}_{dq2}^*(k-1) + v_2(k) - R_A[i_{dq}(k) - i_{dq}(k-1)]. \quad (24)$$

Since $u_{dq1}^*$ and $u_{dq2}^*$ share the same integrator, it is unnecessary to perform the same operation on (22b). Instead, the difference between $u_{dq2}^*$ and $u_{dq1}^*$ is calculated by subtracting (22b) from (22c):

$$\begin{aligned} u_{dq1}^*(z) - u_{dq2}^*(z) &= \frac{z}{z-1}(Y_1(z) - Y_2(z))v_0'(z) \\ &= -((1-x)\Phi_1^* + y\Phi_2^*)v_0'(z). \end{aligned} \qquad (25)$$

Using (22a), (24), and (25), the block diagram of the proposed current controller is shown in Fig. 9. Since matrix multiplication is generally non-commutative, the arrangement of matrix parameter blocks must be preserved, except for non-salient machines. Integration is performed on $u_{dq2}^*$ rather than $u_{dq1}^*$ because $u_{dq1}^*$ may not exist when $n = m$, and this approach reduces a delay element in the implementation. For the constant-$u_{\alpha\beta}^*$ and constant-$u_{dq}^*$ patterns, where $x = 1$ and $y = 0$, the dotted path in Fig. 9 can be omitted.

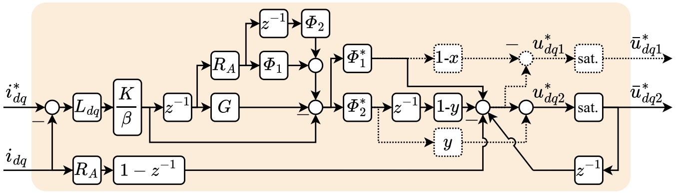


Fig. 9. Block diagram of the proposed current controller with anti-windup mechanism.

### B. Coefficient Matrix Calculation

Accurate computing $G$, $\Phi_1$, and $\Phi_2$ is critical for implementing the proposed current controller. While analytical expressions for these matrices are simple for non-salient machines, they become more complex for salient machines with unequal $L_d$ and $L_q$. This paper utilizes the simplification method from [23], approximating the matrices $G_1$ and $H_1$ as:

$$G_1 \approx \begin{bmatrix} e^{-\frac{R_s}{L_d}T_h}\cos\omega_e T_h & e^{-(\frac{R_s}{L_d}+\frac{R_s}{L_q})\frac{T_h}{2}}\sin\omega_e T_h \\ -e^{-(\frac{R_s}{L_d}+\frac{R_s}{L_q})\frac{T_h}{2}}\sin\omega_e T_h & e^{-\frac{R_s}{L_q}T_h}\cos\omega_e T_h \end{bmatrix} \qquad (26)$$

$$H_1 \approx \frac{1}{R_s}\begin{bmatrix} 1 - e^{-R_s T_h/L_d} & 0 \\ 0 & 1 - e^{-R_s T_h/L_q} \end{bmatrix} e^{-J\omega_e T_h} \qquad (27)$$

The matrix $G$ can be obtained by replacing $T_h$ with $T_s$ in $G_1$. If necessary, the exponential functions can be further simplified using their Taylor series expansions. For machines exhibiting flux saturation, the incremental inductance should be used instead of the nominal inductance to ensure accuracy.

Once $G_1$ and $H_1$ are determined, the coefficient matrices $\Phi_1$ and $\Phi_2$ are obtained from (7). In the experimental validation, (26) and (27) are used for computational efficiency. Although the per-sample cost of forming $\Phi_1$ and $\Phi_2$ grows with the number of sub-periods $n$, the proposed voltage update scheme substantially reduces the overall burden for $n \geq 2$ by consolidating multiple switching periods into one sampling period. Tasks such as A/D conversion, controller state updates, and coordinate transformations are executed once per sampling period rather than in every sub-period. As a result, the total computation time grows sublinearly with $n$ and remains well below $n$ times that of the $n = 1$ case.

By minimizing redundant operations in the current control loop, the proposed approach effectively mitigates the computational demands associated with high switching frequencies while maintaining minimal computation delay. Additionally, the dual-update strategy in the current controller inherently compensates for the adverse effects introduced by fractional-step computation delay, ensuring robust performance across a wide range of operating conditions.

TABLE I
PARAMETERS OF THE TESTED PMSM DRIVE

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| Pole pairs | 5 | Rated speed | 1500rpm |
| Stator resistance | 0.57Ω | Rated current | 6.6A |
| $d$-axis inductance | 3.75mH | DC-bus voltage | 300V |
| $q$-axis inductance | 3.75mH | Encoder lines | 2500 |

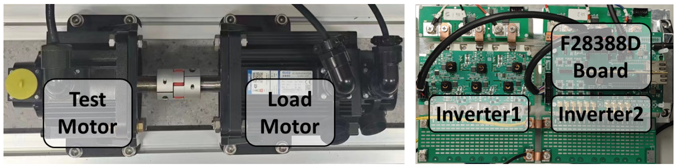
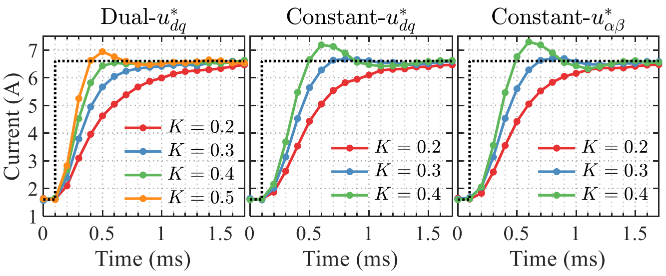


Fig. 10. Experimental setup.



(a) (b) (c)

Fig. 11. Current responses with various K when n = 2 and m = 1. (a) Dual-$u_{dq}^*$ pattern. (b) Constant-$u_{dq}^*$ pattern. (c) Constant-$u_{\alpha\beta}^*$ pattern.

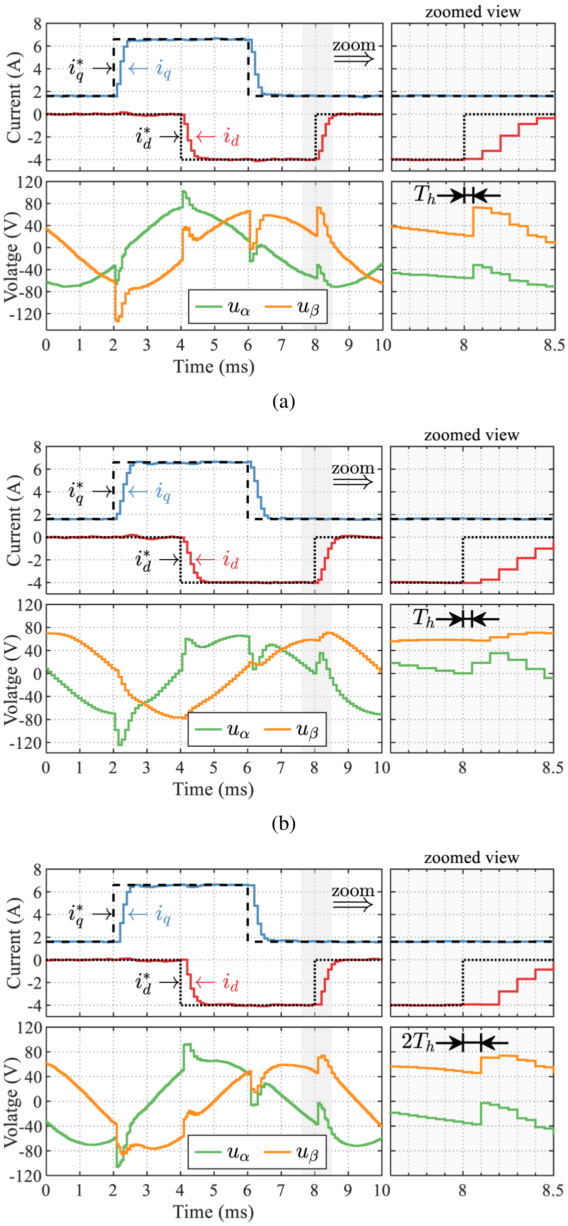
## V. VALIDATION

The experimental setup is shown in Fig. 10. Experiments are conducted on the tested motor with parameters listed in Table I. The motor operates in current-control mode, and the algorithm is executed on a microcontroller unit TMS320F28388D with a 200 MHz clock. Another PMSM serves as the load motor and operates in speed-control mode. Unless otherwise specified, the shaft is maintained at the rated speed of 1500 rpm in the following experiments, resulting in a fundamental frequency of $f_e = 125$ Hz for the test motor. $T_h = 0.5T_{sw}$ is configured for all subsequent experiments.

### A. Transient-state Response

First, experiments are conducted under a standard 10 kHz switching frequency. Fig. 11 depicts the current responses with various $K$ for the three voltage patterns. The configuration is $(n, m) = (2, 1)$ with $T_h = 50$ $\mu$s. It is observed that both the constant-$u_{dq}^*$ pattern and the constant-$u_{\alpha\beta}^*$ pattern exhibit similar response characteristics, as they theoretically employ identical command tracking mechanisms. Nevertheless, these two patterns show larger overshoots compared to the dual-$u_{dq}^*$ pattern when $K \geq 0.3$. This disparity is attributed to the phase lag introduced by the controller for the two patterns to decouple the $dq$-axes currents.

Detailed evaluations of the dual-$u_{dq}^*$ pattern and the constant-$u_{\alpha\beta}^*$ pattern are shown in Fig. 12(a) and Fig. 12(b), respectively. The sampling period remains $T_s = 100$ $\mu$s with $(n, m) = (2, 1)$. The sampled $dq$-axes currents are visualized using stairstep lines with time interval $T_s$, while the applied $\alpha\beta$-axes voltages are plotted with time interval $T_h$. Specifically, the $q$-axis current steps from 1.6A (24% of rated current) to 6.6A (100% of rated current) and back, and the $d$-axis current transitions from 0A to -4A and back. Notably, the decoupling between the axes currents during transient states is evident. From the zoomed view on the right side of Fig. 12(a), following the $i_q$ steps, the change in $u_{\alpha\beta}$ is delayed by $T_h$ due to $m = 1$. The magnitudes of $u_{\alpha\beta}$ at each $2T_h$ are nearly balanced and distinguishable. Furthermore, prior to the $i_d$ transition, $u_\alpha$ and $u_\beta$ exhibit smooth variations, indicating the characteristics of an asymmetrical PWM pattern. In Fig. 12(b), the zoomed view clearly illustrates the application of a symmetrical PWM strategy.



(a) (b) (c)

Fig. 12. Current step responses for (a) Dual-$u_{dq}^*$ pattern with $n = 2$ and $m = 1$. (b) Constant-$u_{\alpha\beta}^*$ pattern with $n = 2$ and $m = 1$. (c) Dual-$u_{dq}^*$ pattern with $n = 2$ and $m = 2$. Controller parameters: K = 0.4, $\alpha_A$ =0.1.

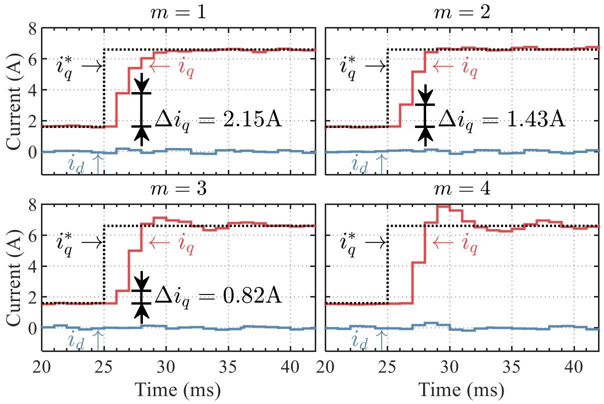


Fig. 13. Current step response when n = 4 and m = 1,2,3,4 with 2 kHz switching frequency and 1 kHz sampling frequency. The dual-$u_{dq}^*$ pattern is applied. (Controller parameters: K = 0.5, $\alpha_A$ =0.1)

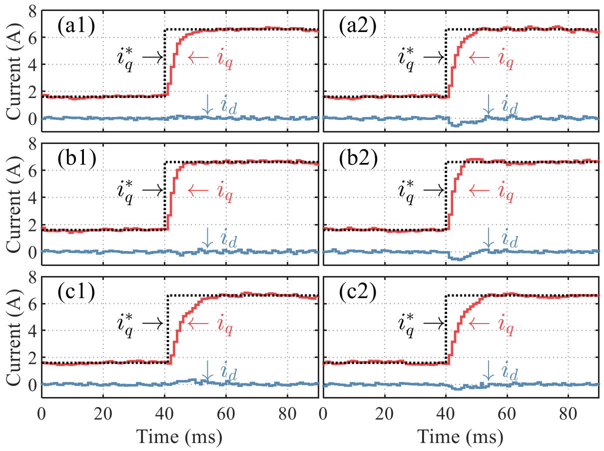


Fig. 14. Comparison of the current response between the proposed method (left column) and the method in [25] (right column) with parameter error: (a1)(a2) $L_d = L_d, L_q = L_q$, (b1)(b2) $L_d = 1.3L_d, L_q = 1.3L_q$ and (c1)(c2) $L_d = 0.7L_d, L_q = 0.7L_q$. Conditions: n = 2, m = 1, $f_s = f_{sw} = 1$ kHz, K = 0.3, $\alpha_A$ =0.1. Both methods are tuned for similar bandwidth.

Fig. 12(c) presents the current step response when $(n, m) = (2, 2)$. The difference from Fig. 12(a) is that the change in $u_{\alpha\beta}$ is delayed by $2T_h$ relative to the $i_q$ step, and the current response lags the reference by two sample cycles. The asymmetrical PWM pattern is also maintained at steady states.

Current step experiments are also performed at lower switching and sampling frequencies to evaluate control performance under a low ratio of sampling to fundamental frequency. Fig. 13 demonstrates the current response with $n = 4$ and various $m$. The switching frequency is 2 kHz, and the sampling frequency is 1 kHz. For $m < n$, the current increment $\Delta i_q$ at the first sample after the command step is approximately $n - m$, and the current response for $m = n = 4$ lags the command step by two sample cycles.

In real PMSMs, the actual inductance depends on current magnitude due to magnetic saturation. Consequently, evaluating control performance under parameter uncertainties is essential. Fig. 14 presents a comparative analysis of current responses under parameter variations. The left column shows the performance of the proposed method using the dual-$u_{dq}^*$ pattern, while the right column shows the method from [25]. The evaluation includes accurate parameters and scenarios with ±30% inductance errors. The proposed method demonstrates superior current dynamics across all test conditions. Notably, since [25] retains coupling zeros in the closed-loop system, observable variations in $d$-axis current appear during $i_q$ step changes. To quantitatively assess performance, the integral of absolute error (IAE) is employed, defined as

$$\text{IAE} = T_s \sum_{k=1}^{20} |i_x(t_0 + kT_s) - i_x^*(t_0 + kT_s)|, \quad x = d, q, \tag{28}$$

which is used to analyze the system response following current reference changes at $t_0$. The comparative results are presented in Table II. As the experimental evaluation only modifies the $q$-axis current command, the $d$-axis IAE serves as an effective indicator of decoupling performance. While both methods are tuned to achieve comparable bandwidths, resulting in nearly identical $q$-axis IAE values, the proposed method exhibits significantly reduced $d$-axis IAE, attributable to its enhanced decoupling capability.

TABLE II
IAE COMPARISON OF CURRENT CONTROL PERFORMANCE

| Approach | $\widehat{L}_d = L_d$, $\widehat{L}_q = L_q$ | | $\widehat{L}_d = 1.3L_d$, $\widehat{L}_q = 1.3L_q$ | | $\widehat{L}_d = 0.7L_d$, $\widehat{L}_q = 0.7L_q$ | |
|---|---|---|---|---|---|---|
| | $d$-axis | $q$-axis | $d$-axis | $q$-axis | $d$-axis | $q$-axis |
| Proposed | 1.76 | 33.67 | 1.72 | 27.3 | 3.72 | 45.18 |
| [25] | 6.94 | 36.23 | 7.21 | 28.05 | 4.3 | 45.95 |

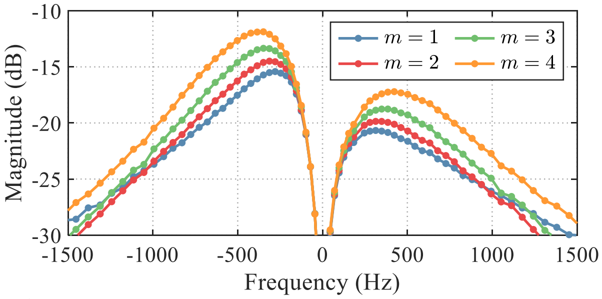


Fig. 15. Disturbance rejection test by virtually injecting voltage disturbance into $u_{q1}^*$ and $u_{q2}^*$ with $n = 4$ and various $m$. Conditions: 10 kHz switching frequency, $T_h = 50$ $\mu$s, $\alpha_A = 0.2$, $K = 0.3$.

Disturbance rejection performance is validated by virtually injecting voltage disturbance into the $q$-axis voltage references $u_{q1}^*$ and $u_{q2}^*$. Fig. 15(a) shows the current responses with various $\alpha_A$ when a $\Delta u_q = 20$V voltage disturbance is injected. A higher $\alpha_A$ leads to a faster settling time. Fig. 15(b) compares the current responses with the same controller parameters under various $m$. A lower $m$, corresponding to a lower computation delay, results in a lower peak value of current deviation.

## B. Steady-state Performance

The THD of the measured phase current under various combinations of $(n, m)$ and fixed switching frequencies of 10 kHz and 25 kHz are listed in Table III. For a fixed switching frequency, the THD of the steady-state phase current is minimally affected by the configuration of $(n, m)$. This indicates that the proposed method can be used to reduce

TABLE III
CURRENT THD UNDER VARIOUS COMBINATIONS OF $(n, m)$

| | $(n, m)$ | (2,1) | (4,2) | (5,2) | (10,2) |
|---|---|---|---|---|---|
| $f_{sw} = 25000$Hz | $f_s$ (Hz) | 25000 | 12500 | 10000 | 5000 |
| | THD (%) | 2.03 | 1.98 | 2.0 | 1.99 |
| $f_{sw} = 10000$Hz | $f_s$ (Hz) | 10000 | 5000 | 4000 | 2000 |
| | THD (%) | 4.16 | 4.14 | 4.13 | 4.11 |

TABLE IV
ALGORITHM EXECUTION TIME WITH THE DUAL-$u_{dq}^*$ PATTERN.

| $n$ | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| Time ($\mu$s) | 6.95 | 7.52 | 8.05 | 8.51 | 9.07 | 9.63 | 10.2 | 10.7 | 11.3 | 11.8 |

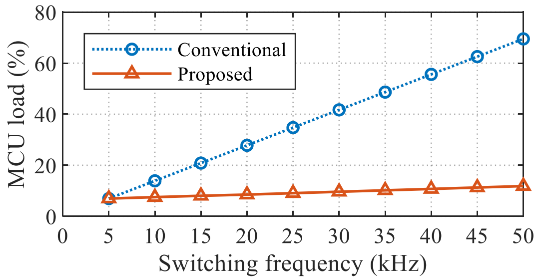


Fig. 16. Computational load of the current control algorithm under various switching frequencies when fixing the sampling frequency of the proposed method to 10 kHz.

the computational burden by employing a lower sampling frequency without distorting the phase currents.

### C. Execution Time

The average time to execute the current control algorithm for various $n$ with the dual-$u_{dq}^*$ pattern is recorded and listed in Table IV. The value of $m$ does not affect the execution time in our code. For a fixed sampling frequency of 10 kHz and asymmetrical PWM strategy, the computational burden of the current loop with the proposed method under various switching frequencies is shown in Fig. 16. The computational burden of conventional methods that sample current once and update PWM once is also compared, assuming they also take 6.95 $\mu$s per execution (1390 cycles under 200 MHz clock). This indicates that the proposed method can significantly reduce the computational burden as the switching frequency increases, which is valuable in applications where response speed is not the primary concern and a moderate sampling frequency is sufficient.

## VI. CONCLUSION

This paper develops a digital current controller tailored for PMSM drives with fractional-step computation delay, addressing the unique challenges posed by the transmission zero in the discrete-time model. The proposed controller achieves decoupled $dq$-axes current dynamics through complementary zero assignment and enhances disturbance rejection using active resistance. The controller enables operation at lower sampling frequencies with asymmetrical PWM, significantly reducing computational burden while maintaining high control performance with reduced digital delay. Experimental results confirm the effectiveness in achieving precise current regulation, robust disturbance rejection, and optimized steady-state performance, even under low sampling-to-fundamental frequency ratios. This makes the proposed approach particularly valuable for high-switching-frequency applications, such as electric vehicle traction inverters equipped with wide-bandgap semiconductors. Future work could explore integrating the proposed method with advanced sampling techniques to further enhance noise immunity and control robustness.

## APPENDIX

Letting $R_s \to 0$, for dual-$u_{dq}^*$ and constant-$u_{dq}^*$ patterns, (7) is simplified as:

$$\begin{cases} \Phi_1 \approx \sum_{i=m}^{n-1} e^{-J(n-i)\omega_e T_h} \approx (n-m)T_h e^{-J\frac{(n-m+1)\omega_e T_h}{2}} \\ \Phi_2 \approx \sum_{i=0}^{m-1} e^{-J(n-i)\omega_e T_h} \approx mT_h e^{-J\frac{(2n-m+1)\omega_e T_h}{2}} \end{cases} \tag{29}$$

and for constant-$u_{\alpha\beta}^*$ pattern, (7) is simplified as:

$$\begin{cases} \Phi_1 \approx (n-m)T_h e^{-J(n-m)\omega_e T_h} \\ \Phi_2 \approx mT_h e^{-J(2n-m)\omega_e T_h} \end{cases} \tag{30}$$

In both cases, the first factor (e.g., $n - m$ for $\Phi_1$ and $m$ for $\Phi_2$) represents the effective duration of the applied voltage commands within the sampling period, scaled by the sub-control period $T_h$. The last term captures the phase shift introduced by the discrete-time integration, depending on the voltage update patterns and the computation delay.

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