# Pulse Magnitude Modulation and Token Rotation-based Voltage Balancing Method of Multilevel Inverter for Wireless Power Transfer

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***Abstract*—The multilevel inverter has attracted more and more attention in high-power wireless power transfer (WPT) systems, but its switching loss and capacitor voltage balancing are worrying issues. To solve these problems, this paper proposes and implements a sigma-delta (Σ-Δ) pulse magnitude modulation (PMM) of a flying-capacitor multilevel inverter (FCMLI) for WPT systems. It can achieve wide-range output voltage regulation and zero voltage switching simultaneously. Besides, a token rotation-based flying-capacitor voltage balancing method of the FCMLI for WPT is proposed. It can balance the capacitor voltages of the FCMLI with arbitrary voltage levels while maintaining little ripples and resisting the step dynamic. The corresponding parameter selection of the flying capacitors is discussed. Theoretical analysis, computer simulation, and an 850 W seven-level flying capacitor inverter-based hardware experimentation are given to verify the effectiveness of the proposed Σ-Δ PMM FCMLI-based WPT system.**

***Index Terms*—Wireless power transfer; Pulse magnitude modulation; Multilevel inverter; Zero voltage switching; Capacitor voltage balance**

## I. Introduction

Wireless power transfer (WPT) technology can be traced back over one century to the work of Nikola Tesla and has been applied to a wide range of fields with power levels ranging from milliwatts to megawatts [1]-[3], helping to charge micro-robots, electric toothbrushes, electric vehicles [4], and high-speed train [5], due to electrical isolation, the safety, convenience, and better user experience. Identified as an epoch-making technology, the WPT has been attracting a growing number of academic researchers and engineers to participate in the great explorations.

In recent years, WPT systems based on multilevel inverters have attracted more and more attention due to the advantage of realizing a large operating range [6]-[7], breaking voltage limitations [8]-[9], [11]-[12]. On the one hand, a multilevel inverter-based WPT system has been studied for low-voltage high-power EV charging whose loading conditions can vary up to 450% [6]-[7]. On the other hand, a medium-voltage (1.5 kV-50 kV) DC distribution network is often equipped in high-power applications [10] to decrease the current in the DC bus, such as the submarine data center and fast charging of EVs. Multilevel inverters-based WPT systems can be connected to the medium-voltage DC-power system to reduce the voltage stress for each semiconductor component [11]-[12]. Moreover, multilevel inverters have been applied for decoupled multichannel WPT systems to eliminate the transformers and simplify the system configuration [13]. It is noticed that the modulation method and capacitor voltage balancing of multilevel inverter-based WPT systems are two key problems to be further investigated.

Recently, many significant modulation schemes of two-level inverter-based WPT systems have been fully investigated, including pulse-width modulation (PWM), on-off keying modulation, hybrid modulation, pulse density modulation (PDM), pulse frequency modulation (PFM), and step density modulation (SDM). As a kind of PWM with a controllable angle, phase-shift control (PSC) [14]-[15] is generally utilized in the converters of the WPT system, but it suffers from hard switching. On-off modulation uses the low-frequency on-off duty ratios to control the converter [16], but causes large output ripples. Hybrid modulation combining the PFM and on-off modulation suffers from the same issues [17]. By comparison, PDM [18]-[20] and PFM are more suitable for WPT systems due to breaking through the above limitations. A low-subharmonic, full-range, and rapid PDM strategy is proposed in [20] for the full-bridge converters-based WPT system. The PFM for WPT systems was proposed in [21]-[23], and it regulates the output power by using high-order harmonics of the square wave at a specific frequency. The studies of the Σ-Δ PFM are also presented in [22] to decrease the output ripple, but the realization is a little complicated. Recently, SDM, which uses the density of steps to regulate the output power, was proposed in [24], combining both the advantages of PDM and PFM.

However, the above methods are unsuitable for the multilevel inverter-based WPT system. The study in [13] proposes the PWM T-type multilevel inverter-based multichannel WPT system, and switching signals are exchanged to balance neutral voltages, but there is a hard switching problem. The ZVS modulation method of the modular multilevel converter (MMC)-based WPT system is proposed [7], but the output voltage of the MMC-based WPT system is not continuous, and the capacitor voltage balancing method of multilevel inverter with arbitrary voltage levels remains unclear. It is unsuitable for other multilevel inverters such as T-type or flying-capacitor multilevel inverters [25].

This work was partially supported by a grant from the Hong Kong Research Grants Council, Hong Kong Special Administrative Region, China, under Project No. T23-701/20-R, and partially supported by a grant from The Hong Kong Polytechnic University, under Project No. P0048560. (*Corresponding author: K.T. Chau.*)

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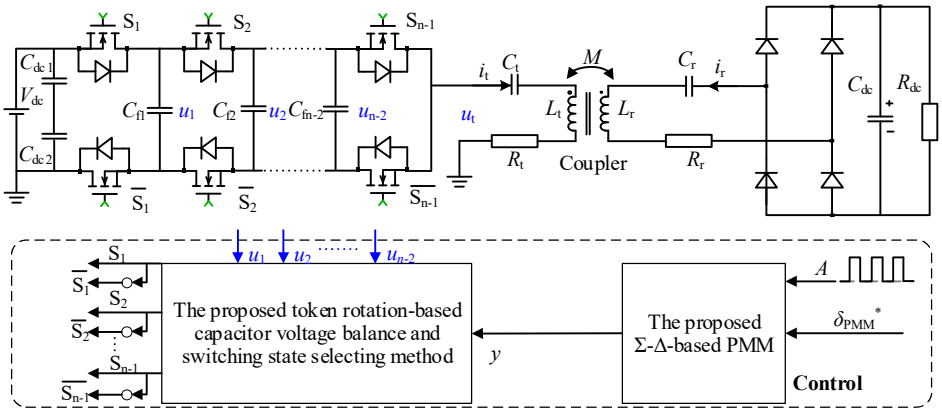


Fig.1. PMM flying-capacitor multilevel inverter-based WPT system.

Our previous work proposes the segmented vector pulse frequency modulation method of the flying-capacitor three-level inverters for the WPT system [26], but the total harmonic distortion (THD) of the transmit current is high especially when under the light load, which could lead to EMI noise that will influence the system stability. Besides, due to the capacitor voltage balancing, the precious method can only be used for the three-level inverter-based WPT system. Moreover, a ZVS modulation method with low THD and DC-side voltage ripple for the flying-capacitor multilevel inverters (FCMLI) needs to be further investigated.

The voltage balancing of the FCMLI-based WPT is a key issue to be solved. Many flying capacitor voltage balance methods have been proposed for 50Hz/60Hz FCMLIs [27]-[30], which are based on the low-frequency phase currents and voltage deviation of flying capacitors [31]-[32]. Different from the 50Hz/60Hz FCMLI, the capacitor voltage balancing method of the FCMLI for the high-frequency WPT system has more challenges. First of all, the algorithm needs to be completed in a more high-speed control cycle, which is half the resonant cycle of the WPT system. Secondly, the high-frequency transmitter current in the WPT system will not be measured. Besides, the capacitor voltage balancing method of the FCMLI needs to match the ZVS modulation method. Moreover, the voltage balancing approach needs to be easy to implement and easily portable to the FCMLIs with arbitrary voltage levels.

To realize the soft-switching modulation, balance capacitor voltages of the FCMLI in a high-speed control cycle, and reduce the DC-side voltage ripple and THD of the transmitter current of the FCMLIs-based WPT systems, this paper proposed an Σ-Δ pulse magnitude modulation (PMM) method of the multilevel inverter and a token rotation-based capacitor voltage balancing method, the main contribution of this article is listed as follows.

1) The Σ-Δ PMM of the FCMLI for WPT systems is proposed to realize the wide-range continuous DC-side output voltage regulation and ZVS simultaneously, reduce the THD of the transmitter current, and decrease the DC-side voltage ripple.

2) A token rotation-based capacitor voltage balancing method of the FCMLI for the WPT system is proposed.

3) The parameter design method of the flying capacitor of the FCMLI for the WPT system is given.

The rest of the paper is organized as follows: Section II presents the proposed Σ-Δ PMM method of the FCMLI-based WPT system. Section III presents the proposed token rotation-based capacitor voltage balancing method of the FCMLI for the WPT system. Section IV presents the simulation and experimental verification. Section V concludes this work.

## II. Delta-Sigma Pulse Magnitude Modulated Multilevel Inverter-Based WPT System

### A. Description of the FCMLI-based WPT System

Fig. 1 shows a typical WPT system based on the FCMLI, where $C_{dc1}$ and $C_{dc2}$ are the DC-side capacitors; $u_1$, $u_2$, $u_3$, …, and $u_{n-2}$ are the voltages of the flying capacitors $C_{f1}$, $C_{f2}$, $C_{f3}$, …, and $C_{fn-2}$; $L_t$ and $L_r$ are the inductances of the transmitter and receiver coils; $R_t$ and $R_r$ are the equivalent series resistances of the transmitter and receiver parts; $M$ denotes the mutual inductance between the primary coil and the secondary coil; $C_t$ and $C_r$ are the capacitances of series compensated capacitors, respectively; $R_{dc}$ and $C_{dc}$ are the DC-link load and capacitor of the diode rectifier. The FCMLI is fed by a DC input voltage $V_{dc}$ and drives a series-series resonant tank. The proposed control of the multilevel inverter consists of two parts: the Σ-Δ-based PMM and the flying-capacitor voltage balancing method. The voltages of the flying capacitors $u_1$, $u_2$, $u_3$, …, and $u_{n-2}$ are sampled for capacitor voltage balancing. The proposed control of the FCMLI-based WPT system will be discussed in sections II.B and III in detail. The resonant frequencies of the resonators on the two sides are given as

$$f_r = \frac{1}{2\pi\sqrt{L_t C_t}} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

The input impedance on the transmitter side of the WPT system can be derived as follows:

$$Z_{in} = j\omega L_t + \frac{1}{j\omega C_t} + R_t + \frac{\omega^2 M^2}{j\omega L_r + \frac{1}{j\omega C_r} + R_r + R_{eq}} \tag{2}$$

where $R_{eq}$ is the equivalent AC load of the diode load.

To equalize the voltage of each switch, the voltages of the $m_{th}$ flying capacitor $C_{fm}$ of the FCMLI should be controlled as

$$V_c(m) = \frac{(n-1-m)V_{dc}}{n-1},\ m = 1,\ 2,\ ...,\ n-2 \tag{3}$$

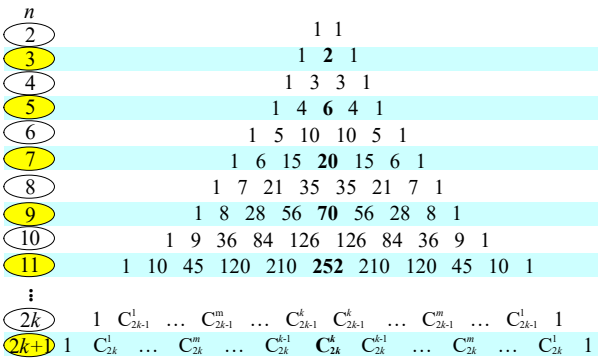


Fig. 2. Redundant switching states of the FCMLI with the arbitrary number of levels.

The output voltage of the $n$-level flying-capacitor inverter is equal to the sum of the MOSFET voltages of all lower side arms, which can be derived as

$$u_t = \frac{V_{dc}}{n-1}\sum_{m=1}^{n-1} S_m \tag{4}$$

Except for 0 and $V_{dc}$, the other voltage levels have redundant switching states. As shown in Fig. 2, according to (4), it can be concluded that there are $C^m_{n-1}$ kinds of switching states to produce the output voltage of $mV_{dc}/(n\text{-}1)$ for the $n$-level flying capacitor inverter.

### B. Proposed PMM Method

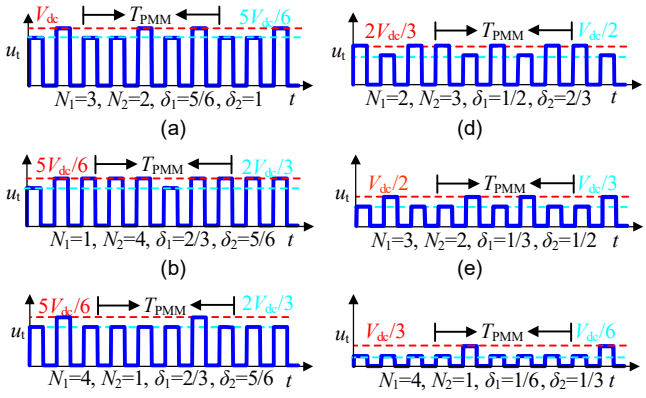


Fig. 3. Output Voltage of seven-level inverters for different $\delta_{PMM}$*. (a) $\delta_{PMM}$*=0.9. (b) $\delta_{PMM}$*=0.8. (c) $\delta_{PMM}$*=0.7. (d) $\delta_{PMM}$*=0.6. (e) $\delta_{PMM}$*=0.4. (f) $\delta_{PMM}$*=0.2.

The series-series compensated WPT system exhibits the bandpass characteristics around the resonant frequency. It can be approximately regarded that only the fundamental component of the output voltage ($u_1$) of the multilevel inverter determines the transfer power of the WPT system. The average magnitude of the fundamental frequency component of the output voltage as shown in Fig. 3 can be expressed as follows:

$$\overline{u_1} = \frac{2V_{dc}}{\pi}\delta \tag{5}$$

where $\delta$ is defined as the normalization output ratio.

For the seven-level flying-capacitor inverter, there are seven kinds of basic voltage pulses, which can be expressed as "$\delta$=0, 1/6, 1/3, 1/2, 2/3, 5/6, and 1". For example, "$\delta$=1" means the voltage pulse with the magnitude at $V_{dc}$ and the frequency at $f_r$, represented as the maximum average voltage. "$\delta$=5/6" means the voltage pulse with the magnitude at $5V_{dc}/6$ and the frequency at $f_r$. The proposed PMM uses the whole-wave voltage pulse with adjacent voltage magnitude to construct the desired output voltage wave. Fig. 3 shows the output voltage pulse of the seven-level flying-capacitor inverter with different $\delta_{PMM}$*. For example, Fig. 3 (a) shows that when $\delta_{PMM}$*=0.9, the output square wave combines the basic voltage pulses of $\delta_1$=5/6 and $\delta_2$=1. Fig. 3 (c) shows that when $\delta_{PMM}$*=0.7, the output square wave combines the basic voltage pulses of $\delta_1$=5/6 and $\delta_2$=2/3.

According to the principle of time averaging, the normalization output ratio of the $n$-level inverter by using the proposed PMM method can be further derived as:

$$\delta_{PMM}{}^* = \frac{N_1\delta_1 + N_2\delta_2}{N_1 + N_2} \tag{6}$$

where the $N_1$ and $N_2$ mean the numbers of the whole-wave voltage pulse with $\delta=\delta_1$ and $\delta=\delta_2$, respectively.

The modulation period of the PMM methods can be calculated as

$$T_{PMM} = (N_1 + N_2)T_s \tag{7}$$

where $T_s$=1/$f_r$.

As shown in Fig. 3, while $\delta_{PMM}$*=0.9, 0.8, 0.7, 0.6, 0.4, and 0.2, all the minimum modulation periods are $5T_s$, which is the minimum solution that can be calculated according to (6).

### C. Sigma-Delta Modulator of PMM

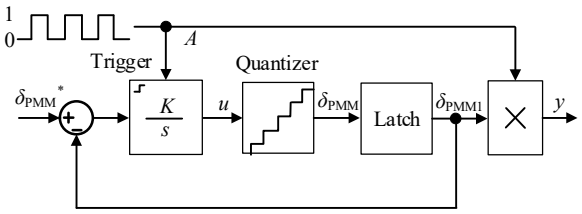


Fig. 4. The proposed Σ-Δ PMM for the multilevel inverter.

Fig. 4 shows the proposed Σ-Δ modulator structure of the PMM of the multilevel inverter for the WPT system. The rising edges of the input pulses trigger the integrator, and the input of the integrator is the difference between the given $\delta_{PMM}$* and the output of the quantizer. It is noticed that the output of the integrator needs to be capped in [0, 1]. According to the output $u$ of the integrator, the quantizer will output the magnitude $\delta_{PMM}$. The quantizer of the Σ-Δ PMM can be given as follows:

$$\begin{cases} \delta_{PMM} = 1, & u \ge \dfrac{2n-3}{2(n-1)} \\ \delta_{PMM} = \dfrac{m}{n-1}, & \dfrac{2m+1}{2(n-1)} \ge u \ge \dfrac{2m-1}{2(n-1)}, m = 1, 2, \ldots, n-2 \\ \delta_{PMM} = 0, & u < \dfrac{1}{2(n-1)} \end{cases} \tag{8}$$

where $n$ is the voltage level number of the multilevel inverter.

Then, the latch is used to keep $\delta_{PMM}$ for at least two control cycles, because the whole-cycle voltage pulse is the minimum unit of the output voltage of the half-bridge multilevel inverter

for the WPT system. The modulation wave is produced by multiplying the output of the quantizer and the input pulse $A$. Finally, the modulation wave will be used as the input of the capacitor voltage balance method in the next chapter. Fig. 5 shows the waveforms of the proposed Σ-Δ PMM modulator and the output voltage and current of the multilevel inverter in detail. The relationship between the output of the Σ-Δ PMM modulator and the output voltage of the multilevel inverter can be given as follows:

$$u_t(t) = y\frac{V_{dc}}{2} \tag{9}$$

It can also be found that the current direction can be judged by the given input pulse ($A$). The transmitter current is positive when $A$=1, and is negative when $A$=0.

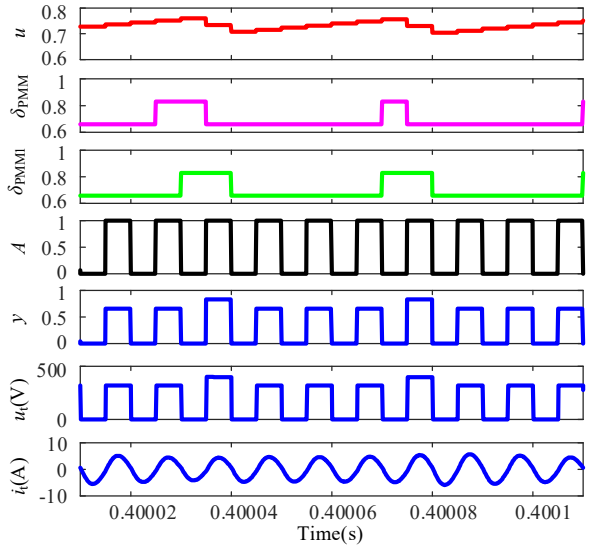


Fig. 5. Waveforms of Σ-Δ modulator with $\delta^*$=0.7 of seven-level FCMLI.

### D. ZVS Analysis

To enable the robust ZVS of the multilevel inverter-based WPT system, the input impedance of the series-series compensated WPT system needs to be slightly inductive at the switching frequency, which can be realized by slightly increasing the transmitter capacitor. Then, the magnitude and phase of the input impedance $Z_{in}$ at the switching frequency can be approximately derived as [26]:

$$|Z_{in}| \approx R_t + \frac{\omega_r{}^2 M^2}{R_r + R_{eq}} \tag{10}$$

$$\tan\alpha \approx \frac{(R_{eq}+R_r)\Delta C}{(\omega_r{}^2 M^2 + R_t R_r + R_t R_{eq})\omega_r C_r{}^2} = k\frac{\Delta C}{C_r} \tag{11}$$

The ZVS of the multilevel inverter can be realized when $Q_{zvs}$, defined as the integral of $i_t$ during the dead time, can charge/discharge all the drain-source capacitors of the MOSFETs from zero to $V_{dc}/(n\text{-}1)$, or vice versa. Taking a seven-level inverter as an example, while "$S_1S_2S_3S_4S_5S_6$" is changed from "111111" to "000000", six upper switches need to be charged from zero to $V_{dc}/6$, and six lower switches need to be charged from $V_{dc}/6$ to zero during the dead time. Thus, in order to realize the ZVS of $n$-level inverter, it can be obtained as follows:

$$Q_{zvs} = \int_0^{T_d} i_t dt \geq \int_0^{V_{dc}/(n-1)} \left(C_{oss1} + C_{oss2} + \cdots C_{ossm} \cdots + C_{oss2n\text{-}2}\right) dv \tag{12}$$

where $C_{oss1}$, $C_{oss2}$, ..., and $C_{oss2n\text{-}2}$ represent the drain-source capacitors of $2n$-2 MOSFETs, respectively.

Assuming that the transmitter current $i_t$ during the dead time is part of the sine waves and all the $C_{oss}$ are the same, (12) can be derived as follows:

$$\int_0^{T_d} I_t \sin(\omega_r t)\, dt \geq \int_0^{V_{dc}/(n-1)} 2(n-1) C_{oss}\, dv \tag{13}$$

Then, according to (13), the minimum phase difference $\alpha_{min}$ and dead time $T_{dmin}$ can be derived as

$$\cos(\alpha_{min}) = 1 - \frac{2\omega_r C_{oss} V_{dc}}{I_t} \tag{14}$$

$$T_{dmin} = \frac{\alpha_{min}}{\omega_r} \tag{15}$$

According to (6), ignoring the influence of the harmonic current, $I_t$ can be calculated as

$$I_t = \frac{2\delta_{PMM} V_{dc}}{\pi |Z_{in}|} \tag{16}$$

Besides, it can be obtained as:

$$(\tan\alpha)^2 + 1 = \frac{1}{(\cos\alpha)^2} \tag{17}$$

Based on (10)-(17), $(\Delta C)/C_r$ can be derived as follows:

$$\frac{\Delta C}{C_r} \geq \frac{1}{k}\sqrt{\frac{\delta_{PMM}{}^2}{(\delta_{PMM} - \pi\omega_r C_{oss}|Z_{in}|)^2} - 1} \tag{18}$$

Although (18) contains no $n$ and $V_{dc}$, the DC-side voltage of the MOSFET $V_{dc}/(n\text{-}1)$ will influence $C_{oss}$. A bigger $C_{oss}$ and a bigger $\delta_{PMM}$ lead to a bigger $\Delta C$. Limited by the transfer power of the WPT system, $\Delta C/C_r$ is suggested to be less than 5% to realize wide-range ZVS during power control [26].

## III. The Proposed Voltage Balancing Method of Multilevel Inverter for WPT System

### A. Switching State Analysis

Whether a flying capacitor is charging or discharging depends on the transmitter current ($i_t$) and the way the flying capacitor is connected to the circuit. The charge or discharge of $C_m$ is determined by the switching state of adjacent switch sets "$S_mS_{m+1}$". As shown in Fig. 6(a) and (d), while "$S_mS_{m+1}$" is selected as "11" and "00", $C_m$ is bypassed, and the transmitter current flows on the upper and lower branches, respectively. As shown in Fig. 6(b) and (c), while "$S_mS_{m+1}$" is selected as "10" and "01", $C_m$ is charged and discharged by the transmitter current, respectively. Moreover, while $i_t$ is the opposite and "$S_mS_{m+1}$" is selected as "10" and "01", $C_m$ is discharged and charged by the transmitter current, respectively. The key information of the FCMLI can be summarized as:

1) The output voltage of the multilevel inverter depends on the number of one in "$S_1S_2S_3 \ldots S_{n-1}$".

2) The charging or discharging pattern of the flying capacitors $C_{f1}$, $C_{f2}$, $C_{f3}$, ..., and $C_{fn\text{-}2}$ depends on the switching

states of "$S_1S_2$", "$S_2S_3$", "$S_3S_4$", ..., and $S_{n-2}S_{n-1}$, and the direction of transmitter current.

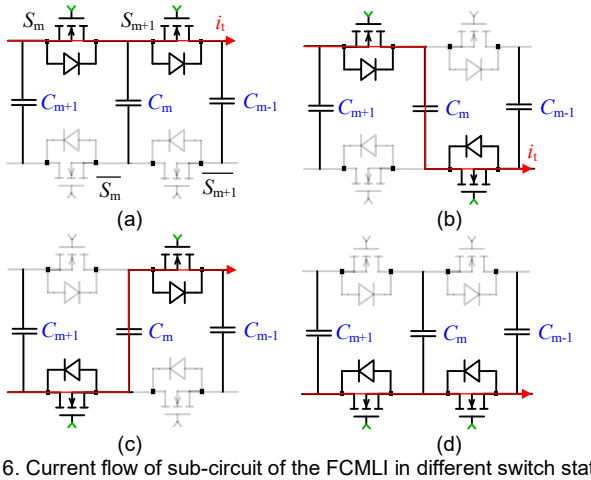


Fig. 6. Current flow of sub-circuit of the FCMLI in different switch states of "$S_mS_{m+1}$". (a) 11 (b) 10 (c) 01 (d) 00.

TABLE I
SWITCHING STATES OF SEVEN-LEVEL INVERTER ($u_t$=0.5$V_{DC}$, $i_t$>0)

| $S_1S_2S_3S_4S_5S_6$ | $u_t$ | $C_{f1}$ | $C_{f2}$ | $C_{f3}$ | $C_{f4}$ | $C_{f5}$ |
|---|---|---|---|---|---|---|
| 000111 | 0.5$V_{dc}$ | – | – | ↓ | – | – |
| 001011 | 0.5$V_{dc}$ | – | ↓ | ↑ | ↓ | – |
| 001101 | 0.5$V_{dc}$ | – | ↓ | – | ↑ | ↓ |
| 001110 | 0.5$V_{dc}$ | – | – | ↓ | ↑ | |
| 010011 | 0.5$V_{dc}$ | – | ↓ | ↑ | – | – |
| 010101 | 0.5$V_{dc}$ | ↓ | ↑ | – | – | – |
| 011001 | 0.5$V_{dc}$ | ↑ | – | – | – | – |
| 011010 | 0.5$V_{dc}$ | – | – | – | ↓ | – |
| 010110 | 0.5$V_{dc}$ | | | | | |
| 011100 | 0.5$V_{dc}$ | – | – | ↓ | – | ↑ |
| 100011 | 0.5$V_{dc}$ | – | ↓ | – | ↑ | – |
| 100101 | 0.5$V_{dc}$ | ↓ | – | ↑ | – | – |
| 100110 | 0.5$V_{dc}$ | – | ↑ | – | – | – |
| 101001 | 0.5$V_{dc}$ | ↑ | – | – | – | ↓ |
| 101010 | 0.5$V_{dc}$ | – | – | ↑ | – | – |
| 101100 | 0.5$V_{dc}$ | – | – | ↓ | – | – |
| 110001 | 0.5$V_{dc}$ | ↓ | – | – | – | ↑ |
| 110010 | 0.5$V_{dc}$ | – | ↓ | – | – | – |
| 110100 | 0.5$V_{dc}$ | ↑ | – | ↓ | – | – |
| 111000 | 0.5$V_{dc}$ | – | – | ↑ | – | – |

According to the above analysis, the charge/discharge states of every flying capacitor can be easily judged by the switching states of $S_1S_2…S_{n-1}$. For example, Table I presents all the charge/discharge states of the seven-level flying-capacitor inverter when the output voltage is 0.5$V_{dc}$ and $i_t$ is positive, where "↓", "↑", and "–" mean the discharging, discharging, and keeping of the flying capacitors, respectively. Furthermore, one special case where the switching state ($S_1S_2…S_6$) is "010101" will be explained. Considering the switching states of $S_1S_2$, $S_2S_3$, and $S_3S_4$, are "01", "10", "01" "10" and "01", thus, when the transmitter current is positive, $C_{f1}$ is discharging, $C_{f2}$ is charging, $C_{f3}$ is discharging, $C_{f4}$ is charging, and $C_{f5}$ is discharging based on the above analysis.

### *B. Token Rotation-based Flying-Capacitor Voltage Balancing Method*

As is required for the FCMLI, the voltage stress of each MOSFET is supposed to be the same or similar value. Thus, the voltages of flying capacitors need to be controlled at the reference value. Fig. 7 shows the token rotation-based charging/discharging sequence of the flying capacitors, where the inner ring represents the charging priority of the capacitors $C_{f1}$, $C_{f2}$, $C_{f3}$, …, and $C_{fn-2}$, and the outer ring represents the position of the token. The position of the token is cyclic along the pointer and it represents the highest priority of charging and discharging of the capacitor. For example, when the token reaches the position of $C_{f1}$, the priority for the charging or discharging of the flying capacitors is "$C_{f1}$>$C_{f2}$> $C_{f3}$>…> $C_{fn-2}$". Then, the token reaches the position of $C_{fn-2}$, and the priority for the charging/discharging of the flying capacitors becomes "$C_{fn-2}$>$C_{f1}$>$C_{f2}$> $C_{f3}$>…> $C_{fn-3}$". After each charging or discharge process is completed, the capacitor charge or discharge priority is changed in turn to ensure that each capacitor voltage can be balanced at the reference value.

First of all, the voltage across each flying capacitor is sensed by an isolated voltage-sensing circuit, and the ADC values $u_1$, $u_2$, …, $u_m$, …, and $u_{n-2}$ are passed to the microcontroller. The deviations of the flying capacitor voltages from their nominal values are given as follows:

$$\begin{cases} a_1 = u_1 - \dfrac{n-2}{n-1}V_{dc} \\ a_2 = u_2 - \dfrac{n-3}{n-1}V_{dc} \\ \vdots \\ a_m = u_m - \dfrac{n-1-m}{n-1}V_{dc} \\ \vdots \\ a_{n-2} = u_{n-2} - \dfrac{1}{n-1}V_{dc} \end{cases} \tag{19}$$

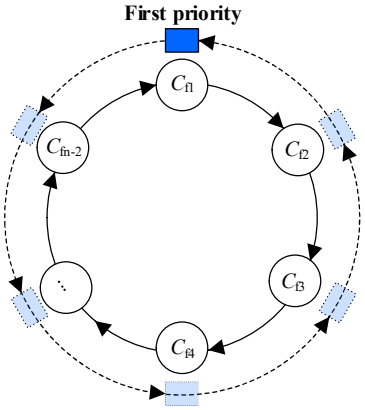


Fig. 7. Token rotation-based charging/discharging sequence of the flying capacitors.

Based on the signs of $A_n$=[$a_1$, $a_2$, …, $a_m$, …, $a_{n-2}$], the optimal switching state will be selected to balance the capacitor voltage. Fig .8 shows the process of switching state selection based on $\boldsymbol{A}_n$, which is divided into two parts. First of all, according to $\boldsymbol{A}_n$, the optimal switching states ($\boldsymbol{B}_n$=[$b_1$, $b_2$, …, $b_m$, …, $b_{n-1}$] ) can be selected. Then, according to modulation wave $y$, the number of one in $\boldsymbol{B}_n$ can be obtained, further determining the final switching states ($\boldsymbol{S}_{nf}$=[ $S_1$, $S_2$, …, $S_m$, …, $S_{n-1}$]).

Fig.9 shows the flow chart of the proposed token rotation-based flying capacitor voltage balance method over one

control cycle. The steps of the proposed token rotation-based flying capacitor voltage balance method of the *n*-level FCMLI can be summarized as follows:

**Step 1:** The first priority is rotated from $C_{fn-2}$- $C_{fn-3}$-…-$C_{fm}$-…-$C_{f3}$-$C_{f2}$-$C_{f1}$-$C_{fn-2}$. It can be realized by a priority sign $j$ in Fig. 9. For example, when $j$=1, the priority of capacitor charge and discharge is $C_{f1}$>$C_{f2}$>…>$C_{fm}$>…>$C_{fn-2}$. Only when 0<$y$<1, does $j$ need to subtract 1 to change the order of priority.

The output of the wave generator ($y$) shown in Fig. 5 consists of "1", "(*n*-2/*n*-1)", …, "0". When $y$=1 and 0, the voltage levels of the multilevel inverter are $V_{dc}$ and 0, respectively. Thus, the switching state is "111…111" and "000…000", and no capacitor is charging/discharging. Therefore, the order of priority is kept when $y$=1 or 0.

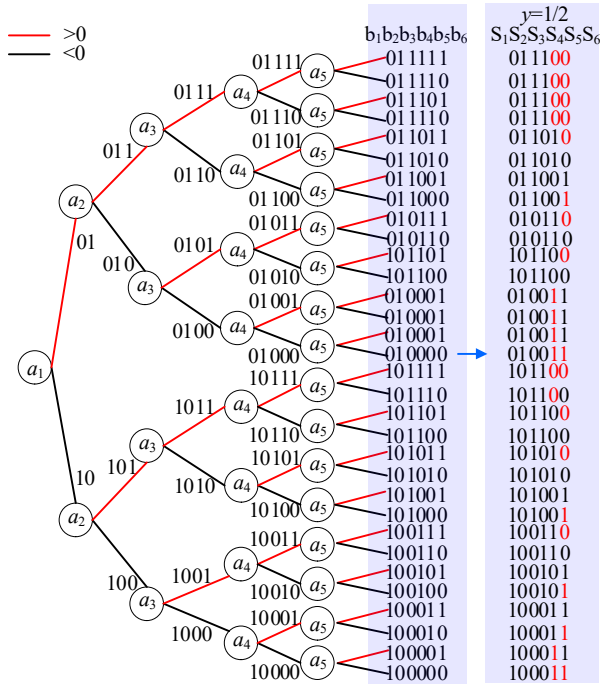


Fig.8 Tree-map-based ideal switching state for different voltage samples of the seven-level FCMLI when $C_{f1}$ is the first priority and $i_t$>0.

**Step 2:** Sampling the voltages ($u_1$, $u_2$, $u_3$, …, $u_{n-2}$) of *n*-2 flying capacitors, then, obtain $a_1a_2a_3$… $a_{n-2}$ according to (20). According to the priority sign, obtain the optimal $b_1b_2b_3$… $b_{n-1}$. First of all, if $a_1$>0, "$b_1b_2$" is selected as "01"; otherwise, "$b_1b_2$" is selected as "10". Then, if $a_m$>0, $b_{m+1}$=1; otherwise, $b_{m+1}$=0, and $m$=2, 3, 4…, $n$-2. Furthermore, if $a_j$>0, $b_j$=0; otherwise, $b_j$=1.

**Step 3:** According to the output of the Σ-Δ PMM for the multilevel inverter ($y$), calculate the limited number of ones in the desired switching states, defined as $i$. Based on (4), the calculation method is given as follows:

$$i = y(n-1) \tag{20}$$

Then, calculate the number of ones in $b_1b_2b_3$… $b_{n-1}$, which is calculated as follows:

$$j = b_1 + b_2 + b_3 + \ldots + b_{n-1} \tag{21}$$

If $i$ equals to $j$, $b_1b_2b_3$… $b_{n-1}$ keeps unchanged; If $i$>$j$, in descending order of the priority sequences, change ($i$-$j$) 1s to 0s in $b_1b_2b_3$… $b_{n-1}$; If $i$<$j$, in descending order of the priority sequences, change ($i$-$j$) 0s to 1s in $b_1b_2b_3$… $b_{n-1}$. Then, $\boldsymbol{S}_{nf}$=[$b_1$; $b_2$; $b_3$… $b_{n-1}$].

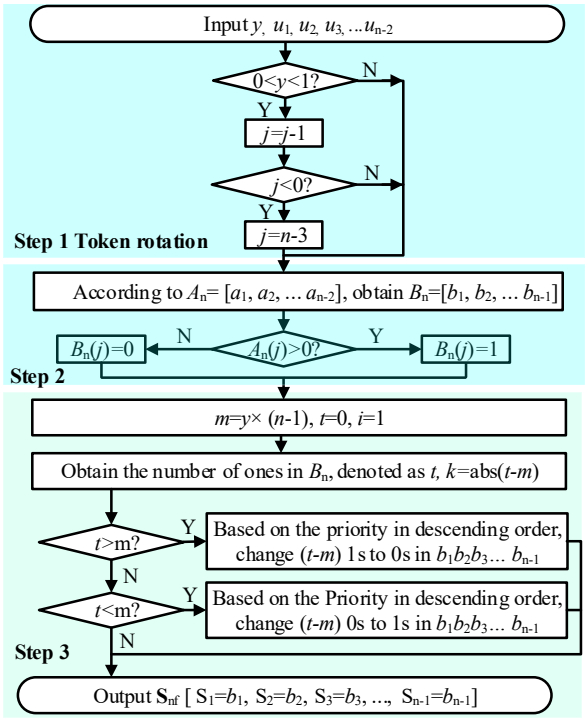


Fig. 9. Flow chart of the token rotation-based flying capacitor voltage balance method for *n*-level inverter-based WPT system.

### C. Capacitor Voltage Balance Analysis

To further explain the charging/discharging process of the proposed token rotation-based capacitor voltage balancing method, Fig. 10 shows an example of the flying capacitor charging/discharging of the seven-level inverter-based WPT system when $\delta_{PMM}^*$=0.7. As shown in Fig. 10, the half-wave transmitter current is used for charge/discharging. The charging and discharging of the flying capacitor of the multilevel inverter is proportional to the integral of the positive half-wave transmitter current of the WPT system. The balancing algorithm execution frequency is twice the switching frequency. During a control period, the voltage variation of $m_{th}$ flying capacitor can be expressed as follows:

$$\Delta u_{cm} = \frac{1}{C_{fm}} \int_0^{T_s/2} i_t(t)\,dt = \frac{I_t T_s}{\pi C_{fm}} \tag{22}$$

where $I_t$ is the peak value of the transmitter current.

A heavier load and a larger $\delta_{PMM}^*$ can lead to a bigger transmitter current. Ignoring the influence of harmonic current, according to (16), $\delta_{PMM}^*$ is proportional to the transmitter current. Thus, the transmitter current can be further derived as follows:

$$I_t = \delta_{PMM}^* I_{tr} = \frac{\pi \delta_{PMM} P_r}{V_{dc}} \tag{23}$$

where $I_{tr}$ and $P_r$ are the rate transmitter current and input rate power of the WPT system, respectively.

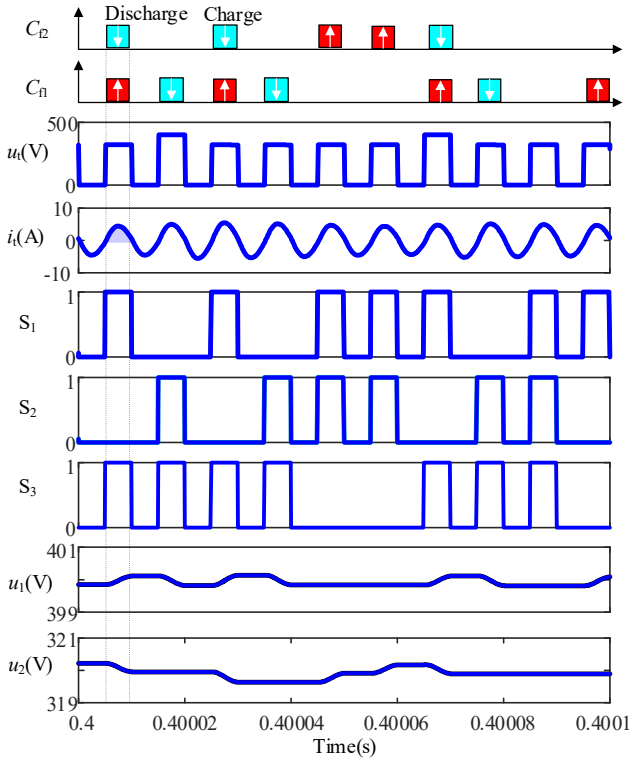


Fig. 10. Simulation results of the flying capacitor charging/discharging of the 7-level inverter when $\delta_{PMM}^*$=0.7 and $C_{f1}$=$C_{f2}$=$C_{f3}$=$C_{f4}$=$C_{f5}$=55 uF.

According to (22)-(23), the voltage ripple of the flying capacitor can be derived as follows:

$$\Delta u_{mn} = N\Delta u_m = \frac{\delta_{PMM} N P_r T_s}{C_{fm} V_{dc}} \le \frac{(n-2) P_r T_s}{C_{fm} V_{dc}} \tag{24}$$

where $1 \le N < n-2$.

As shown in (26), the voltage ripple of every flying capacitor is the same when the capacitor values are the same. The voltage ripple rate of the $m_{th}$ flying capacitors can be defined as follows:

$$\varepsilon_m = \frac{\Delta u_{mn}}{V_c(m)} = \frac{(n-1)\Delta u_{mn}}{(n-1-m)V_{dc}} \tag{25}$$

As shown in Fig. 10, the voltage ripple ($\Delta u_1$) in one control period is 0.36 V, which is consistent with (24). Based on (24) and (26), the $n$-2 capacitors can be selected as follows:

$$C_{fm} \ge \frac{2(n-2)(n-1) P_r T_s}{(n-m-1)\varepsilon_m V_{dc}^2} \tag{26}$$

Furthermore, based on (26), it can be found that while all the flying capacitors are the same, the voltage ripple of $m_{th}$ capacitor can be derived as follows:

$$\varepsilon_m = \frac{n-1-m}{n-2}\varepsilon_1 \tag{27}$$

Moreover, a higher switching frequency leads to a smaller capacitor value required.

## IV. Simulation and Experimental Verification

### A. Hardware Implementation

Fig. 11 shows the 850 W prototype of the seven-level flying capacitor inverter-based WPT system, where the system consists of a DC power source (MR50040), a power analyzer (WT3000), a silicon-carbide-based seven-level flying-capacitor inverter with drivers, a WPT circuit, a bridge rectifier, electronic load (PLZ1003WH), a 24 V auxiliary voltage source, and a TMS320FDSP28377 board. The transmitter and receiver coils are copper Litz wire. The 24 V voltage source is used to feed the auxiliary circuit. The power analyzer with only one channel measures the input power. All flying capacitors have the same capacitance and rated voltage for convenience and lower voltage ripple, consisting of ten parallel MLCCs (450 V/2.2 uF) and one electrolytic capacitor (450 V/33 uF). However, it is noticed that the flying capacitors with different capacitance and rated voltage can be used to reduce the cost in the actual application. The system parameters are listed in Table II.

TABLE II
System Parameters of the WPT System

| Items | Value |
|---|---|
| DC-link voltage ($U_{dc}$) | 480 V |
| Primary (Secondary) capacitance ($C_t$, $C_r$) | (8.7, 8.44) nF |
| Primary (Secondary) coil inductance ($L_t$, $L_r$) | (304.63, 300.15) μH |
| Primary (Secondary) series resistance ($R_t$, $R_r$) | (0.3, 0.3) Ω |
| Coils diameter ($d_1$, $d_2$) | (30, 30) cm |
| Distance between two coils ($d$) | 10 cm |
| Mutual inductance ($M$) | 72.9625 μH |
| Resonant frequency ($f_r$) | 100 kHz |
| Output capacitance ($C_o$) | 220 μF |
| DC capacitors ($C_{dc1}$, $C_{dc2}$) | (100, 100) μF |
| Load resistance ($R_{dc}$) | 57.86 Ω |
| Dead time ($T_d$) | 100 ns |
| Integration coefficient ($K$) | 0.2 |
| Digital signal processer | TMS320F28377 |
| SiC MOSFET | SCT3080 |
| Diode | CVFD20065A |
| Driver | UCC21710 |
| Voltage sample | AMC1311DWVR |

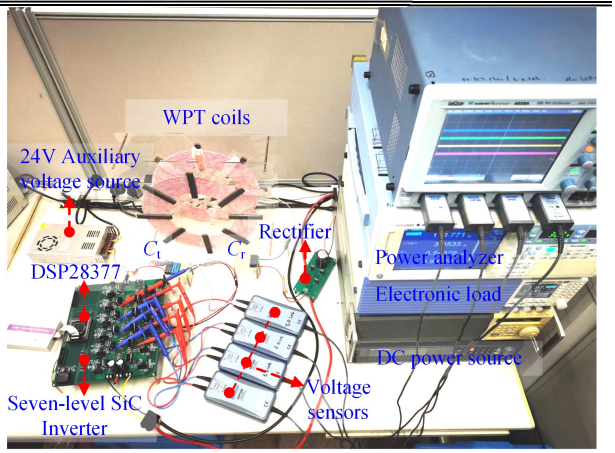


Fig. 11. Experimental platform.

### B. Flying-Capacitor Voltage Balance Analysis

Fig. 12 shows the simulation results of the capacitor voltages of the $n$-level inverter-based WPT system when $\delta_{PMM}^*$=0.7. All the capacitor voltages can be balanced at the reference values at a quick rate, and the start-up times of all the capacitors are less than 0.3 s. Besides, comparing Fig. 12 (a)-(d), it can be found that a bigger $n$ leads to a longer start time of the capacitor voltage. Fig. 12 verifies that the proposed token rotation-based capacitor voltage balance method is

effective for multilevel inverter-based WPT systems with arbitrary voltage levels.

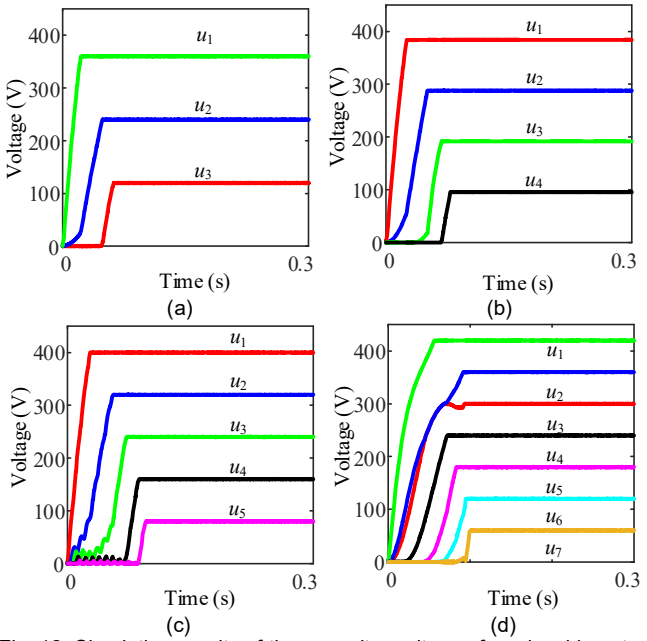


Fig. 12. Simulation results of the capacitor voltages for *n*-level inverter-based WPT system when $\delta_{PMM}^*$=0.7. (a) *n*=3. (b) *n*=4. (c) *n*=5. (d) *n*=7.

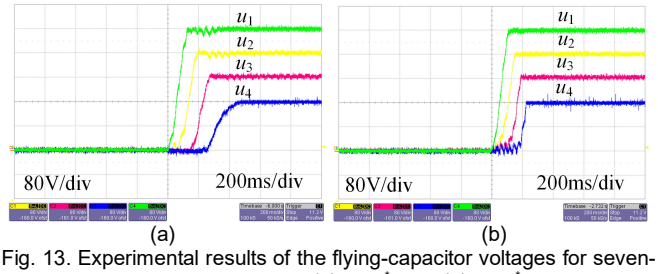


Fig. 13. Experimental results of the flying-capacitor voltages for seven-level inverter-based WPT system (a) $\delta_{PMM}^*$=0.2; (b) $\delta_{PMM}^*$=0.8.

Fig. 13 shows the experimental results of the capacitor voltage of the seven-level inverter for the WPT system with different $\delta_{PMM}^*$. All the capacitor voltages can be balanced at the reference values within 0.42 s while $\delta_{PMM}^*$=0.2, and within 0.24 s while $\delta_{PMM}^*$=0.8. Comparing Fig. 13 (a) and (d), it can be found that a bigger $\delta_{PMM}^*$ leads to a shorter start time of the capacitor voltages. This is because a bigger $\delta_{PMM}^*$ leads to a bigger transmitter current. Fig. 13 further verifies the effectiveness of the proposed token rotation-based capacitor voltage balancing method of the multilevel inverter-based WPT systems.

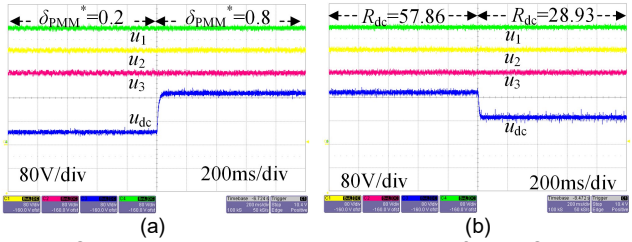


Fig. 14. Output voltage and capacitor voltages of the FCMLI-based WPT system. (a) Increasing $\delta_{PMM}^*$. (b) Decreasing $R_{dc}$.

Fig. 14 shows the flying capacitor voltages and output voltage of the WPT system with step responses. As shown in Fig. 14(a), while $\delta^*$steps from 0.2 to 0.8, the output voltage steps from 44.1 V to 176.0 V within 0.04 s, but the flying capacitor voltages ($u_1$, $u_2$, and $u_3$) have insignificant changes. Similarly, as shown in Fig. 14(b), while $R_{dc}$ steps from 57.86 Ω to 28.93Ω, the output voltage steps from 176.0 V to 88.0 V within 0.02 s, the flying capacitor voltages ($u_1$, $u_2$, and $u_3$) have insignificant changes. The experimental results in Fig. 14 show the stability of the proposed voltage balance method of the FCMLI for the WPT system under step perturbations.

### C. ZVS and Transfer Efficiency Analyses

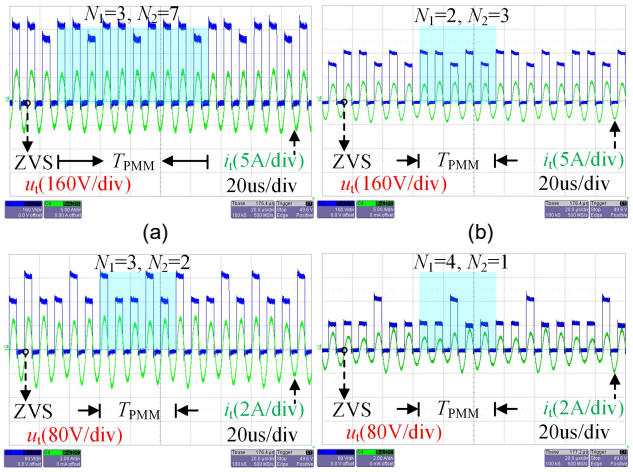


Fig. 15. Inverter output voltages and currents with different $\delta_{PMM}^*$. (a) $\delta_{PMM}^*$=0.95. (b) $\delta_{PMM}^*$=0.6. (c) $\delta_{PMM}^*$=0.4. (d) $\delta_{PMM}^*$=0.2.

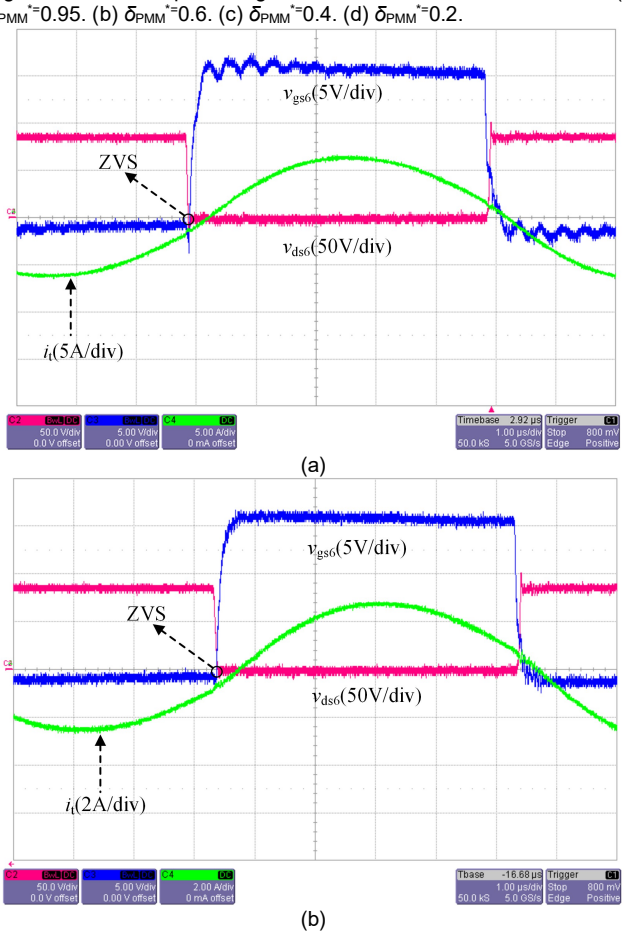


Fig. 16. $V_{gs}$ and $V_{ds}$ and of $Q_6$ and the transmitter current $i_t$ with different $\delta_{PMM}^*$. (a) $\delta_{PMM}^*$=0.95. (b) $\delta_{PMM}^*$=0.4.

The proposed PMM FCMLI-based WPT system features ZVS. With different $\delta_{PMM}^*$ in the PMM, Fig. 15 shows the measured waveforms of the inverter output voltage ($u_t$) and the transmitter current ($i_t$). The system optimization is realized by slightly increasing the transmitter capacitor to enable the robust ZVS reliably. Under the PMM with a variable $\delta_{PMM}^*$, Fig. 15 (a)-(d) shows that the PMM input voltage can energize the transmitter current slightly before the zero-crossing points with a robust ZVS during power control. Furthermore, Fig. 16 shows the gate-source voltage ($v_{gs}$) and drain-source voltage ($v_{ds}$) of $Q_5$ and $Q_6$ when $\delta_{PMM}^*$ equals 0.95 and 0.4, respectively. It can be observed that $v_{gs5}$ and $v_{gs6}$ become high-level voltage after $v_{gs5}$ becomes zero, indicating that $S_5$ and $S_6$ can realize reliable ZVS. As the operating characteristics of the 12 switches are the same, all of them can realize the desired ZVS. Figs. 15 and 16 show that the proposed PMM can realize the wide-range output voltage regulation and ZVS simultaneously. It is noticed that the hard switching appears during the switch-off period, but the SiC MOSFETs turn off near the zero transmitter current. As a result, the power loss caused by the hard switching off is minimal.

Fig. 15 shows that the minimal cycle of $u_t$ is equal to $10T_s$, $5T_s$, $5T_s$, and $5T_s$ when $\delta_{PMM}^*$=0.95, 0.6, 0.4, and 0.2. It can be found that the modulated numbers of whole-cycles $N_1$ and $N_2$ are the minimum solution, which matches the calculated result. For example, in Fig. 15(a), while $\delta_{PMM}^*$=0.95, $\delta_1$ and $\delta_2$ in (8) are 5/6 and 1, respectively. Furthermore, according to (8), it can be obtained that $7N_1=3N_2$. Considering $N_1$ and $N_2$ are positive integers, that "$N_1$=3 and $N_2$=7" are the minimum solution, which is consistent with the experimental result in Fig. 15(a).

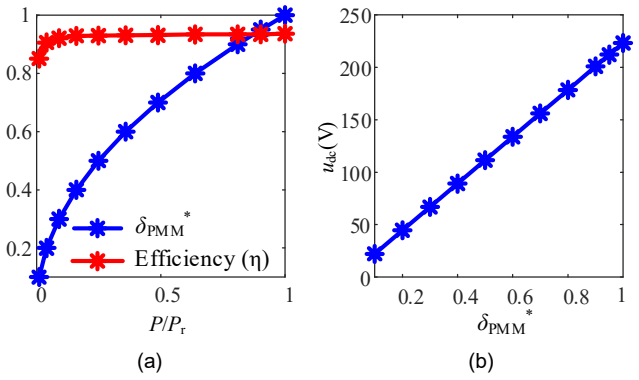


Fig. 17. The relation between the system efficiency, output power, *and* output voltage by changing $\delta_{PMM}^*$. (a) The system efficiency and output power by changing $\delta_{PMM}^*$. (b) The output voltage by changing $\delta_{PMM}^*$.

Besides, Fig. 17 shows the relationship among the system efficiency, output power, output voltage, and $\delta_{PMM}^*$, where $\delta_{PMM}^*$ is selected as [0.1, 0.2, 0.3, 0. 4, 0.5, 0.6, 0.7, 0.8, 0.9, 0.95, 1]. As shown in Fig. 17(a), the system efficiency is kept above 92% in a wide output power range (9%-100% $P_r$, and $P_r$ is the rated power of the WPT system). Besides, Fig. 17(a) shows that the output power is proportional to the square of $\delta_{PMM}^*$, and Fig. 17(b) indicates that the DC-side output voltage is proportional to $\delta_{PMM}^*$. Due to the realization of the ZVS, the system efficiency is high during a wide-range output voltage and output power.

### *D. The Comparison of the Proposed Method and Conventional Methods*

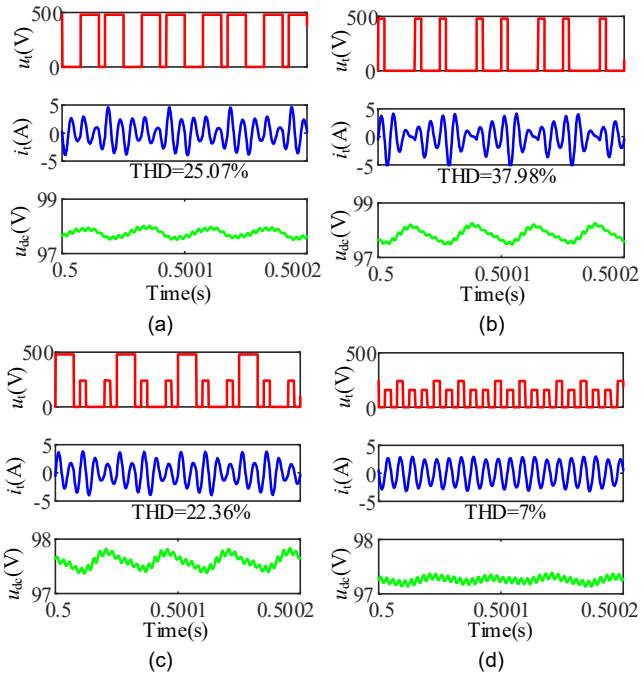


Fig. 18. Waveforms of PFM, PDM, SVPFM, and PMM for $\delta$=0.4. (a) PFM [23]. (b) PDM (c) SVPFM [26] (d) the proposed PMM.

Fig.18 compares the waveforms of the proposed PMM and different modulation methods by using the half-bridge inverter. Both of them have the same circuit and parameters, except that Fig. 18(a) and (b) use the two-level inverter, Fig. 18(c) uses the three-level inverter, and Fig. 18(d) uses the seven-level inverter. It can be shown that the proposed PMM method has the lowest harmonic current on the transmitter side and the lowest DC-side voltage ripple, compared with SVPFM, PFM, and PDM.

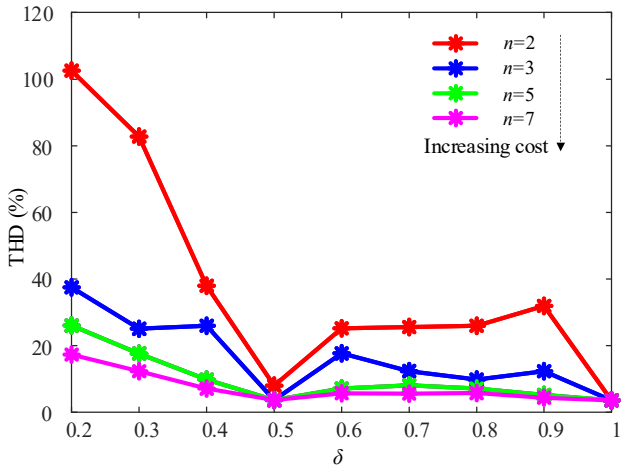


Fig. 19. THD of the transmitter current of the PMM *n*-level inverter-based WPT system.

Reducing THD in the WPT system can lead to increased reliability, compliance, performance, power quality, and lower power loss. The THD of the transmitter current of the WPT system is related to factors such as power level, the

normalized voltage ratio ($\delta$), modulation method, the compensated circuit, etc. Based on the MATLAB/Simulink, Fig. 19 further shows the THD of the transmitter current of the PMM $n$-level inverter-based WPT system under different normalized voltage ratios. It can be observed that a larger $n$ leads to a smaller THD of the PMM multilevel inverter-based WPT system over a wide-range normalized voltage ratio. But when $n$ increases by 1, two additional MOSFETs, an additional set of flying capacitors, and an additional set of voltage sampling circuits are required. The cost of the system increases linearly with an increase in $n$. As shown in Fig. 19, by comparison, the PMM seven-level inverter-based WPT system has the lowest THD and can be connected to the highest DC voltage bus, but it has the highest cost.

## V. Conclusions

The PMM and token rotation-based capacitor voltage balance methods of the multilevel inverter for WPT systems have been proposed and implemented. Some conclusive remarks are summarized below:

1) This paper proposes the Σ-Δ PMM method of multilevel inverters for WPT systems. The proposed PMM has the significant advantage of realizing easily and achieving wide-range voltage regulation and ZVS simultaneously.

2) Besides, the token rotation-based capacitor voltage balancing method of the fly-capacitor multilevel inverter for the WPT system has been proposed. The technique can make the flying-capacitor voltages of the multilevel inverter with arbitrary voltage levels balanced as the reference voltage.

3) The parameter design of the flying capacitor for the proposed PMM multilevel inverter-based WPT system has been given.

Finally, experimental verification is given to verify the feasibility of the proposed modulation method and token rotation-based capacitor voltage balancing method.

## References


[1] Thomas, S. "Connecting with wireless power transfer," *Nat. Electron.* vol. 6, no. 106, Feb. 2023.

[2] C. Jiang, K. T. Chau, C. H. T. Lee, W. Han, W. Liu, and W. H. Lam, "A wireless servo motor drive with bidirectional motion capability," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12001–12010, Dec. 2019.

[3] S. Li, X. Yu, Y. Yuan, S. Lu, and T. Li, "A novel high-voltage power supply with MHz WPT techniques: achieving high-Efficiency, high-isolation, and high-power-density," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 14794-14805, Dec. 2023.

[4] Q. Deng, J. Liu, D. Czarkowski, W. Hu, and H. Zhou, "An inductive power transfer system supplied by a multiphase parallel inverter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 7039-7048, Sept. 2017.

[5] J. H. Kim, B.-S. Lee, J.-H. Lee, S.-H. Lee, C.-B. Park, S.-M. Jung, S.-G. Lee, K.-P. Yi, and J. Baek, "Development of 1-MW inductive power transfer system for a high-speed train," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6242-6250, Oct. 2015.

[6] W. V. Wang, D. J. Thrimawithana and M. Neuburger, "An Si MOSFET-Based High-Power Wireless EV Charger With a Wide ZVS Operating Range," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11163-11173, Oct. 2021.

[7] W. V. Wang, D. J. Thrimawithana, F. Lin and G. A. Covic, "An MMC-based IPT system with integrated magnetics and ZVS operations," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 2425-2436, Feb. 2022.

[8] X.-J. Ge, Y. Sun, Z.-H. Wang, and C.-S. Tang, "A single-source switched capacitor multilevel inverter for magnetic coupling wireless power transfer systems," *Elect. Eng.*, vol. 101, no. 4, pp. 1083–1094, 2019.

[9] J. -Y. Lee, C. -Y. Liao, S. -Y. Yin and K. -Y. Lo, "A multilevel inverter for contactless power transfer system," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 68, no. 1, pp. 401-405, Jan. 2021.

[10] R. Guan, Z. He, L. Fang, J. Qin, Z. Li, Q. Xu, and Y. Chen, "A power self-balanced high step-down medium voltage DC converter With expandable soft-switching range," *IEEE Trans. Ind. Electron.*, vol. 71, no. 1, pp. 398-408, Jan. 2024.

[11] H. Zhou, J. Chen, Q. Deng, F. Chen A. Zhu, W. Hu, and X. Gao, "Input-series output-equivalent-parallel multi-inverter system for high-voltage and high-power wireless power transfer," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 228-238, Jan. 2021.

[12] J. Chevinly, S. Salehi Rad, E. Nadi, B. Proca, J. Wolgemuth, A. Calabro, H. Zhang, F. Lu, "Gallium nitride (GaN) based high-power multilevel H-bridge inverter for wireless power transfer of electric vehicles", 2024 *IEEE Transportation Electrification Conference and Expo (ITEC*), pp.1-5, 2024.

[13] Y. Liu, C. Liu, X. Gao, and S. Liu, "Design and control of a decoupled multichannel wireless power transfer system based on multilevel inverters," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 10045-10060, Aug. 2022.

[14] A. Berger, M. Agostinelli, S. Vesti, J. A. Oliver, J. A. Cobos, and M. Huemer, "A wireless charging system applying phase-shift and amplitude control to maximize efficiency and extractable power," *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6338–6348, Nov. 2015.

[15] Y. Jiang, L. Wang, Y. Wang, J. Liu, X. Li, and G. Ning, "Analysis, design, and implementation of accurate ZVS angle control for EV battery charging in wireless high-power transfer," *IEEE Trans. Ind. Electron*., vol. 66, no. 5, pp. 4075–4085, May 2019.

[16] W. Zhong and S. Y. R. Hui, "Maximum energy efficiency operation of series-series resonant wireless power transfer systems using on-off keying modulation," *IEEE Trans. Power Electron*., vol. 33, no. 4, pp. 3595–3603, Apr. 2018.

[17] Z. Hua, K. T. Chau, W. Han, W. Liu, and T. W. Ching, "Output-controllable efficiency-optimized wireless power transfer using hybrid modulation," *IEEE Trans. Ind. Electron*., vol. 69, no. 5, pp. 4627-4636, May 2022.

[18] H. Li, S. Chen, J. Fang, Y. Tang, and M. A. de Rooij, "A low-subharmonic, full-range, and rapid pulse density modulation strategy for ZVS full-bridge converters," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8871-8881, Sept. 2019.

[19] M. Fan, L. Shi, Z. Yin, L. Jiang, and F. Zhang, "Improved pulse density modulation for semi-bridgeless active rectifier in inductive power transfer system," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5893–5902, Jun. 2019.

[20] V. Yenil and S. Cetin, "An improved pulse density modulation control for secondary side controlled wireless power transfer system using LCC-S compensation," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12762–12772, Dec. 2022.

[21] R. Shinoda, K. Tomita, Y. Hasegawa, and H. Ishikuro, "Voltage-boosting wireless power delivery system with fast load tracker by ΣΔ-modulated sub-harmonic resonant switching," *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 288–289.

[22] X. Li, Y. -P. Li, C. -Y. Tsui and W. -H. Ki, "Wireless power transfer system with Σ-Δ modulated transmission power and fast load response for implantable medical devices," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 64, no. 3, pp. 279-283, Mar. 2017.

[23] W. Liu, K. T. Chau, C. H. T. Lee, W. Han, X. Tian, and W. H. Lam, "Full-range soft-switching pulse frequency modulated wireless power transfer," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6533-6547, June 2020.

[24] J. Tang, T. Na, and Q. Zhang, "A novel full-bridge step density modulation for wireless power transfer systems," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 41-45, Jan. 2023.

[25] W. Ma, B. Zhang, and D. Qiu, "Robust single-loop control strategy for four-level flying-capacitor converter based on switched system theory," *IEEE Trans. Ind. Electron*, vol. 70, no. 8, pp. 7832-7844, Aug. 2023.

[26] J. Guo, K. T. Chau, W. Liu, Z. Hua, and S. Li, "Segmented-vector pulse frequency modulated three-level converter for wireless power transfer," *IEEE Trans. Power Electron.*, vol.39, no. 7, pp. 8959-8972, July 2024.

[27] E. Candan, N. C. Brooks, A. Stillwell, R. A. Abramson, J. Strydom, and R. C. N. Pilawa-Podgurski, "A six-level flying capacitor multilevel converter for single-phase buck-type power factor correction," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6335-6348, Jun. 2022.

[28] C. B. Barth et al., "Design and control of a GaN-based, 13-level, flying capacitor multilevel inverter," *IEEE J. Emerg. Select. Topic Power Electron.*, vol. 8, no. 3, pp. 2179-2191, Sept. 2020.
[29] T. Modeer, N. Pallo, T. Foulkes, C. B. Barth, and R. C. N. Pilawa-Podgurski, "Design of a GaN-based interleaved nine-level flying capacitor multilevel inverter for electric aircraft applications," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12153-12165, Nov. 2020.
[30] G. Kampitsis, E. I. Batzelis, A. Kolokasis, E. Matioli, and B. C. Pal, "A Generalized phase-shift PWM extension for improved natural and active balancing of flying capacitor multilevel inverters," *IEEE Open J. Power Electron.*, vol. 3, pp. 621-634, 2022.
[31] J. Ebrahimi, H. Karshenas, S. Eren and A. Bakhshai, "An optimized capacitor voltage balancing control for a five-level nested neutral point clamped converter," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2154-2165, Feb. 2021.
[32] J. Ebrahimi, S. Shahnooshi, S. Eren, H. Karshenas and A. Bakhshai, "Optimized switching frequency voltage balancing schemes for flying capacitor based multilevel converters," *IEEE Trans. Ind. Electron*, vol. 70, no. 11, pp. 10775-10788, Nov. 2023.

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