

Pulse Increment Modulation of Three-Level Inverter-based Wireless Power Transfer

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Abstract—Multilevel inverters have attracted more and more attention in high-power WPT systems, but their switching loss is a worrying issue. To solve this problem, this article proposes and implements a sigma-delta pulse increment modulation (PIM) of a full-bridge three-level flying-capacitor inverter for wireless power systems. The proposed method outperforms the segmented vector pulse frequency modulation of the three-level full-bridge inverter-based WPT system for lower harmonics and an easier realization. A commutative flying-capacitor voltage balancing and switch-state selecting method of the three-level full-bridge inverter for the WPT is also proposed. It can balance the capacitor voltage with dynamic perturbations and eliminate the voltage spike caused by current commutation. Finally, theoretical analysis, simulations, and hardware experimentation are given further to verify the effectiveness of the proposed Σ - Δ PIM WPT system.

Index Terms—Wireless power transfer; Pulse increment modulation; Three-level full-bridge inverter; Zero voltage switching

I. INTRODUCTION

Wireless power transfer (WPT) technology can be traced back over one century to the work of Nikola Tesla and has been applied to a wide range of fields with power levels ranging from milliwatts to megawatts [1]-[5], helping to charge micro-robots, electric toothbrushes, electric vehicles, and high-speed train, due to electrical isolation, the safety, convenience, and better user experience. As a key point, modulation methods of the converter for the WPT system have been a research hotspot from academia.

The modulation methods for the WPT system originated from communication technology. Based on the principle of time averaging, many significant modulation methods of two-level inverter-based wireless power systems have been fully studied, including pulse-width modulation (PWM), on-off keying modulation, pulse frequency modulation (PFM), hybrid modulation, pulse density modulation (PDM), and step density modulation (SDM), and so on. The control object of the PWM is the duty ratio or phase-shift angle. As a kind of PWM with a controllable angle, phase-shift control (PSC) [6]-

[8] is generally utilized in the converters of the WPT system, but it is difficult to achieve zero-voltage switching (ZVS) in a wide range of load variation. The on-off modulation uses the low-frequency on-off duty ratios to control the converter [9], causing large output ripples. The PFM for WPT systems is proposed in [10]-[13], and it regulates the output power by using high-order harmonics of the square wave at a specific frequency. The Σ - Δ PFM is also presented in [11]-[12] to decrease the output ripple, but its realization is complicated. To maintain the high efficiency of the WPT system in all operating ranges, the hybrid modulation combining the PFM and on-off modulation is proposed in [15], but it suffers from the same issue of the large output ripple. Compared with PFM, PDM is easier to implement, and it regulates the output power by varying the density of the pulses [16]-[19]. To obtain contentious outputs, the Σ - Δ PDM is proposed and applied to WPT systems [16]. Then, the PDM has been gradually improved by several works to decrease the subharmonic, and enhance the dynamic characteristic and stability [17]-[20], but it has bad characteristics in the half-bridge inverter-based WPT system. From a new perspective, SDM using the density of steps to regulate the output power is proposed in [21], owning both advantages of PDM and PFM.

Recently, the WPT system based on multilevel inverters has attracted more and more attention due to the advantage of realizing a large operating range and breaking voltage limitations [22]-[24]. It has been studied for low-voltage high-power EV charging whose loading conditions can vary up to 450% [23]. Besides, multilevel inverter-based WPT systems can be connected to the medium-voltage DC power system to reduce the voltage stress for each semiconductor component. Moreover, multilevel inverters have been applied for decoupled multichannel WPT systems to simplify the system configuration [24]. Compared with the two-level converter-based WPT system, the modulation methods of the multilevel converter for the WPT system are more flexible due to the additional freedom of the pulse magnitude.

Multiple PWM waves with different frequencies are superposed for the multilevel inverter-based multichannel WPT systems [24], but the modulation method has the problem of hard switching. The ZVS modulation method of the MMC-based inductive power transfer system is proposed in [23]. It changes the number of submodules connected to the circuit to adjust the pulse magnitude of the MMC, but the output voltage magnitude of the MMC is discrete. Our previous work proposes the segmented vector pulse frequency modulation (SVPFM) method of the three-level flying capacitor inverter-based WPT system [25], and the control objects are the magnitude and frequency of the voltage pulse together, but the algorithm is complex, and the total harmonic

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TABLE I
COMPARISON BETWEEN THE PROPOSED PIM AND THE CONVENTIONAL ONES

	[27] PDM	[12] PFM	[24]	[23]	[25]SVPFM	Proposed
Output voltage	continuous	continuous	continuous	discrete	continuous	continuous
ZVS range	wide	wide	very narrow	wide	wide	wide
MOSFET voltage stress	v_{in}	v_{in}	v_{in}	$v_{in}/(n-1)$	$0.5v_{in}$	$0.5v_{in}$
Voltage levels	Two	Two	Three	n	Three	Three
Control complexity	simple	complex	simplest	complex	most complex	simple
Interharmonic of current	low	highest	N/A	N/A	high	lowest

distortion (THD) of the transmitter current is high, especially when under a light load. In this paper, from a new perspective, an Σ - Δ pulse increment modulation of a three-level inverter is proposed, and its control object is the pulse magnitude increment. Table I compares the proposed method and the above typical methods. Compared with the above methods [23]-[25], the proposed method can achieve a wide-range ZVS, a continuously adjustable output voltage, and a low THD simultaneously, and the algorithm is relatively simple. The main contribution is listed as:

1) The Σ - Δ pulse increment modulation (PIM) is proposed to realize the wide-range ZVS and low harmonics of the flying capacitor full-bridge three-level inverter (FCTLFI)-based WPT systems.

2) The commutative capacitor voltage balancing method of the FCTLFI for the WPT system is proposed. It can balance the flying-capacitor voltage of the full-bridge inverter and eliminate the voltage spike.

The rest of the paper is organized as follows: Section II presents the proposed Σ - Δ PIM and capacitor voltage balancing and switching state selecting methods of the FCTLFI-based WPT. Section III presents its characteristic analysis. Section IV presents the experimental verification. Section V concludes this work.

II. PULSE INCREMENT MODULATED THREE-LEVEL FULL-BRIDGE INVERTER-BASED WPT SYSTEM

A. Three-Level Full-Bridge Inverter-Based WPT System

Fig. 1 shows the circuit and control of a series-series compensated WPT system, including a DC voltage source U_{dc} , an FCTLFI, a transmitter coil, a receiver coil, and a diode rectifier load. C_a and C_b are the flying capacitors of the three-level full-bridge inverter. L_t and L_r are the self-inductances of the coupler, respectively. The power is transferred from the transmitter side to the receiver side via the mutual inductance M . Besides, R_t and R_r are the parasitic resistances of the coils. C_t and C_r are compensated capacitors on the transmitter and receiver sides. The three-level full-bridge inverter operates at the resonant frequency of the LC resonators, and the relationship between the LC resonators is

$$\omega_r = 2\pi f_r = \frac{1}{\sqrt{L_t C_t}} = \frac{1}{\sqrt{L_r C_r}} \quad (1)$$

The circuit equation of the WPT system can be given as

$$\begin{bmatrix} u_t \\ 0 \end{bmatrix} = \begin{bmatrix} j\omega L_t + 1/(j\omega C_t) + R_t & j\omega M \\ j\omega M & j\omega L_r + 1/(j\omega C_r) + R_r + R_{eq} \end{bmatrix} \begin{bmatrix} i_t \\ i_r \end{bmatrix} \quad (2)$$

where R_{eq} is the equivalent load of the diode rectifier load, and $R_{eq} = 8R_{dc}/\pi^2$; R_{dc} is the dc-link load.

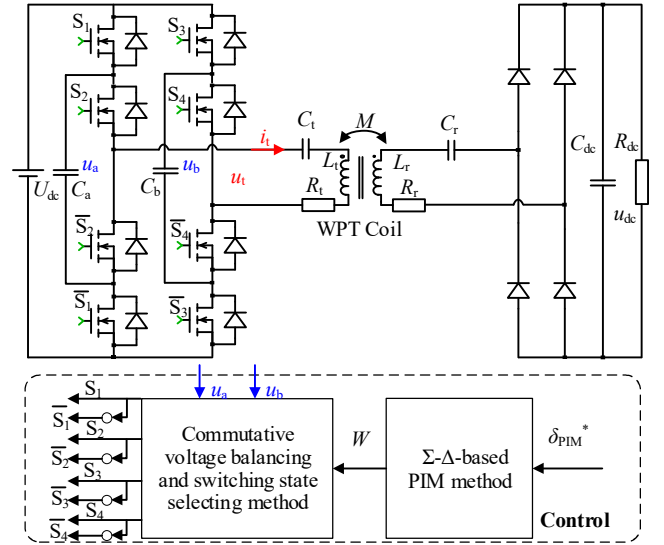


Fig. 1. The FCTLFI-based WPT system by using the proposed PIM.

B. Principle of Proposed PIM

The WPT system characterizes the bandpass filter around the resonant frequency. It can be approximately regarded that only the fundamental component of the output voltage u_t of the flying-capacitor full-bridge multilevel inverter determines the transfer power of the WPT system. The fundamental component of the output voltage of the multilevel inverter u_t is proportional to pulse magnitude increments. Thus, the adjustment object of the PIM can be the pulse magnitude increment, and the principle of PIM is averaging different voltage pulse magnitude increments to regulate the output power. Voltage pulse magnitude increments of the n -level full-bridge inverter are shown in Fig. 2 (a). The n -level full-bridge inverter can generate $2(n-1)$ types of voltage increments: $-2V_{dc} + 2mU_{dc}/(n-1)$, which are denoted as " $\Delta M = -2 + 2m/(n-1)$," in Fig. 2(a), respectively, and $m = 1, 2, 3, \dots, n-2$. For example, as shown in Fig. 2 (b), all the voltage magnitude increments of the three-level full-bridge inverter are obtained as: $-2U_{dc}$, $-1.5U_{dc}$, $-U_{dc}/2$, 0 , $U_{dc}/2$, U_{dc} , $1.5U_{dc}$, $2U_{dc}$, as shown in Fig.3, which are denoted as $\Delta M = -2$, $\Delta M = -1.5$, $\Delta M = -1$, $\Delta M = -0.5$, $\Delta M = 0$, $\Delta M = 0.5$, $\Delta M = 1$, $\Delta M = 1.5$, and $\Delta M = 2$, respectively. The voltage pulse magnitude increment can be positive or negative. While the incremental magnitudes are the same, the positive and negative increments can be regarded as one kind.

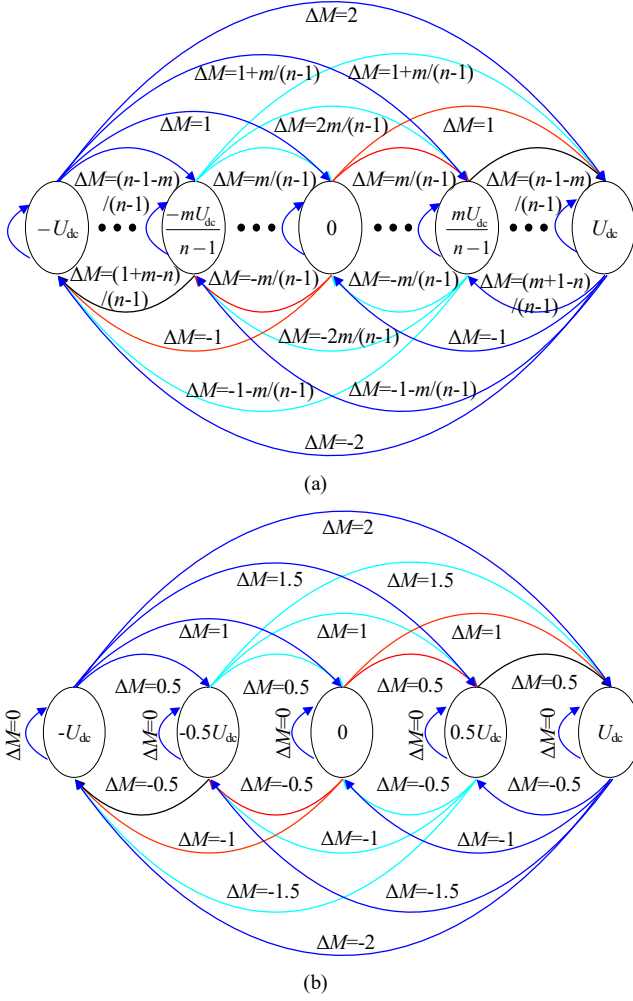


Fig. 2. Voltage increment of multilevel inverter (a) n -levels (b) three levels.

First of all, the normalized voltage ratio δ is defined as:

$$u_{r1} = \frac{4\delta U_{dc}}{\pi} \quad (3)$$

The control object of the PIM is the voltage pulse magnitude increment, as shown in Fig. 2, and the minimum units of PIM are shown in Fig. 3. It is noticed that the period of the voltage increment is half the switching period. The output of the PIM combines one or two different kinds of pulse magnitude increments. In terms of the three-level full-bridge inverter, δ_{PIM}^* will be divided into four different intervals: $[0, 0.25]$, $(0.25, 0.5]$, $(0.5, 0.75]$, and $(0.75, 1.0]$, as shown in Table II. When $0.5|\Delta M_1| < \delta_{PIM}^* \leq 0.5|\Delta M_2|$, the output voltage only contains two modes of the pulse increments with $|\Delta M_1|$ and $|\Delta M_2|$, and $|\Delta M_2| - |\Delta M_1| = 0.5$. In the same interval, the density of the pulse increments with $|\Delta M_1|$ and $|\Delta M_2|$ are changed to form different δ_{PIM} . As shown in Fig. 4(a), the normalized voltage ratio of the PIM for the three-level full-bridge inverter can be derived as:

$$\delta_{PIM} = \frac{N_1 |\Delta M_1| + N_2 |\Delta M_2|}{2(N_1 + N_2)} = 0.5|\Delta M_1| + \frac{0.25N_2}{(N_1 + N_2)} \quad (4)$$

where the N_1 and N_2 mean the numbers of the voltage increments with $|\Delta M| = |\Delta M_1|$ and $|\Delta M| = |\Delta M_2|$, respectively; $|\Delta M_2| = |\Delta M_1| + 0.5$.

Note that the sum of N_1 and N_2 has to be an even number, and the periodical repetition of voltage pulse increment determines a period T_{PIM} that is an integer multiple of the switching period. The minimum modulation period of the PIM can be calculated as follows:

$$T_{PIM} = 0.5(N_{1min} + N_{2min})T_s \quad (5)$$

where $T_s = 1/f_r$, N_{1min} , and N_{2min} are the minimum numbers that satisfy (4).

TABLE II
COMBINATION FOR DIFFERENT δ_{PIM}^*

$ \Delta M_1 = 0$	$ \Delta M_1 = 0.5$	$ \Delta M_1 = 1$	$ \Delta M_1 = 1.5$
$ \Delta M_2 = 0.5$	$ \Delta M_2 = 1$	$ \Delta M_2 = 1.5$	$ \Delta M_2 = 2.0$
$\frac{0.25N_2}{N_1 + N_2}$	$\frac{0.25N_1 + 0.5N_2}{N_1 + N_2}$	$\frac{0.5N_1 + 0.75N_2}{N_1 + N_2}$	$\frac{0.75N_1 + N_2}{N_1 + N_2}$
$0.25 \geq \delta_{PIM}^* \geq 0$	$0.5 \geq \delta_{PIM}^* > 0.25$	$0.75 \geq \delta_{PIM}^* > 0.5$	$1.0 \geq \delta_{PIM}^* > 0.75$

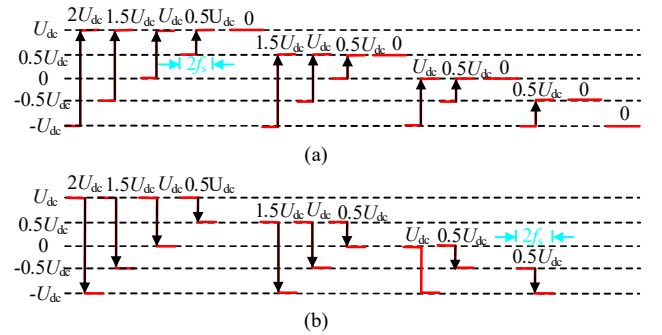


Fig. 3. Minimum units of PIM for three-level full-bridge inverter (a) $\Delta M \geq 0$. (b) $\Delta M < 0$.

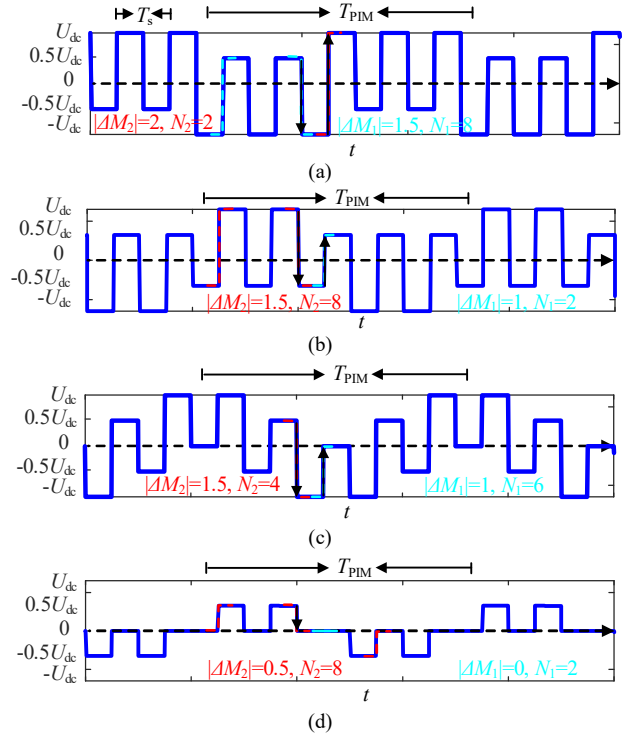


Fig. 4. Output voltage of three-level inverters for different δ_{PIM}^* using PIM. (a) $\delta_{PIM}^* = 0.8$. (b) $\delta_{PIM}^* = 0.7$. (c) $\delta_{PIM}^* = 0.6$. (d) $\delta_{PIM}^* = 0.2$.

For a clear explanation, Fig. 4 shows the output voltage when $\delta_{PIM}^* = 0.8, 0.7, 0.6$, and 0.2 . When $\delta_{PIM}^* = 0.8$, it can be obtained that $N_1 = 4N_2$ from (4). Considering that the sum of N_1

and N_2 is an even number, $N_{1\min}$ and $N_{2\min}$ should be 8 and 2, respectively. It is consistent with the results in Fig. 4 (a), where the output voltage pulse consists of two voltage pulse increments with $|\Delta M_2|=2$ and eight voltage pulse increments with $|\Delta M_1|=1.5$ in the minimum modulated cycle. When $\delta_{\text{PIM}}^*=0.7$, $|\Delta M_1|$ and $|\Delta M_2|$ will be 1 and 1.5, respectively. Then, it can be calculated that $N_2=4N_1$. Thus, $N_{1\min}$ and $N_{2\min}$ in a modulated period should be 2 and 8, respectively, as shown in Fig. 4(b). While $\delta_{\text{PIM}}^*=0.6$, $|\Delta M_1|$ and $|\Delta M_2|$ will be 1 and 1.5, respectively. Then, it can be obtained that $2N_1=3N_2$. Thus, $N_{1\min}$ and $N_{2\min}$ should be 6 and 4, respectively, as shown in Fig. 4(c). While $\delta_{\text{PIM}}^*=0.2$, $|\Delta M_1|$ and $|\Delta M_2|$ will be 0 and 0.5, respectively. Then, it can be obtained that $N_2=4N_1$. Thus, $N_{1\min}$ and $N_{2\min}$ should be 2 and 8, respectively, which is shown in Fig. 4(d). Furthermore, it can be found the modulation periods of the PIM when $\delta_{\text{PIM}}^*=0.8, 0.7, 0.6$, and 0.2 are $5T_s$.

C. Proposed Delta-Sigma Modulator for PIM

The delta-sigma modulation for the WPT system is generally applied for high-density resolution, which is based on the principle of time averaging. Fig. 5 shows the proposed Σ - Δ modulator structure of the PIM for the FCTLFI-based WPT system. The input signals of the PIM modulator consist of a clock signal A whose frequency is equal to f_t and a specified normalized voltage ratio δ_{PIM}^* . The rising or falling edges of the input pulses trigger the integrator, and the input of the integrator is the difference between the given δ_{PIM}^* and $0.5|\Delta M_b|$. According to the output of the integrator, the quantizer will output the absolute value k of the magnitude increment. The quantizer in Fig. 5 for the FCTLFI-based WPT system can be given as:

$$\begin{cases} k = 2, & u \geq 0.875 \\ k = 1.5, & 0.875 > u \geq 0.625 \\ k = 1.0, & 0.625 > u \geq 0.375 \\ k = 0.5, & 0.375 > u \geq 0.125 \\ k = 0, & u < 0.125 \end{cases} \quad (6)$$

Meantime, there are five kinds of zero increments as shown in Fig.3. Only zero increments appearing at zero voltage level are applied. Thus, a limited condition is added as follows:

$$o = 0.5, k = 0 \text{ \& \& } W_{\text{last}} \neq 0 \quad (7)$$

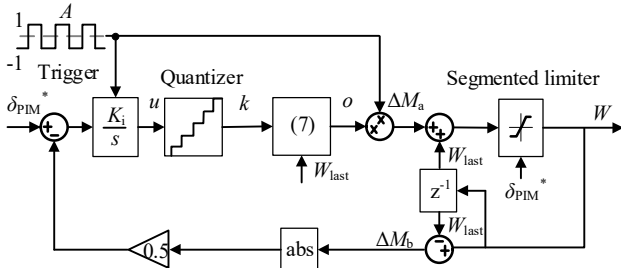


Fig. 5. Proposed Σ - Δ PIM of three-level inverter for the WPT system.

The pulse increment ΔM_a is produced by multiplying the output of the quantizer k and the input pulse signal A . Then, the pulse increment is accumulated to obtain the voltage pulse magnitude. Moreover, considering the limitation of the pulse magnitude, a segmented limiter in Fig. 5 is added. When $0 \leq \delta_{\text{PIM}}^* \leq 0.5$, the range of the limiter is $[-0.5, 0.5]$. When

$0.5 \leq \delta_{\text{PIM}}^* \leq 1$, the range of the limiter is $[-1, 1]$. Moreover, the segmented limiter might change the actual pulse increment, causing the final pulse increment $\Delta M_b \neq \Delta M_a$. Thus, the actual pulse increment $|\Delta M_b|$ is regarded as a feedback variable of the Σ - Δ modulator for accurate output, instead of $|\Delta M_a|$. The relationship between the modulated wave W and the output voltage of the FCTLFI can be expressed as

$$u_t = WU_{\text{dc}} \quad (8)$$

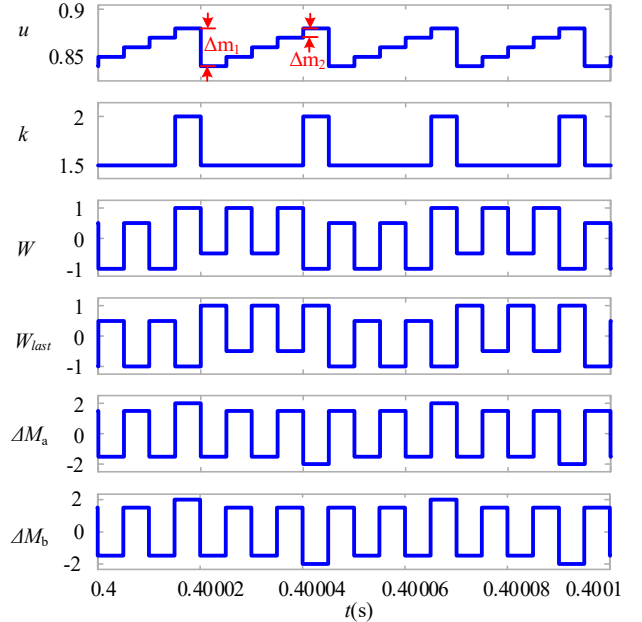


Fig. 6. Waveforms of the proposed Σ - Δ modulator of PIM when $\delta_{\text{PIM}}^*=0.8$.

Fig. 6 shows the waveform of the proposed Σ - Δ PIM when $\delta_{\text{PIM}}^*=0.8$. The integration coefficient K_i as shown in Fig. 5 is an important parameter that determines the stability of the Σ - Δ PIM. As shown in Fig. 6, Δm_1 and Δm_2 are defined as the decrement and increment of u caused by the integrator in a control cycle. When δ_{PIM}^* ranges in $[n/4, (n+1)/4]$, $n=0, 1, 2$, and 3 , Δm_1 and Δm_2 can be calculated as follows:

$$\begin{cases} \Delta m_1 = K_i \left(\frac{n+1}{4} - \delta_{\text{PIM}}^* \right) \\ \Delta m_2 = K_i \left(\delta_{\text{PIM}}^* - \frac{n}{4} \right) \end{cases} \quad (9)$$

While δ_{PIM}^* is fixed, u needs to remain in a fixed zone to ensure the stability of the Σ - Δ PIM. For example, while $0.75 < \delta_{\text{PIM}}^* \leq 1$, $u \geq 0.625$. Thus, $\Delta m_{1\max}$ and $\Delta m_{2\max}$ should be less than 0.25. According to (9), $\Delta m_{1\max}=0.25K_i$ and $\Delta m_{2\max}=0.25K_i$. Therefore, K_i should be less than 1 to ensure the stability of the Σ - Δ PIM. In Fig.6, $K_i=0.2$ is used as an example.

D. Voltage Balancing of FCTLFI for WPT System

Sixteen switching states (0000, 0001 ... and 1111) of the eight SIC-MOSFETs (S_z and $\bar{S}_z$, $z \in \{1, 2, 3, 4\}$) are available to generate five levels of inverter output voltage. For example, Fig. 7(a) shows the “1101” switching operation of the FCTLFI, where S_1 , S_2 , and S_4 turn on, while S_3 turns off, and C_b is charged while C_a is kept. Fig. 7(b) shows the “1110” switching operations, where S_1 , S_2 , and S_3 turn on, while S_4

turns off, and C_b is discharged while C_a is kept. Fig. 7(c) shows the “0100” operations, where C_a is discharged while C_b is kept. Fig. 7(d) shows the “1000” switching operation, where C_a is charged while C_b is kept.

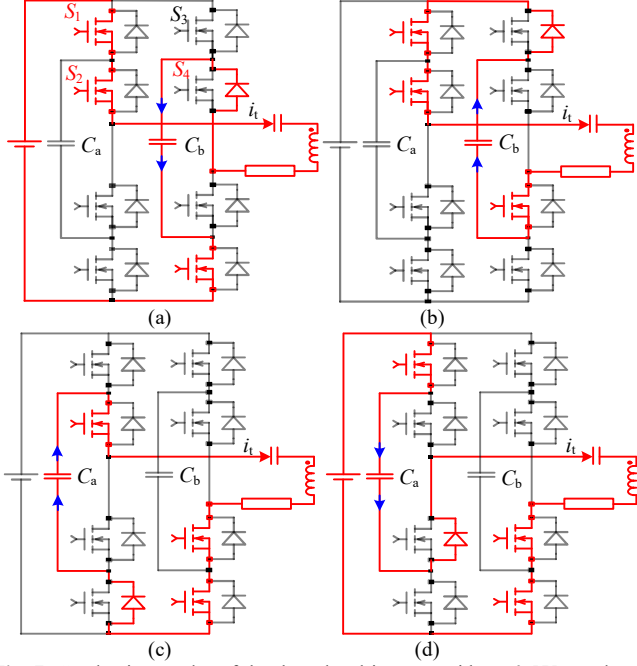


Fig. 7. Conduction modes of the three-level inverter with $u_i=0.5U_{dc}$, and $i_i>0$ for different switching states. (a) 1101. (b) 1110. (c) 0100. (d) 1000.

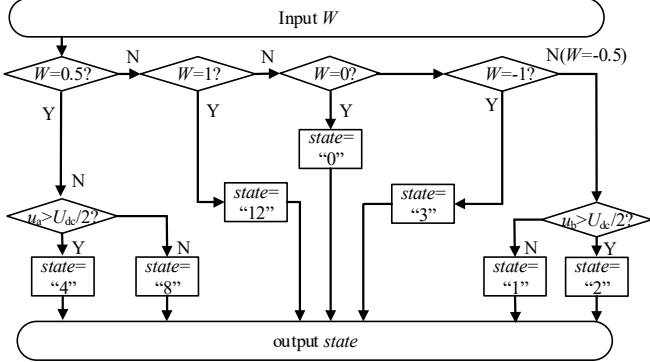


Fig. 8. Proposed commutative voltage balancing method.

Fig. 8 shows the proposed voltage balancing method. The output of the wave generator W shown in Fig. 5 consists of “1”, “0.5”, “0”, “-0.5”, and “-1”. When $W=1$ and -1 , the output voltages are U_{dc} and $-U_{dc}$, and the switching states are selected as “1100”, denoted as “state=12” and “0011”, denoted as “state=3” in Fig. 8, respectively.

There are many redundant switching states for zero voltage and $U_{dc}/2$. An inappropriate switching state selection can lead to voltage spikes in the output voltage of the FCTLFI. One of the state-selecting methods to avoid the voltage spike of the output voltage is shown in Fig. 8.

If $W=0.5$, i_i will be positive, and C_a needs to be charged or discharged. If $u_a \geq U_{dc}/2$, the switching state is selected as “0100”, denoted as “state=4” in Fig. 8. If $u_a < U_{dc}/2$, the switching state is selected as “1000” to charge C_b , denoted as “state=8” in Fig. 8. If $W=-0.5$, i_i will be negative, and C_b needs to be charged or discharged. If $u_b \geq U_{dc}/2$, the switching state is selected as “0001”, denoted as “state=1” in Fig. 8. If

$u_b < U_{dc}/2$, the switching state is selected as “0010”, denoted as “state=2” in Fig. 8. Considering that “0001”, “0010”, “0100” and “1000” are selected for $-0.5U_{dc}$ and $0.5U_{dc}$, the switching state for zero voltage can only be selected as “0000”, denoted as “state=0” in Fig. 8. The ab -phase capacitors will be charged in turn by using the method in Fig. 8 to avoid the voltage spike. It is worth noting that δ_{PIM}^* needs to be preset as some value, such as 0.2, to start the system and balance the flying capacitor voltages first.

III. ANALYSIS OF PIM FCTLFI-BASED WPT SYSTEM

A. Harmonic Comparative Analysis

The output voltage of the three-level full-bridge inverter can be represented by a Fourier series of [14], [26]

$$u_i(t) = \sum_{n=-\infty}^{\infty} k_n e^{2\pi n f_0 t} \quad (10)$$

where f_0 is called the fundamental frequency, and k_n is the Fourier coefficient at the n th harmonic. The harmonic frequency can be derived as follows:

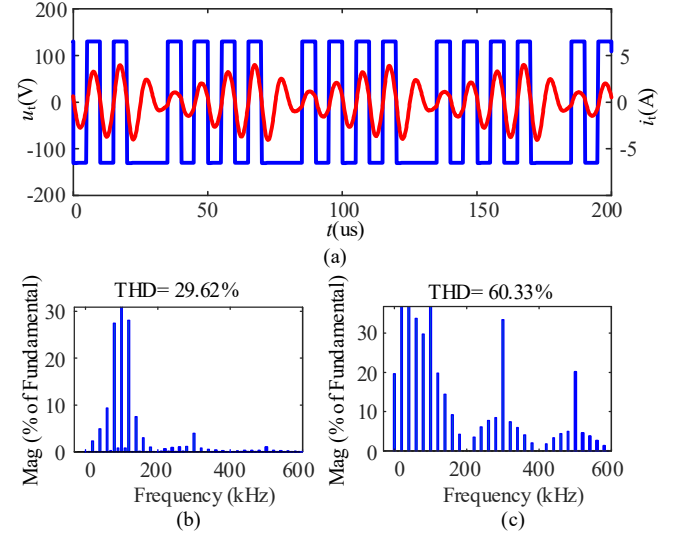


Fig. 9. Waveforms of the SVPFM WPT system and FFT analysis (a) Transmitter current i_i and inverter voltage u_i (b) DFT of i_i . (c) DFT of u_i .

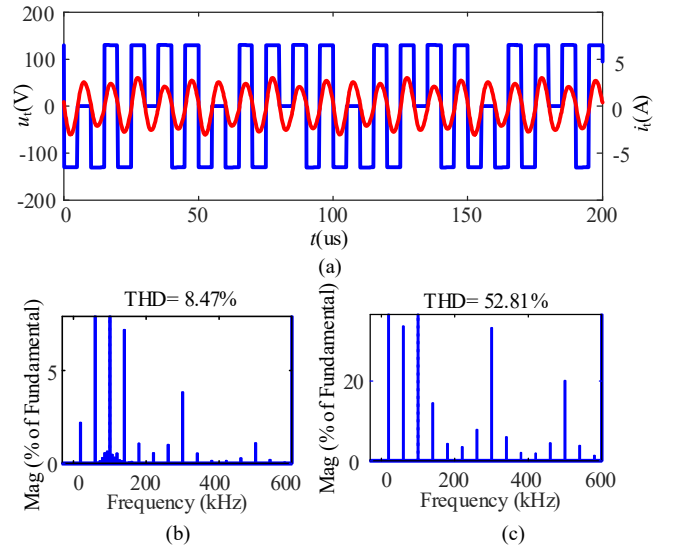


Fig. 10. Waveforms of the PIM WPT system and DFT analysis (a) Transmitter current i_i and inverter voltage u_i (b) DFT of i_i . (c) DFT of u_i .

$$f_h = \left(1 \pm \frac{h}{N_t}\right) (2n-1) f_0, h = 0, 1, 2, \dots, N_t - 1 \quad (11)$$

Due to the fact that a complete control period T_0 includes several resonant cycles, the spectrum of u_t contains both subharmonics and interharmonics. When only considering the subharmonics, the Fourier series expansion of the output voltage u_t can be further derived as:

$$u_t(t) = a_0 + \sum_{n=1}^{\infty} (a_n \cos 2\pi n f t + b_n \sin 2\pi n f t) \quad (12)$$

where

$$a_0 = \frac{1}{N_t T_s} \int_0^{T_{\text{PIM}}} u_t(t) dt = 0 \quad (13)$$

$$a_n = \frac{2}{N_t T_s} \int_0^{T_{\text{PIM}}} u_t(t) \cos 2\pi n f t dt = 0 \quad (14)$$

$$b_n = \frac{2}{N_t T_s} \int_0^{T_{\text{PIM}}} u_t(t) \sin 2\pi n f t dt \quad (15)$$

Furthermore, according to (4), and (12)-(15), it yields:

$$u_{t_{\text{PIM}}} = \delta_{\text{PIM}} \sum_{n=1}^{\infty} \frac{4U_{\text{dc}}}{n\pi} (1 - \cos(n\pi)) \sin n\omega t \quad (16)$$

Similarly, the output voltage of the three-level full-bridge inverter by using the improved SVPFM can be derived as:

$$u_{t_{\text{SVPFM}}} = \delta_{\text{SVPFM}} \sum_{n=1}^{\infty} \frac{4U_{\text{dc}}}{n\pi} (1 - \cos(n\pi)) \sin n\omega t \quad (17)$$

According to (16)-(17), it can be found that both SVPFM and PIM have the same expression, and both the even harmonics of u_t are zero. The difference between SVPFM and PIM is the interharmonics of the output voltage. The magnitude of interharmonics is related to the sequence of the voltage pulse, which is difficult to derive, but the Discrete Fourier transform (DFT) could be applied. Fig. 9 and Fig. 10 show the time-domain waveform of the u_t , i_t , and their DFT analysis. Comparing Fig. 9 and Fig. 10, the THD of the transmit current of the PIM WPT system is much smaller than that of the SVPFM WPT system, caused by the different interharmonics.

B. Capacitor Voltage Balance Analysis

The harmonic current of the three-level full-bridge inverter-based WPT system using the proposed PIM method is small. In the steady state, the voltage of the ab -phase flying capacitor voltage will be balanced at $0.5U_{\text{dc}}$ with one control cycle voltage ripple. The voltage ripple of the ab -phase flying capacitor can be derived as follows [25]:

$$\Delta u_{\text{cx}} \leq \frac{P_r T_s}{C_x U_{\text{dc}}} \quad (18)$$

where P_r is the rated power of the WPT system; x represents a and b , respectively.

C. Dead-Time Effect and ZVS Analysis

The input impedance of the series-series compensated WPT system is inductive while the transmitter capacitor is slightly increased. While the switch state is changed from “0011” to “1100” as shown in Fig. 11(a), i_t lags u_t slightly during the dead time, and the phase difference is α . Supposing that the transmitter current i_t during the dead time is part of the sine

waves, Q_{ZVS} is defined as the integral of i_t during the dead time and can be derived as:

$$Q_{\text{ZVS}} = \int_0^{T_d} i_t dt = \int_0^{T_d} I_t \sin \omega_r t dt = \frac{I_t}{\omega_r} (1 - \cos \alpha) \quad (19)$$

where I_t is the peak value of the transmitter current.

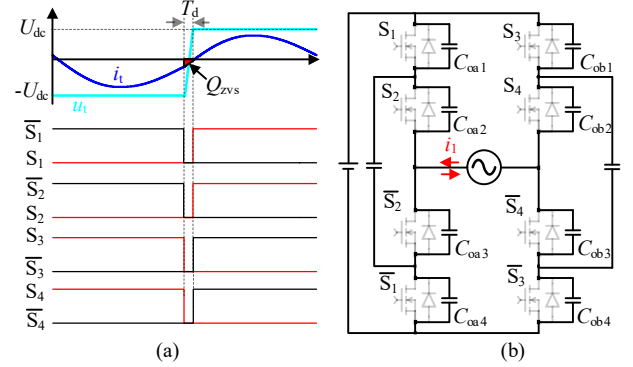


Fig. 11. Operating waveforms of soft switching. (a) Switching state from “0011” to “1100”. (b) Equivalent circuit during dead time.

Based on [27] and Fig. 11(b), the ZVS of the TLFCFBI can be realized when Q_{ZVS} satisfy the following conditions:

$$\begin{cases} |Q_{\text{ZVS}}| \geq \int_0^{0.5U_{\text{dc}}} (C_{\text{oa}1} + C_{\text{oa}2} + C_{\text{oa}3} + C_{\text{oa}4}) \\ |Q_{\text{ZVS}}| \geq \int_0^{0.5U_{\text{dc}}} (C_{\text{ob}1} + C_{\text{ob}2} + C_{\text{ob}3} + C_{\text{ob}4}) \end{cases} \quad (20)$$

It is assumed that all switching output capacitances are the same as C_{oss} . According to (19) and (20), the minimum phase difference α_{min} and dead time T_{dmin} can be derived as follows:

$$\alpha_{\text{min}} = \arccos \left(1 - \frac{2\omega_r C_{\text{oss}} U_{\text{dc}}}{I_t} \right) \quad (21)$$

$$T_{\text{dmin}} = \frac{\alpha_{\text{min}}}{\omega_r} \quad (22)$$

Furthermore, the relationship between the desired increased capacitor (ΔC) and the load condition (R_{eq}) to realize the ZVS can be derived as follows [25]:

$$\frac{\Delta C}{C_r} \geq \frac{1}{m} \sqrt{\frac{16\delta_{\text{PIM}}^2}{\left(4\delta_{\text{PIM}} - \pi\omega_r C_{\text{osst}} \left(R_t + \frac{\omega_r^2 M^2}{R_t + R_{\text{eq}}} \right) \right)^2} - 1} \quad (23)$$

Note that $\Delta C/C_r$ is suggested to be 5% to realize wide-range ZVS during power control [21]. The ZVS of the proposed method is dependent on the transmitter current influenced by the equivalent load R_{eq} and δ_{PIM} . When ΔC and C_{oss} are fixed, a small load and δ_{PIM} might lead to the failure of the ZVS. However, in this situation, the switch is turned on near zero current, thus, the power loss of the PIM will still be smaller than that of the PWM.

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

A. Hardware Implementation

Fig. 12 shows the 1.1 kW prototype of the three-level full-bridge inverter-based WPT system, where the system consists of a DC power source (MR50040), a power analyzer, a silicon

carbide-based three-level flying capacitor full-bridge inverter with integrating drivers and TMS320F28377 board, a WPT circuit, a bridge rectifier, electronic load (PLZ1003WH), a 24V auxiliary voltage source. The transmitter and receiver coils are copper Litz wire. The power analyzer measures the input and output power of the WPT system. The system parameters are listed in Table III.

TABLE III
SYSTEM PARAMETERS OF THE WPT SYSTEM

Items	Value
DC-link voltage (U_{dc})	260 V
Primary (Secondary) capacitance (C_t , C_r)	(8.65, 8.44) nF
Primary (Secondary) coil inductance (L_t , L_r)	(300.0, 303.3) μ H
Primary (Secondary) series resistance (R_t , R_r)	(0.3, 0.3) Ω
Coils diameter (d_1 , d_2)	(30, 30) cm
Distance between two coils (d)	10 cm
Mutual inductance (M)	75.9625 μ H
Resonant frequency (f_r)	100 kHz
Output capacitance (C_o)	220 μ F
Flying capacitance (C_{as} , C_b)	(68, 68) μ F
Load resistance (R_{dc})	55 Ω
Dead time (T_d)	150 ns
Integration coefficient (K)	0.2
Digital signal processor	TMS320F28377
SiC MOSFET	SCT3080
Diode	CVFD20065A

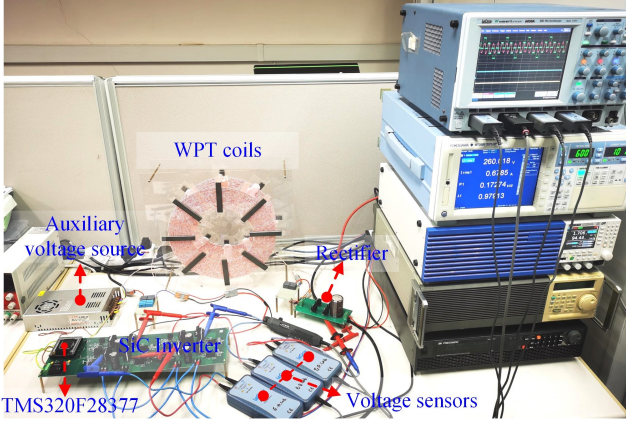


Fig. 12. Experimental platform.

B. Harmonic Analysis of Different Modulation Methods

Fig.13 compares the simulation results of the THD of the transmitter currents of the WPT system by using the proposed PIM, SVPFM, PFM, and EPDM. It can be found that the proposed PIM has the lowest THD for a wide range of δ^* . Furthermore, Fig. 14 shows the waveforms of the inverter output voltage u_t and the transmitter current i_t of the three-level full-bridge inverter-based WPT system by using different modulation methods when $\delta^*=0.4$, including PIM, SVPFM, PFM, and EPDM. It can be seen that the THD of the transmitter current of the proposed PIM is minimal, accounting for only 8.7%.

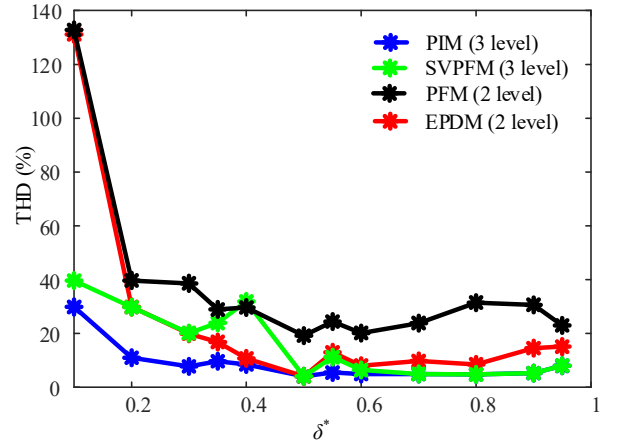


Fig. 13. Simulation results of THD of the transmitter current for different modulation methods.

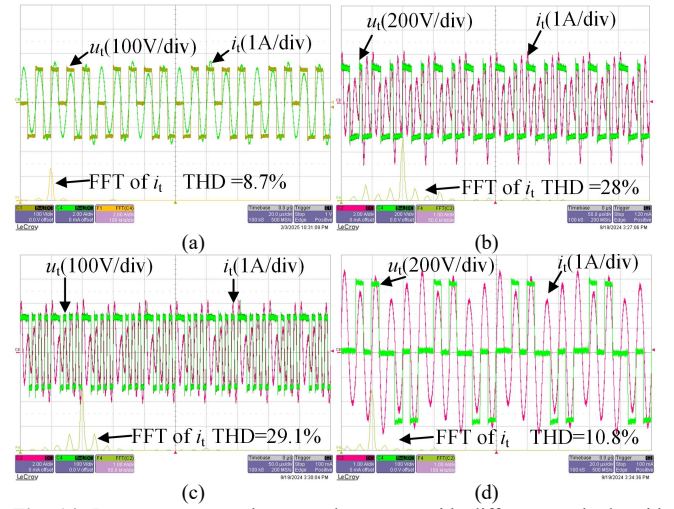


Fig. 14. Inverter output voltages and currents with different methods with $\delta^*=0.4$. (a) PIM. (b) Improved SVPFM. (c) Improved PFM. (d) EPDM.

C. Flying Capacitor Voltage Balance Analysis

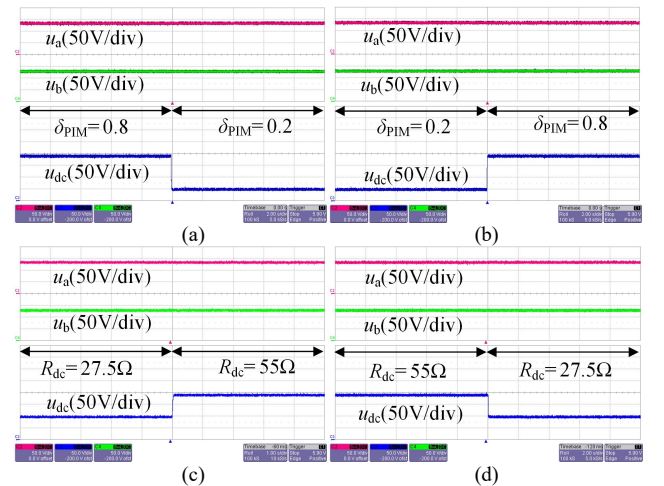


Fig. 15. Output voltage and capacitor voltages for PIM (a) Increasing δ_{PIM} . (b) Decreasing δ_{PIM} . (c) Increasing R_{dc} . (d) Decreasing R_{dc} .

Fig. 15 shows the flying capacitor voltages and output voltage of the WPT system in step responses. As shown in Fig. 15(a) and (b), when δ^* jumps from 0.8 to 0.2 or from 0.2 to 0.8,

the output voltage jumps from 199 V to 49.8 V or 49.8 V to 199 V rapidly, but the flying capacitor voltages (u_a , u_b) have insignificant changes. Similarly, as shown in Fig. 15(c) and (d), while R_l changes from 55 to 27.5 Ω or from 27.5 Ω to 55 Ω , the flying capacitor voltages u_a and u_b have insignificant changes. Both the flying-capacitor voltages are balanced at almost half of the input voltage. The experimental results in Fig. 15 show the effectiveness of the proposed voltage balance method of the three-level full-bridge inverter and its stability under the dynamic response.

D. Impact of Switching-state Selection

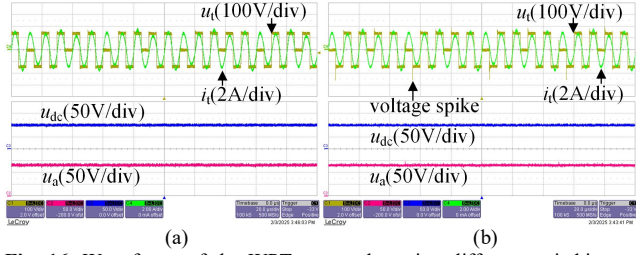


Fig. 16. Waveforms of the WPT system by using different switching state selecting methods. (a) The proposed method. (b) Only changing zero voltage as “1111” in the method of Fig. 8.

Fig. 16 compares the waveforms of the three-level full-bridge inverter-based WPT system by using different switching state selection methods. Fig. 16(a) shows that when the proposed state-selecting method in Fig. 8 is used, there is no voltage spike in the inverter output voltage. By comparison, when the switching state of the zero voltage in Fig. 8 is changed to “1111”, the voltage spikes appear in u_t , leading to the voltage spikes of the output voltage and deterioration of system characteristics, as shown in Fig. 16(b).

E. ZVS, Power Loss and System Efficiency Analysis

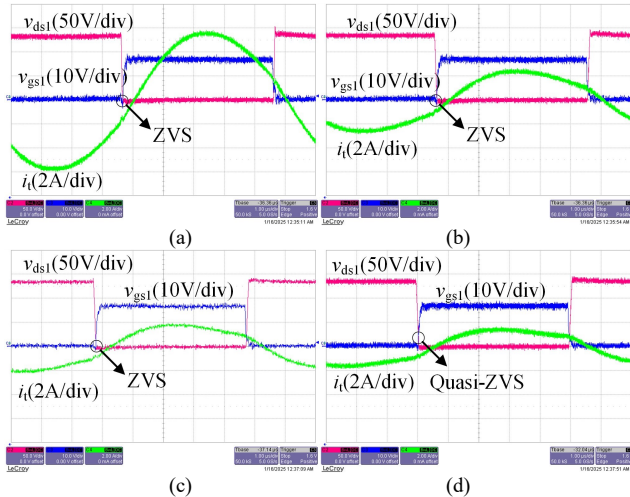


Fig. 17. Experimental waves of the WPT system when $\delta_{PIM}^* = 0.8$ (a) 100% load. (b) 40% load. (c) 30% load. (d) 20% load.

Fig. 17 shows the switching waveforms of the PIM-WPT system while $\delta_{PIM} = 0.8$, where v_{ds1} and v_{gs1} are the drain-source voltage and gate-source voltage of the switch S_1 , respectively. Fig. 17 (a)-(c) shows that v_{gs1} becomes a high-level voltage after v_{ds1} becomes zero, indicating that S_1 can realize reliable ZVS for the PIM-WPT system while changing the load from 100% to 30%. The realization of the ZVS relies on loads.

When the load is decreased, the transmitter current is gradually decreased. Fig. 17(d) shows that when the 20% load is added, the magnitude of the time-domain resonant current becomes small, and ZVS cannot be completely realized. But the MOSFET switches on at the time when the v_{ds1} and i_t are close to zero, thus the power loss is still obviously decreased compared with the hard switching of the PSC WPT system.

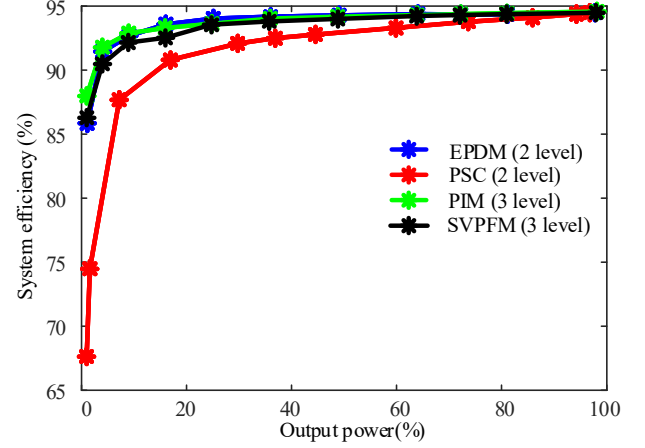


Fig. 18. System efficiency of the WPT system with different methods by only changing δ_{SVPFM}^* or δ_{PIM}^* .

The system efficiency is calculated by dividing the measured output and input power of WT5000, and the power consumption of the auxiliary power supply is 4.3W. The ratio of the auxiliary power supply decreases when output power increases, which is not considered in the calculation of the system efficiency. Fig. 18 compares the system efficiency of the TLFCFBI-based WPT system with different output power by changing the δ^* of different modulation methods. All the modulation methods have the same maximum efficiency of 94.6% for achieving ZVS under the full load while $\delta^* = 1$. Considering the PIM, SVPFM, and EPDM can realize wide-range ZVS, their efficiencies are similar and much bigger than that of PSC even under light load conditions. Besides, the efficiency of PIM is similar to that of EPDM, and the efficiency of PIM is slightly higher than that of the SVPFM when δ^* ranges from [0, 0.5] caused by harmonic currents.

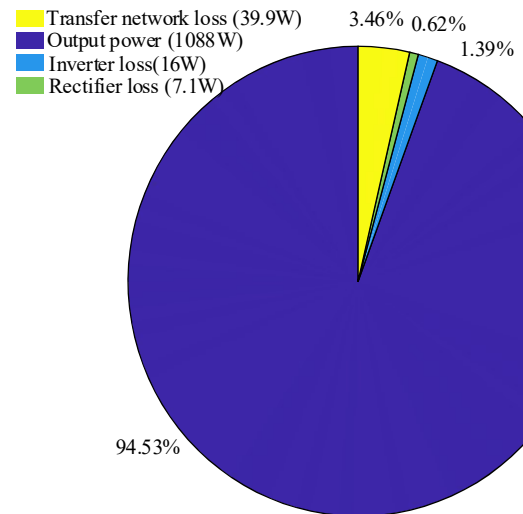


Fig. 19. Output power and power losses when $\delta_{PIM}^* = 0.99$.

Furthermore, the input power, output power, inverter output power, and input power of the diode rectifier are measured by the WT5000. Then, the percentage of loss components with respect to the input power can be calculated. Fig. 19 shows the output power and power loss distribution of the TLFCFBI-based WPT system by using PIM when $\delta_{PIM}^* = 0.99$, where the input power is 1151 W. The transfer network loss accounts for 3.46%, which is maximal. The power loss of the TLFCFBI accounts for 1.39%, and the power loss of the diode rectifier accounts for 0.62%.

F. Closed-loop Control and Misalignment Analysis

Furthermore, the output voltage closed-loop experiments are carried out to verify the proposed PIM method. The PI controller is used to regulate the output voltage of the diode rectifier, and the output of the PI controller is the input of the PIM δ_{PIM}^* . Fig. 20 shows the input voltage step and load step responses and their zoom-in waveforms of the PIM WPT system using PI closed-loop control. When the load changes from 55Ω to 27.5Ω or from 27.5Ω to 55Ω , the flying-capacitor voltages have insignificant changes, the DC-side output voltage fluctuates and is quickly adjusted to 100 V, and ZVS is realized after the step response, as shown in Fig. 20(a) and (b). When the input voltage changes from 260 V to 130 V or from 130 V to 260 V, the DC-side output voltage fluctuates and is quickly adjusted to 100 V, the flying-capacitor voltages change as half of the input voltage quickly, and ZVS is realized after the step response, as shown in Fig. 20(c) and (d). Fig. 20 further verifies the effectiveness of the PIM and capacitor voltage balancing method under the closed-loop conditions.

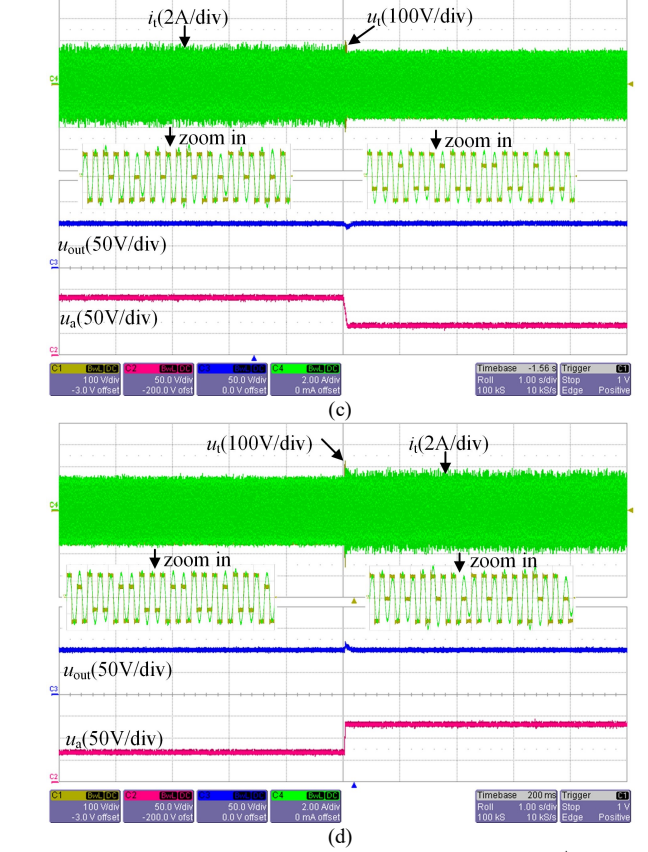
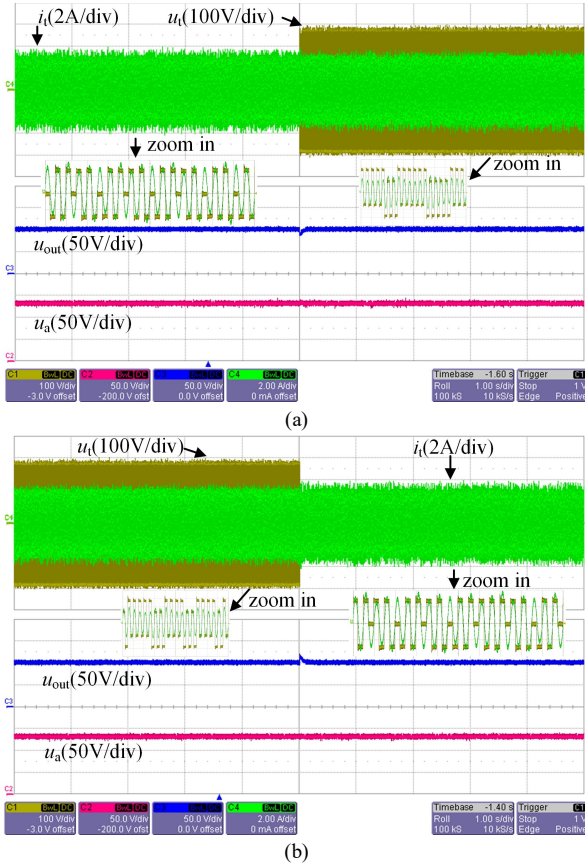


Fig. 20. Step responses of the PIM WPT system when $U_{out}^* = 100V$. (a) decreasing R_L . (b) increasing R_L . (c) decreasing U_{in} . (d) Increasing U_{in} .

Fig. 21 shows the efficiency curve of the WPT system under the voltage closed-loop control with misalignment, where Δl refers to the horizontal offset distance between the centers of the transmitter and receiver coils. The system efficiency is gradually decreased from 93.0% to 87.2 % when $V_{out}^* = 100V$ and Δl is increased from 0 to 10 cm.

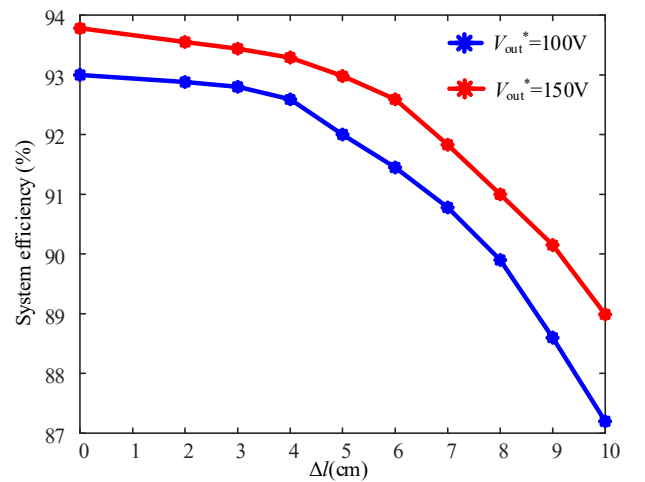


Fig. 21. Misalignment analysis.

Meantime, Fig. 22 shows the output voltage and current of the TLFCFBI for the WPT system with misalignment. To keep the output voltage constant at 100 V, δ_{PIM}^* is decreased from [0.38, 0.415] to [0.249, 0.266] for 10 cm misalignment,

as shown in Fig. 22(a) and (b). Similarly, the system efficiency is gradually decreased from 93.8% to 89.0% when $V_{out}^*=150V$ and Δl is increased from 0 to 10 cm. To keep the output voltage constant at 150 V, δ_{PIM}^* is decreased from [0.58, 0.615] to [0.371, 0.415] for 10 cm misalignment, as shown in Fig. 22(c) and (d). This work does not focus on the misalignment case so it is not evaluated in detail.

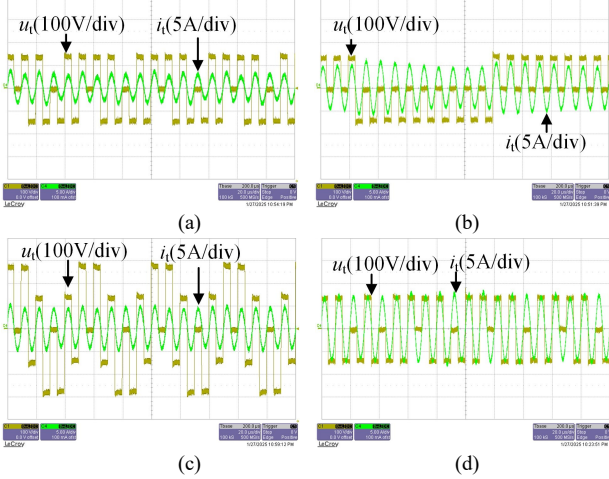


Fig. 22. Voltage and current of the TLFCFBI with misalignment (a) $\Delta l=0$, $u_{out}^*=100$ V. (b) $\Delta l=10$ cm, $u_{out}^*=100$ V. (c) $\Delta l=0$, $u_{out}^*=150$ V. (d) $\Delta l=10$ cm, $u_{out}^*=150$ V.

V. DISCUSSION

The proposed PIM is not only valid for the SS compensation method. However, whether it can be applied to any compensation method needs to be further investigated in the future. Many higher-order compensation topologies can be used for the WPT system. Whether the PIM is applicable depends on the filter characteristics of the higher-order compensation topologies. The output voltage of the TLFCFBI-based WPT system using the PIM still contains interharmonics. If the higher-order compensation topology amplifies these interharmonics and causes ZVS failure, the PIM will not be suitable for this topology. On the contrary, if the higher-order compensation topology can suppress these interharmonics and ensure ZVS, PIM will be suitable for this topology.

VI. CONCLUSIONS

This paper proposed and implemented a PIM method of a three-level full-bridge inverter for WPT. Some conclusions are summarized as follows:

1) This paper proposed the delta-sigma PIM of three-level full-bridge inverters for WPT systems. The proposed method can be extended to the multilevel full-bridge inverter-based WPT system. The PIM has the significant advantage of low harmonics, wide-range ZVS, and realizing easily.

2) Besides, the capacitor voltage balancing and switching state selecting method of the fly-capacitor three-level full-bridge inverter for the WPT system is proposed. The method can balance the flying-capacitor voltages as half of the input voltage, and eliminate the voltage spike of the voltage pulse. Finally, experimental verification is given to verify the feasibility of the proposed modulation method.

VII. APPENDIX

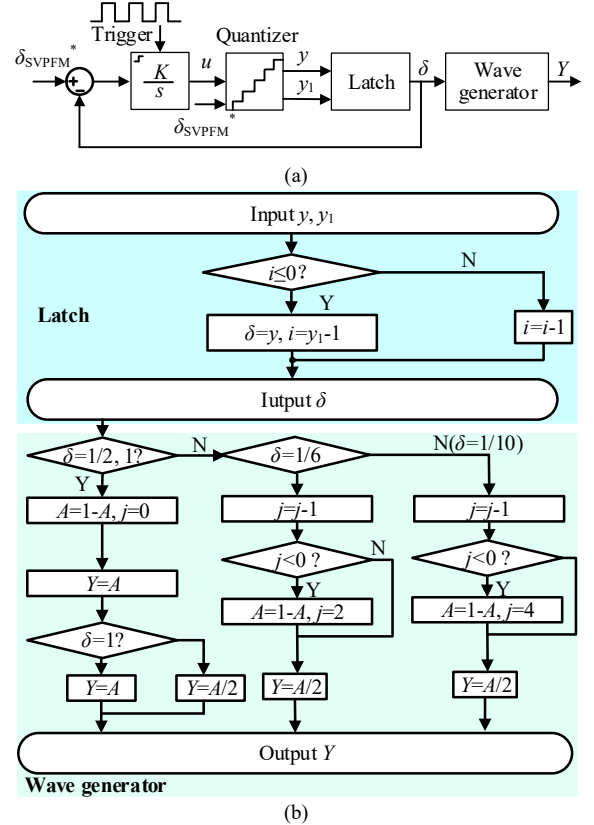


Fig. 23. The modified SVPFM for the FCTLCFBI.

Our previous work has proposed an SVPFM method for the three-level half-bridge inverter [25]. Based on [25], the SVPFM is modified for the three-level full-bridge inverter in this appendix for comparison, as shown in Fig. 23. The quantizer shown in Fig. 23(a) is given as follows:

$$y = \begin{cases} 1, & 0.75 < u \leq 1 \\ 0.5, & 1/3 < u \leq 0.75 \\ \frac{1}{4n+2}, & \frac{n+1}{(2n+1)(2n+3)} < u \leq \frac{n}{(2n-1)(2n+1)} \end{cases} \quad (24)$$

where $n \in \mathbb{Z}^+$.

$$y_1 = \begin{cases} 1, & y = 1 \\ \frac{1}{2y}, & y \neq 1 \end{cases} \quad (25)$$

Fig. 23(b) shows the way of Latch and the wave generator in detail while y is only selected as 1, 1/2, 1/6, and 1/10, and then δ_{SVPFM} only ranges in [1/10, 1] in this situation.

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