van der Waals interface between high-*k* dielectrics and 2D semiconductors

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ABSTRACT

Atomically thin two-dimensional (2D) semiconductors are attractive channel materials for next-generation field-effect transistors (FETs). The high-performance 2D electronics requires high-quality integration of high-*k* dielectrics, which however remains a significant challenge. In this mini-review, we provide a brief introduction on recent progress in the van der Waals (vdW) integration of high-*k* dielectrics onto 2D semiconductors. We first highlight the importance of high-*k* dielectric integration for 2D FETs. Next, we summarize the recent breakthroughs in the various vdW integrations of high-*k* dielectrics with 2D semiconductors, along with their interfaces' properties. Additionally, we examine the quasi-vdW integration of conventional high-*k* dielectrics onto 2D semiconductors. Finally, we discuss the challenges and potential future research directions in this field.

Keywords: Two-dimensional semiconductor, high-*k* dielectrics, van der Waals interface

1 Introduction

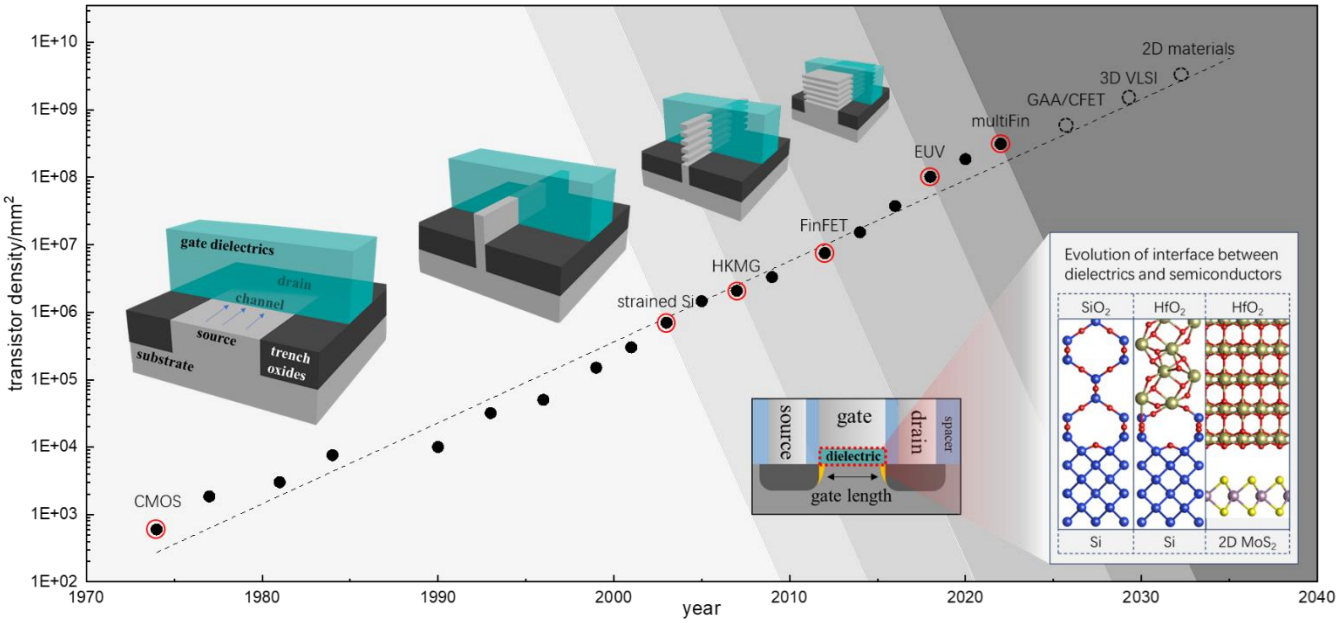

Figure 1. Trends in transistor miniaturization over time. The main technology nodes of transistor are shown with time evolution. Four geometries of transistors are depicted with size scaling. The inset shows representative semiconductor-insulator interfaces.

Silicon-based electronics form the backbone of modern society's technological infrastructure, which have been widely used in many aspects ranging from digital computing, automotive and transportation to health care. In the past few decades, Moore's law and Dennard's law pave the way for the transistor industry to improve the performance of devices by downscaling, which takes us to the 3-nm-node era in 2022 (figure 1). However, after Si dominating market for over decades, it hits a bottleneck for further miniaturizing due to pronounced short-channel effects, difficulties in the deposition of ultra-flat Si film at atomic scale, and the significantly reduced carrier mobility [1–3].

Several key techniques have been used in industry for continuing scaling Si-based devices, as illustrated in figure 1, such as the introduction of strain-Si channel in 90-nm node, the use of high-*k* dielectrics and metal gate (HKMG) into 45-nm node, the Fin structure used in 22-nm node, and the EUV technology in 7-nm node. Topology optimization is one of the most efficient ways to scaling (figure 1), but the approaching physical limits also force us to re-evaluate the interfacial compositions as well [4–6]. For the semiconductor part, strained-Si, strained-SiGe, SiGe, high-mobility Ge and III-V are considered as alternatives to control the unaffordable high-power consumption, low switching speed and high leakage current [7–13]. However, a solution

better than present SiGe is needed to fix the large parasitic capacitance, instability of high-aspect-ratio Fins, difficulties in device epitaxy under 10-nm physical gate length. With the intrinsic atomic thicknesses and atomically flat surfaces, 2D semiconductor materials are one of the best candidates to sub-1-nm node and beyond [14–20]. Among them, transitional metal dichalcogenides (TMD) with prominent electronic properties have been identified as the most promising 2D semiconductors, especially the 2D molybdenum disulfide (MoS_2) since first monolayer TMD-FET was reported in 2011 [21–26].

On the other hand, the inevitable use of high-*k* dielectrics helps to improve the gate control and electrostatics, to reduce short-channel effect, to lower operating voltage and to suppress remote phonon scattering. Although it is efficient and evidenced by the 45-nm process, directly integrating the high-*k* dielectrics like commonly used HfO_2 on 2D semiconductors remains challenging. That is mainly due to: (1) 2D semiconductors, unlike traditional bulk ones, lack dangling bonds at their surfaces. However, surface dangling bonds at the substrate are needed as nucleation centers for high-quality integration; (2) When the high-*k* dielectrics with dangling bonds interface with the dangling-bond-free 2D semiconductors, high density of interfacial states always occur. The high interface state density is detrimental to the electronic device performance. In a word, building an ideal interface of high-*k* dielectrics on 2D semiconductors is recently a leading scheme for the development of high-performance 2D FETs [14,15]. Some of the important criteria for device design are summarized in Table 1.

Table 1 The main figures of merit in FETs.

Figure of merit	Unit	Reference
Equivalent oxide thickness (EOT)	unit	1.00 [14]
Subthreshold swing (SS)	mV/dec	82(HP), 75(HD) [14]
Interface state density (D_{it})	$cm^{-2}\ eV^{-1}$	~1.0×10^{10} (Si/SiO_2) [27]
Field-effect mobility	$cm^2\ V^{-1}\ s^{-1}$	125 [14]
On/off ratio	unit	8.74×10^4 (HP), 6.44×10^6(HD) [14]
Band alignment	eV	CBO > 1 eV, VBO > 1 eV [28]
Gate length	nm	16(HP), 18(HD) [14]
Leakage current	A/cm^2	$1A/cm^2$ at ~1V [28]

Hysteresis	mV/(MV/cm)	0.8(SOI) [29]
Transconductance	μS/μm	1605 [14]
Saturation voltage	V	0.092(HP), 0.104(HD) [14]
Spacer *k* value	unit	3.2 [14]

Extensive efforts have been made to improve the integration of high-*k* dielectrics onto 2D semiconductors [30–38]. Early attempts have mainly focused on activation of 2D semiconductor surfaces to increase the number of nucleation sites for the deposition of high-*k* dielectrics [39–56]. Consequently, interface engineering strategies have also been proposed, in which buffer layers or seeding layers have been used in between high-*k* dielectrics and 2D semiconductors [39–45]. While these methods could improve the deposition quality of high-*k* dielectrics, they inevitably lead to damage to the delicate 2D structures, thus the overall device performance may not be improved. Recently, vdW integration has been developed for the high-performance integration of high-*k* dielectrics onto 2D semiconductors [57–93]. The vdW integration started from the use of the layered 2D insulator such as hexagonal boron nitride (*h*-BN), which can naturally result in ideal interface with layered 2D semiconductors with minimized interface state density [94–98]. Consequently, we have seen the development of various other vdW interfaces formed by vdW integrating higher-*k* dielectrics onto 2D semiconductors, some of which not only show high-performance interface properties, but also demonstrate the direct integration capability [78–93,99–105]. Thus, forming vdW interfaces has shown great potential for advanced 2D electronics. While we are aware that various excellent reviews have been made [106–119], a mini-review remains desired, specifically for the vdW integration of high-*k* dielectrics on 2D semiconductors, due to the rapid development of this filed.

In this regard, we present a mini-review of recent process of vdW interfaces between high-*k* dielectrics and 2D semiconductors. We first introduce the experiment methods for vdW integration of high-*k* dielectrics on 2D semiconductors. Then, we highlight recent important advancements of the vdW and quasi-vdW integrations of high-*k* dielectrics. Finally, we briefly discuss the challenges, limitation and opportunities of vdW integration of high-*k* dielectrics for 2D electronics.

2 vdW integration methods

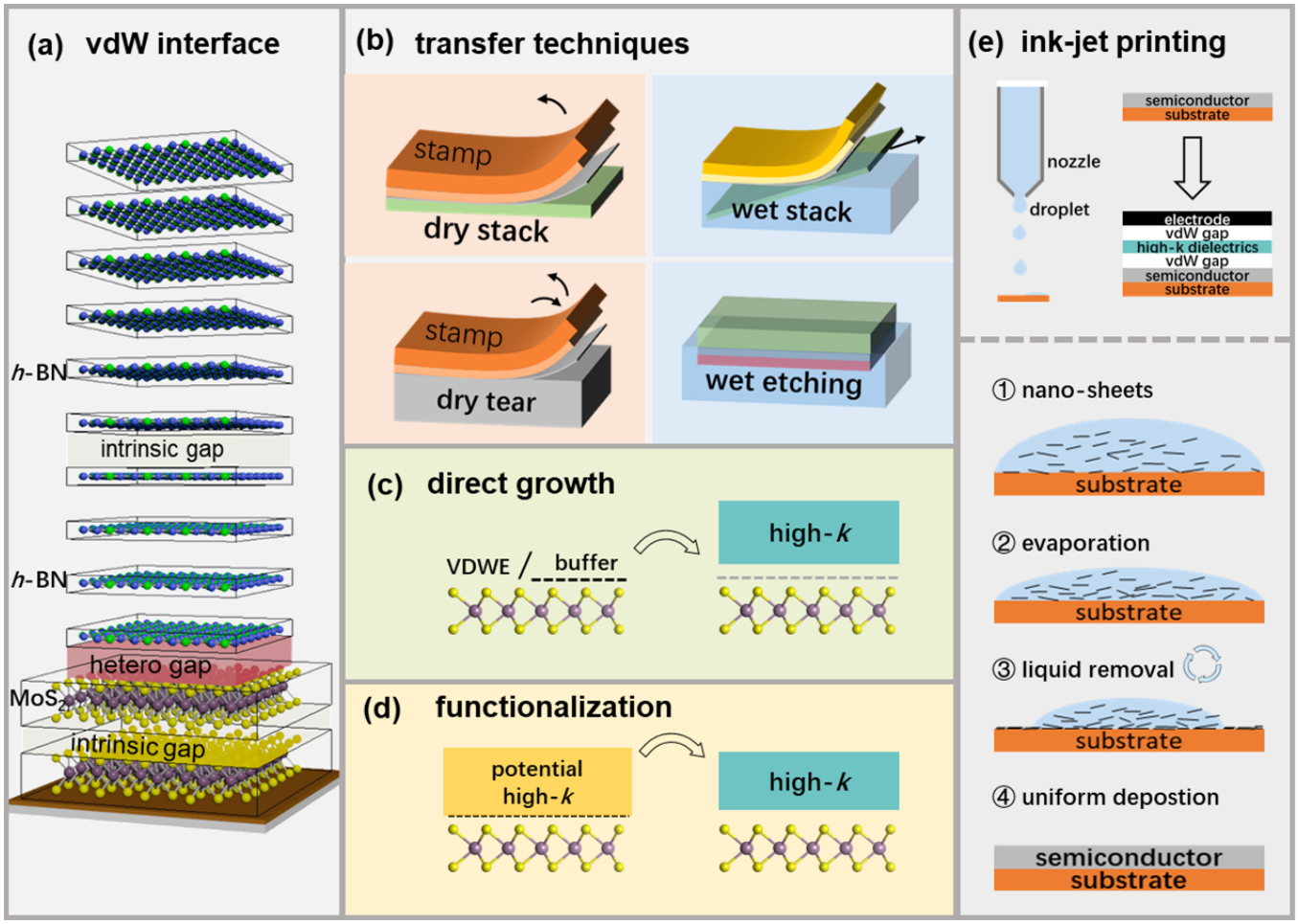

Figure 2. Schematic of integration methods for vdW interfaces. (a) A typical vdW interface formed by multilayer *h*-BN and monolayer MoS_2. (b) Top-down transfer methods. (c)-(d) Bottom-up methods. (e) Ink-jet method diagram.

The vdW interaction consists of various dipole-dipole like interaction within materials or at the interface of heterostructures, the strength of which is several-order weaker than that of covalent bonds or ionic bonds [120]. The formation of vdW interface between high-*k* dielectrics and 2D semiconductors is highly desired as it can bring minimized damage to the 2D semiconductors. Therefore, various methods have been developed for the vdW integration of high-*k* dielectrics onto 2D semiconductors, which include top-down transfer-based integration and bottom-up direct growth as detailed below.

The top-down methods have been prevailing in years as they circumvent the possible direct damage or inconsistent fabrication conditions of each interface side [121–128]. Naturally, the hallmark of the top-down methods is the prefabricated samples, which then will be transferred

onto 2D semiconductors. The most used transfer techniques consist of two main steps: detaching and stacking. Depending on whether a dry or wet environment is employed, different approaches can be devised, as illustrated in figures 2(b). Originally, dry detaching, or mechanical exfoliation, opens the path for detaching 2D materials. Later, wet detaching becomes popular because chemical etching of growth substrates like SiO_2 enables the preparation of floating 'free-standing' 2D layered materials by solution. Subsequently, the development of a modification to replace the etchant with water has been developed to remove etchant contamination, also known as 'water-assisted transfer'. From the physical perspective, detaching and stacking are the processes by using the different adhesion stress between the stamp materials and the substrates. Detaching is the process where the adhesion between the 2D material and the stamp is stronger than the interlayer forces within the 2D material. In constrast, the stacking process operates in the opposite way. As a result, by leveraging disparities in solubility, hydrophilic and hydrophobic properties, viscosity variations at different temperatures, and differences in interlayer forces, one can utilize the transfer technique to obtain high-quality vdW interfaces.

For bottom-up methods, the dielectric thin films can be directly synthesized on the top of 2D semiconductors. They avoid the transfer processes, thus are highly desired for large-scale integration and compatible with current semiconductor technologies. Conventional deposition methods such as sputtering or atomic layer deposition (ALD) require high-density of nucleation sites for the high-quality deposition of high-*k* dielectric films [129–132]. To improve the deposition of high-k dielectrics, nucleation sites are required to be introduce into inert 2D semiconductor surfaces, which however leads to damage to 2D structures and thus deteriorates their electronic properties. To mitigate these issues, various improvements have been made to either the deposition process or the choice of materials, as illustrated in figures 2(c)-(d). The main idea in figure 2(c) is to enable the direct growth of high-*k* dielectrics on the 2D semiconductors or on the auxiliary buffer layer. The direct growth requires a strict selection of materials to make sure that the vdW interaction can dominate [120,133–135]. Compared to conventional buffer layer materials, new buffer layers are made of atomically sharp surfaces, which can not only facilitate the deposition of high-*k* dielectrics, but also minimize the damage to 2D channels [80,92,136–138]. More recently, low-temperature evaporation has been used to deposit novel high-*k* dielectric materials such as inorganic molecule crystals (IMCs) onto 2D semiconductors directly. The low-temperature evaporation process ensures the reduced damage

to 2D lattice structures, and more importantly the resulting interface is vdW-like due to dangling-bond-free surface of IMCs [80]. Consequent study shows that the IMCs can also serve as both seeding and buffer layers to further deposit conventional high-*k* dielectric HfO_2, which further improves the device performance [92].

Another effective way to realize high-performance integration of high-*k* dielectrics into 2D semiconductors is through the functionalization of deposited intermediate structures, as illustrated in figure 2(d). One of the common situations is to form vdW-type overlayer on the 2D semiconductors first, and then the overlayer will be converted into dielectric materials through the functional treatment such as oxidation. Practical systems contain but not limit to the HfX_2/HfO_2 [81–84,104,139], Bi_2SeO_2/Bi_2SeO_5 [78,79] and ZrX_2/ZrO_2 [101–104] interface. In addition, printing methods have been developed as a combination of bottom-up and top-down methods, such as ink-jet printing (see in figure 2(e)) and liquid metal printing [85–90,99,100], where the high-quality interfaces can also be realized.

3 vdW interfaces between high-*k* dielectrics and 2D semiconductors

As discussed above, recent developments on the vdW integration of high-*k* dielectrics have resulted in much-improved device performance of 2D electronics. In this section, we summarize recent advancements in the vdW and quasi-vdW interfaces between high-*k* dielectrics and 2D semiconductors, in which interfaces involving two naturally layered 2D structures are considered as the prototypical vdW interfaces, while those formed by non-layered high-*k* dielectrics on 2D semiconductors are categorized as quasi-vdW interfaces.

3.1 vdW interfaces using top-down method

The vdW interfaces between layered 2D dielectrics and layered 2D semiconductors are commonly using top-down method, in which the pre-fabricated 2D dielectrics are transferred onto 2D semiconductors [57–67]. An example of top-down vdW integration is the use of *h*-BN as the dielectric and MoS_2 as the channel material [62] (see figure 3(a)). Owing to the stability and dangling-bond-free *h*-BN, the resulting devices exhibit excellent interfacial properties. Specifically, the device as shown in figure 3(b) achieves an ultra-low interface density of ~ 5.2×

10^9 cm^{-2} eV^{-1} and hysteresis as low as 0.15% of the sweeping range of bias. Such a low interface state density indicates the high interface quality. Further study has suggested that the interface properties can be improved by post-thermal annealing, as shown in figure 3(c)-(d). Concurrently, a high on/off ratio of 10^8 and low subthreshold swing (SS) values ranging from 63 to 69 mV/decade have been realized in *h*-BN/MoS_2 based devices at an operating voltage of 1 V. However, the challenges to *h*-BN-based MOSFET have been widely discussed. Compared to other high-*k* dielectrics like HfO_2 or SiO_2, the main drawback of *h*-BN is its low dielectric constant (~3.5), consequently higher leakage current under same thickness. Besides, it remains challenging to realize high-quality and large-scale growth of layered *h*-BN films [63].

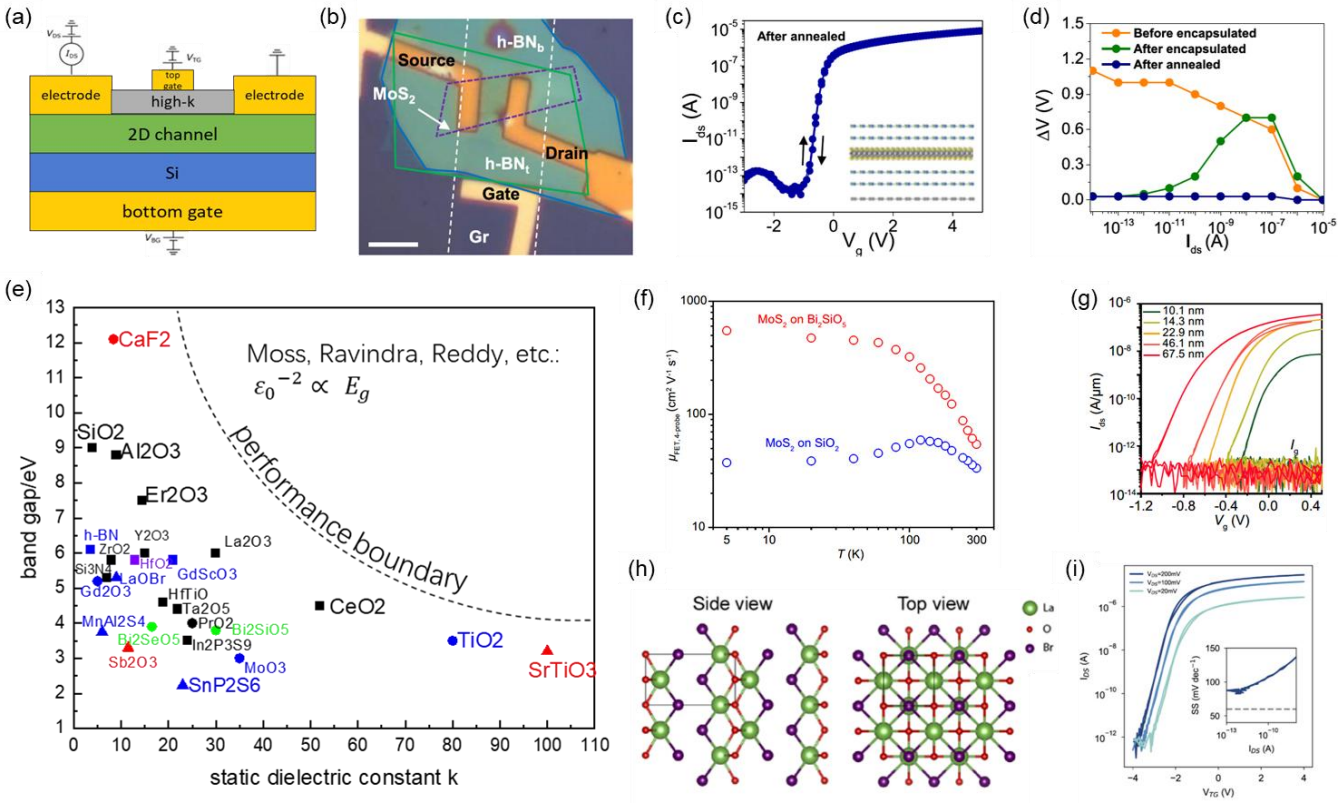

Figure 3. Typical vdW interfaces prepared by top-down method. (a) Schematic of double-gate transistor. (b)-(d) Optical image, transfer curve and comparison of hysteresis of *h*-BN/MoS_2 device. Reproduced with permission from Ref. [59]. (e) The statistics of traditional and novel dielectric materials regarding static dielectric constant and band gap. (f) The temperature-dependent FET mobility of MoS_2 on Bi_2SiO_5 and on SiO_2. (g) Transfer curve of Bi_2SiO_5/MoS_2 varying thickness of Bi_2SiO_5. Reproduced with permission from Ref. [61]. (h) Structure of LaOBr structures from high-throughput screening. Reproduced with permission from Ref. [62]. (i) Transfer curve of LaOBr/MoS_2 FET. Reproduced with permission from Ref. [64].

Consequently, various gate dielectrics with high dielectric constant have been integrated into 2D MoS_2 electronics to form vdW interface using the top-down method, as shown in figure 3(e). Among them, a high carrier mobility (549.3 cm^2 V^{-1} s^{-1} at 5K) has been achieved in $Bi_2Si_2O_5$/MoS_2

[64], which is about 15 times higher than SiO_2 counterpart, as shown in figure 3(f). Due to its high dielectric constant (>30), $Bi_2Si_2O_5/MoS_2$ based device shows a low EOT down to 1.3 nm when thickness of $Bi_2Si_2O_5$ is decreased to 10.1 nm, as shown in figure 3(g). The promising device performances (SS < 70 mV/dec and hysteresis ~ 3 mV) suggest the high-performance interface of $Bi_2Si_2O_5/MoS_2$. However, relatively small band gap and large unit cell thickness may limit the performance in further scaling or other power transistor applications, meanwhile the large-scale synthesis and uniform growth of $Bi_2Si_2O_5$ thin films also deserve further studies.

In addition, high-throughput first-principal calculation has been employed to accelerate the prediction of high-performance layered 2D high-*k* dielectrics in experiments [65–67]. For examples, using large-scale first-principles calculations, LaOBr has been identified as one of the most promising dielectrics screened from 457 layered materials for its proper electronic gap, high dielectric constant and low leakage current density (see figure 3(h)) [65]. This prediction has been verified by consequent experiment, in which LaOBr thin film has been synthesized and transferred onto MoS_2 [67]. Furthermore, the associated transfer characteristics in figure 3(i) show that $LaOBr/MoS_2$ device exhibits decent mobility of 32 $cm^2\ V^{-1}\ s^{-1}$, low SS of 85 mV/dec, low interface state density of $1\times10^{12}\ cm^{-2}\ eV^{-1}$ and high on/off ratio of 10^8. These promising results confirm the contribution of high-throughput calculation to accelerate the discovery of high-performance high-*k* dielectrics for advanced 2D electronics.

3.2 Quasi-vdW interfaces using top-down method

Recently, the high-performance interface between high-*k* dielectrics and 2D semiconductors have been further exploited, enabling a vdW-type integration of those non-layered materials as the high-*k* dielectrics using the top-down method, noted as quasi-vdW interfaces. Compared to vdW interfaces, their advantage lies in the availability of a wider range of high-*k* materials, thereby significantly expanding the possible combinations of 2D semiconductors/high-*k* dielectrics interfaces.

Early quasi-vdW interface has been realized by transferring F-terminated $CaF_2(111)$ onto MoS_2 [73], as illustrated in the figure 4(a). High-*k* dielectrics $CaF_2(111)$ (k~8.43) is intriguing for its naturally saturated surface, which leads to a dangling-bond free surface, in contrast with its (001) surface with dangling bonds. Thus, a high quality quasi-vdW interface can be formed, as

observed in the high-resolution TEM image (figure 4(b)), in which the thickness of the CaF_2 sample can be thinned to 2 nm. The on/off ratio of CaF_2/MoS_2 device is high to 10^7, and its leakage current is low to 10^{-7} μA. As shown in figure 4(c), the sub-1-nm EOT interface can be realized using CaF_2 as the gate dielectric, with excellent electrical stability, small hysteresis window, and high breakdown field.

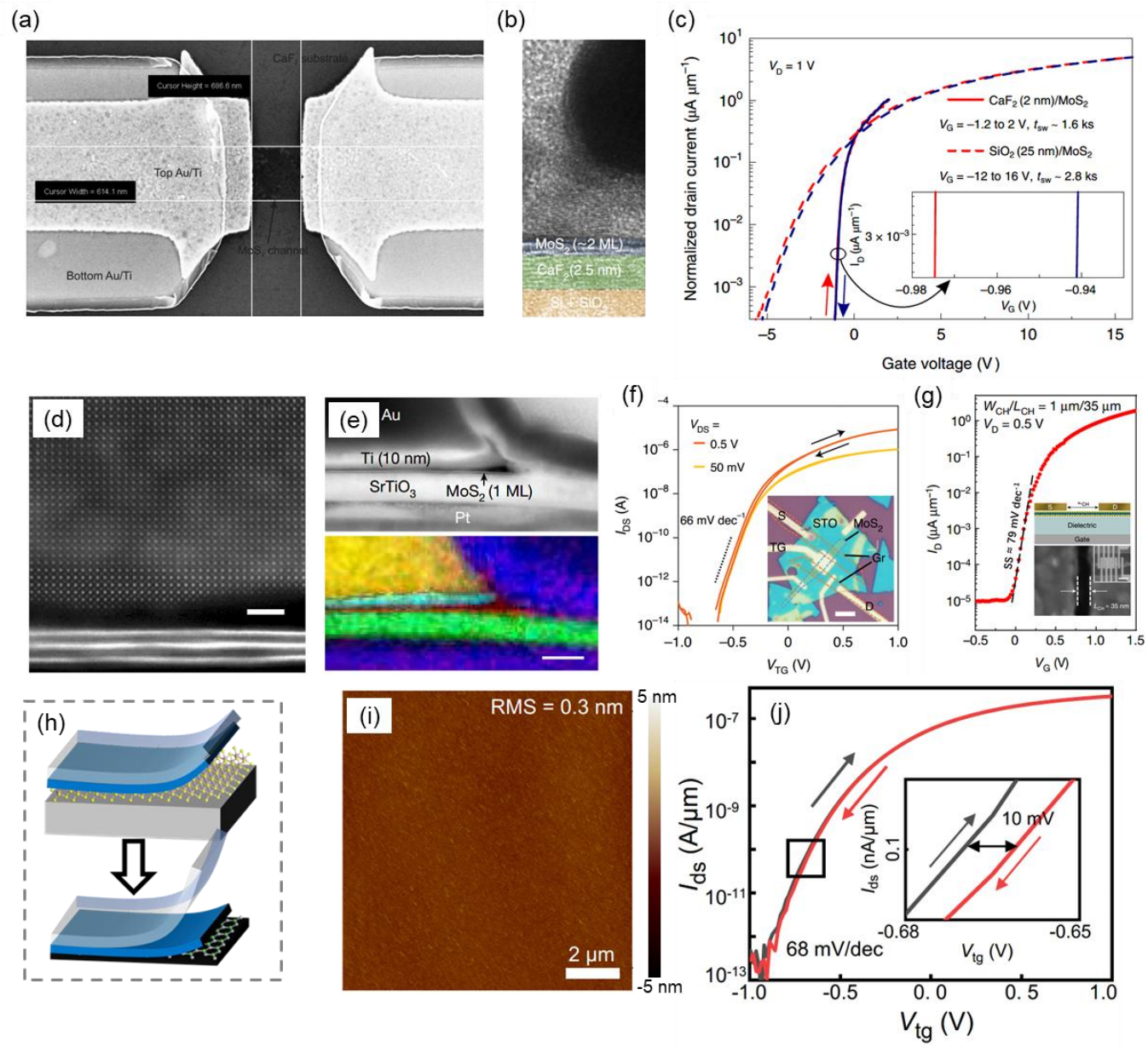

Figure 4. Quasi-vdW interfaces prepared by top-down method. (a)-(c) SEM image and normalized transfer curve of CaF_2/MoS_2 interface. Reproduced with permission from Ref. [70]. (e)–(g) STEM image, optical image and corresponding I_D-V_G characterization of two separate research of STO/MoS_2 system. Reproduced with permission from Ref. [70, 71]. (h) Main steps of fabricating quasi-vdW interface assisted by 2D surface. (i)-(j) AFM height measurement and double-sweep transfer curve of a wafer-scale transferred sample Al_2O_3 and a top-gated MoS_2 FET made from wafer-scale Al_2O_3/MoS_2. Reproduced with permission from Ref. [73].

Gate dielectrics with higher dielectric constant such as Ta_2O_5 and perovskite oxide $SrTiO_3$ (STO) have also been employed to achieve quasi-vdW interface with 2D semiconductor MoS_2 [69,75]. Especially, STO is a highly desired high-*k* dielectric material for 2D semiconductors, due to its ultra-high dielectric constant (~300). Recently, high-performance quasi-vdW interface has been realized by transferring pre-fabricated STO thin film on 2D MoS_2, as shown in STEM images and EDS mapping in figure 4(d) and (e), respectively. The STO/MoS_2 based top-gate devices can reach an attractive electrical performance with SS of 66 mV/dec, on/off ratio of 10^8, off-state current of 1×10^{-13} A, and negligible hysteresis, as shown in figure 4(f). Furthermore, a short-channel device with channel length down to 25-55 nm has been demonstrated in STO/MoS_2, as show in the figure 4(g). Similarly, high-*k* dielectric Ta_2O_5 (*k*~15.5) has also been employ to form high-performance quasi-vdW interface with MoS_2, with high mobility of 60 $cm^2 V^{-1} s^{-1}$ and a SS near the Boltzmann's limit [71].

Besides, traditional high-*k* oxides such as Al_2O_3 and HfO_2 have also been transferred on MoS_2 as the gate dielectrics. In this process, an atomically sharp sacrificial layer is used for a wafer-scale transfer, as illustrated in figure 4(h) [68,70,72,74]. Using graphene and WSe_2 as the sacrificial layer, it is shown that the direct-ALD sample is vdW-type. In figure 4(i), a flat and wafer-scale Al_2O_3 has been fabricated, assisted by sacrificial PVA (polyvinyl alcohol) [76]. The high-*k* film was then transferred onto MoS_2 for 2D device. As shown in figure 4(j), the MoS_2 device using the transferred HfO_2 as the gate dielectric shows low SS (68 mV/dec) and operation voltage (0.5 V), high on/off ratio of 10^7), and small hysteresis window (~10 meV). Besides, the device performance of high-*k*/MoS_2 can be further improved by inserting buffer layers such as *h*-BN in between high-*k* dielectrics and MoS_2, where the dangling bond effect from the dielectrics can be reduced [140–144].

3.3 vdW interfaces by bottom-up methods

The top-down methods discussed above can lead to high-performance integration of high-*k* dielectrics in 2D electronics. However, the process is dependent on the transfer technique, which not only increases the integration complexity, but also presents a grand challenge to large-scale practical applications. In this context, the bottom-up methods that are capable of directly

depositing high-*k* dielectrics onto 2D semiconductors are highly desirable. Previously, direct

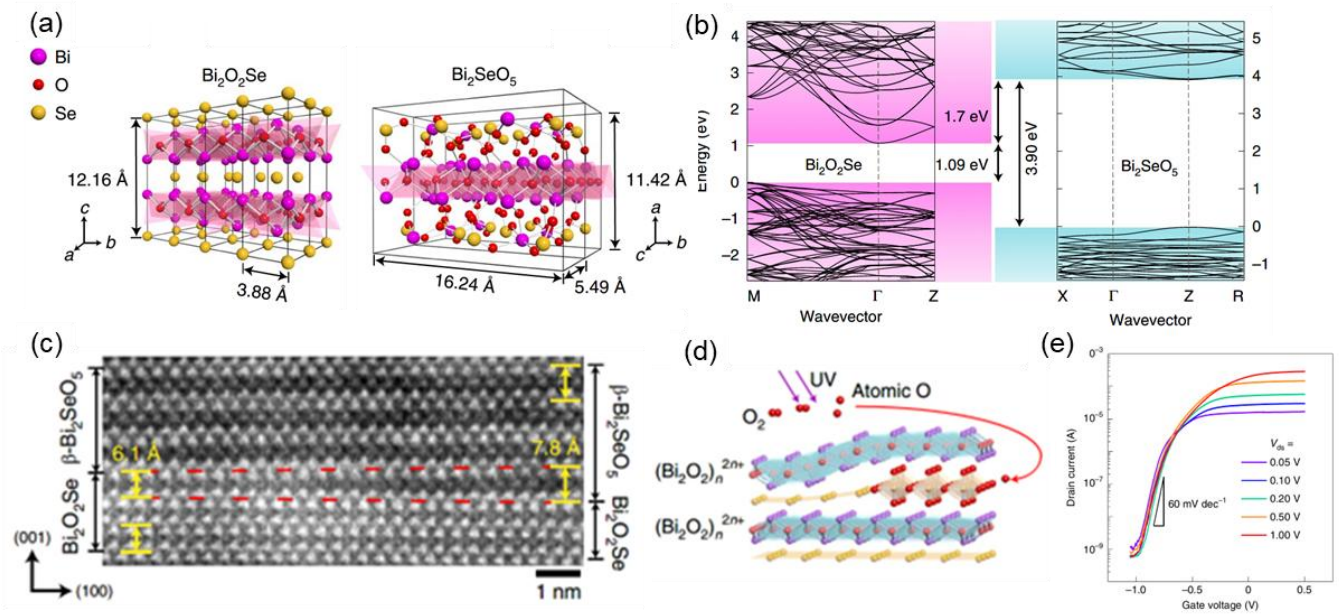

Figure 5. The vdW interfaces prepared by bottom-up method. Reproduced with permission from Ref. [74, 75]. (a) Structure information of Bi_2SeO_5 and Bi_2O_2Se. (b) Band alignment between Bi_2SeO_5 and Bi_2O_2Se. (c) STEM image of Bi_2SeO_5/Bi_2O_2Se. (d) Mechanism of unzip Bi_2SeO_2 by UV oxidation. (e) Transfer curve of a top-dated Bi_2SeO_5/Bi_2O_2Se FET.

deposition relied strongly on the high-energy deposition process, leading to damage to 2D semiconductors. Recently, various progresses have been made in this method, which can result in high-performance interface and improved device properties, as elaborated below.

One of the ideal cases is the Bi_2SeO_5/Bi_2O_2Se interface. Bi_2O_2Se is layered 2D semiconductor with a band gap of 1.09 eV, as shown in figure 5 (a)-(b). It can be directly converted to insulating phase Bi_2SeO_5 (band gap ~3.90 eV and dielectric constant ~16.5 [77]) using a UV-assisted intercalation, as illustrated in figure 5(d). By carefully controlling the oxidation process, vdW interface can be formed between Bi_2SeO_5 and Bi_2O_2Se, as shown in Figure 5(c) [78,79]. This interface exhibits large band offsets, where both conduction and valence band offsets exceed 1 eV, as suggested by first-principles calculations. Therefore, the vdW Bi_2SeO_5/Bi_2O_2Se interface is expected with promising device performance. As figure 5(e) shows, the Bi_2SeO_5/Bi_2O_2Se device with ultra-thin Bi_2SeO_5 (EOT < 0.5 nm) as the gate dielectric shows outstanding transfer characteristics, such as gate leakage below 0.015 A/cm2, low SS of 65 mV/dec, high mobility of 10^2 cm^2 V^{-1} s^{-1}, on/off ratio of 4×10^5 and small hysteresis window of 20 mV. Further study shows that Bi_2SeO_5/Bi_2O_2Se can be used to construct inverter circuits (see Figure 5(d) with large voltage gain. With these promising interface properties of Bi_2SeO_5/Bi_2O_2Se, their practical applications

hinge on the large scale and high-quality growth of 2D semiconductor Bi_2O_2Se.

3.4 Quasi-vdW interfaces by bottom-up methods

Inorganic molecule crystals (IMCs) are emerging high-*k* dielectrics that can form quasi-vdW interface with 2D semiconductors using the bottom-up method. IMCs consist of molecule clusters bound by weak vdW interaction. This unique structural feature endows IMCs dangling-bond-free surface, and more importantly, they could be directly deposited on 2D semiconductors at low temperature. For instance, as shown in Figure 6(a), IMC Sb_2O_3 was grown on a substrate before being integrated onto MoS_2 using thermal evaporation at a relatively low temperature. [80]. The resulting high-performance vdW interface and minimized damage to MoS_2 can be seen from the outstanding device performance, in which high carrier mobility (145 $cm^2 V^{-1} s^{-1}$), large on/off ratio (>10^8), and low SS (64 mV/dec) have been achieved. However, due to the relatively small band gap (~3.9 eV) and loose structure, its band offsets with monolayer MoS_2 might not be large enough[145] and the leakage current is notably increased when the thickness of Sb_2O_3 is decreased.

To address the above issues, further improvement has been made by directly evaporating a thin layer of Sb_2O_3 on MoS_2 [92], followed by ALD growth of HfO_2 (see figure 6(b)-(c)). The thin Sb_2O_3 layer serves as both seeding and buffer layers, in which its hydrophilic surface enables the ALD deposition of HfO_2 thin film, and it also reduces the dangling bond effect of HfO_2 on the channel MoS_2. Therefore, improved electrical performance has been demonstrated in $HfO_2/Sb_2O_3/MoS_2$ based devices, as shown in figure 6(d). Similar efforts include the use of molecular crystal 3,4,9,10-perylene-tetracarboxylic dianhydride (PTCDA) as the buffer/seeding layer. As shown in figure 6(e), an atomically thin PTCDA layer (~0.3 nm) was deposited on MoS_2 using chemical vapor deposition (CVD), and then HfO_2 was grown on PTCDA [93]. A high-performance interface can be formed, as shown in figure 6(f), which is evidenced by the promising device performance (see figure 6(g)-(h)). While this method looks quite promising to achieve high-performance integration of high-*k* dielectrics for 2D electronics, further efforts are needed to explore the large-scale, uniform, and low temperature growth of the buffer/seeding layers with minimum impact on the 2D semiconductors.

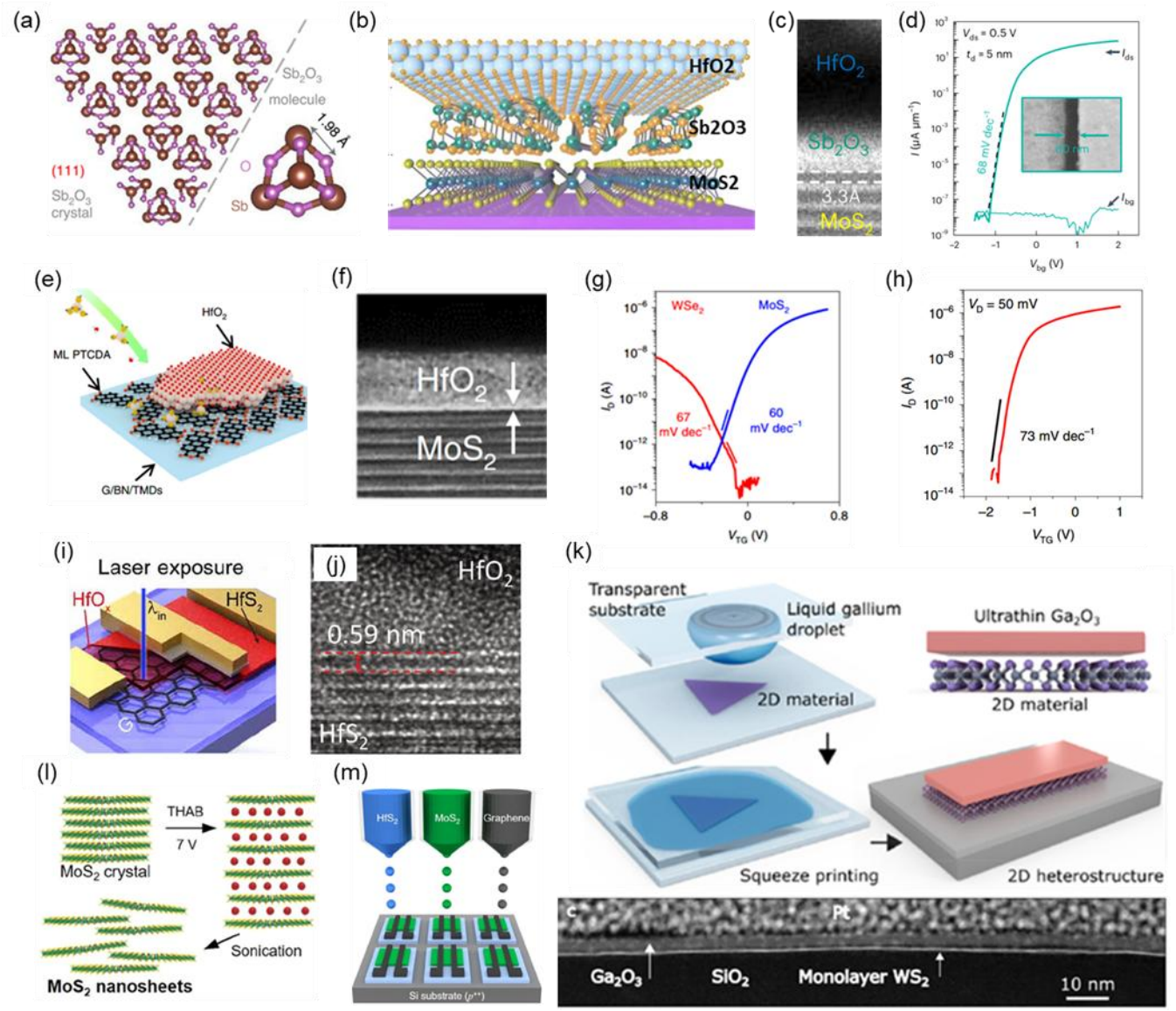

Figure 6. Quasi-vdW interfaces prepared by bottom-up method. (a) Structure information of inorganic molecular crystal Sb_2O_3. Reproduced with permission from Ref. [77]. (b)-(d) Schematic diagram of interface, cross-sectional STEM image, SS statistics and short-channel transfer curve based on HfO_2/MoS_2 transistor with Sb_2O_3 buffer layer. Reproduced with permission from Ref. [89]. (e)-(h) Schematic diagram, STEM image and performance curve of PTCDA-assisted HfO_2/MoS_2. Reproduced with permission from Ref. [90]. (i) Schematic diagram of HfO_2/HfS_2 transistor. Reproduced with permission from Ref. [79]. (j) TEM image of HfO_2/HfS_2 by ozone plasma. Reproduced with permission from Ref. [78]. (k) Liquid metal printing processes. Reproduced with permission from Ref. [87]. (l)-(m) MoS_2 ink preparation and fabrication process of an all-ink-jet printing HfO_2/MoS_2 FET. Reproduced with permission from Ref. [82].

Interface engineering has also been employed to try to achieve quasi-vdW interface between conventional high-*k* oxides and 2D semiconductors [81–84,91,105]. For example, for the layered 2D HfS_2, oxidation has been carried out to oxidize the top layers of HfS_2 and form HfO_2 using ozone plasma. Photo-oxidation (figure 6(i)) [82] and revised ozone treatment (figure 6(j)) [81]

have been used to convert HfS_2/MoS_2 into HfO_2/MoS_2, respectively. The resulting quasi-vdW interface of HfO_2/HfS_2 can be seen from the HETEM image in figure 6(j). The corresponding devices show improved electric performance such as high on/off ratio, small SS (63 mV/dec), and negligible hysteresis window. The main challenge of this interface engineering is on the control of the treatment process, which should realize large-scale high-quality high-*k* oxides while not damaging the 2D semiconductors. Besides, first-principles calculations have revealed that interface hydrogenation can selectively passivate the surface dangling bonds of HfO_2 while not affecting 2D semiconductors such as MoS_2, leading to high-performance interface. However, this theoretic prediction awaits further experimental verification [35].

Moreover, to meet the high-yield, low-cost, large-area production, ink-jet printing methods are employed into laboratory and industry more and more frequently [85–90]. Diverse vdW materials are able to be assembled by different electronic 2D materials inks. Owing to the versatility of liquid-phase exfoliation, various 2D vdW high-*k*/semiconductors devices can be fabricated by ink-jet printing, thus making it a promising way to manufactory. For instance, MoS_2-based ink-jet printing utilize pre-fabricated MoS_2 nanosheets by means in figure 6(l) [85] or electrochemical exfoliation [87]. In an entirely ink-jet printing case shown in figure 6(m), the quasi-vdW surfaces created by the ink-jet printed devices have capability in large-scale fabrication with high mobility of 10 $cm^2\ V^{-1}\ s^{-1}$ high on/off ratio over 10^5. Similarly, the method shown in figure 6(k) necessitates the selection of an appropriate liquid metal system to form high-performance oxide interfaces at ambient conditions [90]. From the lower figure 6(k) we can clearly identify a vdW-gap between WS_2 and Ga_2O_3. However, the high leakage current of 2.4×10^{-4} A/, and trapping state density of $4.8\times10^{12}\ cm^{-2}\ eV^{-1}$ in this device indicates that further improvement is needed for this kind of system. Besides, the accurate control of layer-by-layer deposition remains the issue to take advantages of 2D layered materials, since the agglomeration, low uniformity and uncovered regions always hinder the transport properties.

Perspectives and Conclusions

In summary, this mini-review briefly introduces recent advances in the vdW-integrations of high-*k* dielectrics onto 2D semiconductors, in which both top-down (transfer) and bottom-up

(direct growth) methods, along with their representative examples, have been discussed.

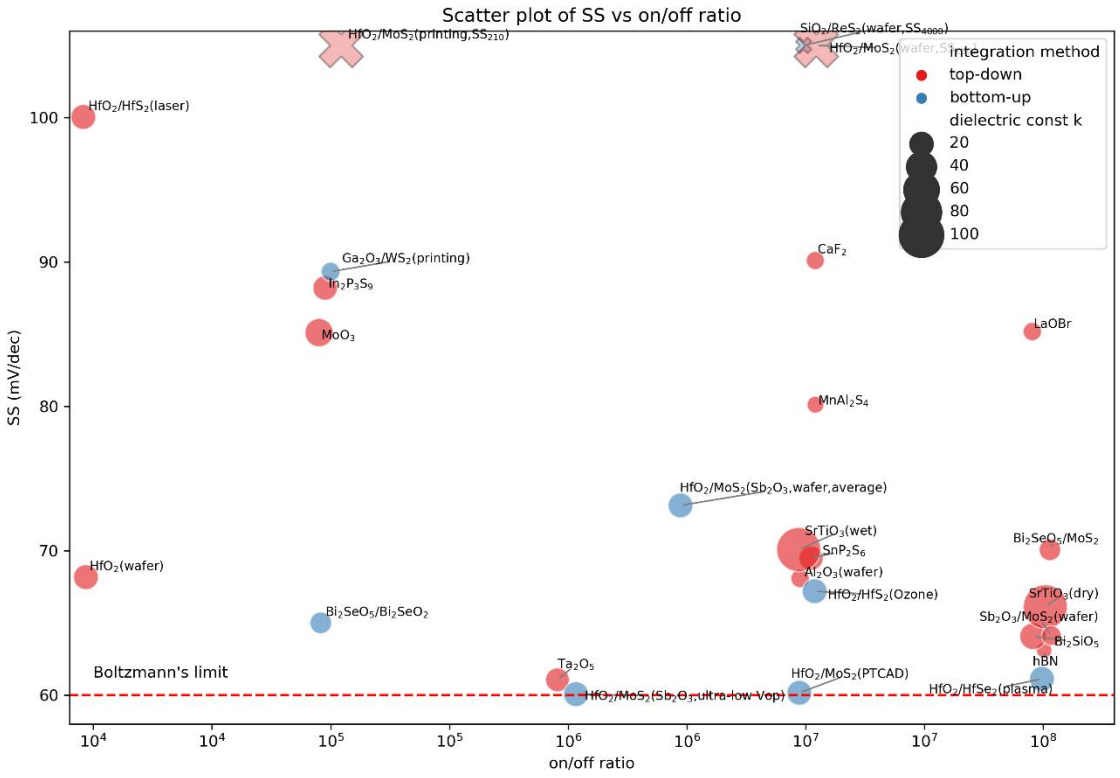

Figure 7. Scattering diagram of various high-*k*/2D interfaces, with the x-axis representing the on/off ratio and the y-axis representing the subthreshold swing (SS). Red circles indicate interfaces made by top-down methods, while blue circles represent those made by bottom-up methods. The size of each circle corresponds to the k value, with larger circles indicating higher k values. The three crosses at the top of the diagram indicate systems with excessively high SS values. Each interface is labeled with brief information.

Significant progresses have been made in both integration methods for the high-performance high-*k* dielectrics/2D semiconductors interfaces. As shown in Figure 7, we have selected the on/off ratio and subthreshold swing (SS) together to evaluate various results. The performance variation reflects the interface quality, and device configurations such as the thickness of the dielectrics and the semiconductors and the channel length. An interface that excels in both SS value and switching ratio must be sufficiently thin and efficient. Thinner dielectrics provide better gate control, as indicated by SS, but suffer from large leakage current as indicated by the on/off ratio, and vice versa. According to this trade-off, some further research of high-*k* dielectric integration on 2D semiconductors could be inferred to further improve the device performance.

Through all these studies, the overall performances and qualities of high-*k* dielectrics/2D semiconductors achieved through top-down methods surpass those obtained via bottom-up

approaches, and wafer-scale samples typically exhibit inferior performance compared to experiment-scale ones. In comparison to *h*-BN, several high-*k* dielectrics using the top-down method have already surpassed its interface performance, as illustrated in figure 7, with the best devices approaching both the Boltzmann limit and a high switching ratio of 10^8. These include $SrTiO_3$, $Bi2SiO_5$, and Bi_2SeO_5. In most large-scale scenarios, unacceptably high SS and low switching ratios are still observed. While large-scale transfer techniques can address challenges associated with uniformity and interface quality[76,147–153], more efforts are needed to address the issues such as high process complexity and low process uniformity. For the bottom-up approaches, they offer advantages such as better scalability and greater compatibility with existing semiconductor fabrication processes. However, they still have significant room for the improvement of interface quality.

To improve the integration performance, the research on the below topics is necessary: (1) To explore the high-*k* materials with high dielectric constant and large band offsets with promising 2D semiconductors such as MoS_2. These high-*k* dielectric candidates should be able to be directly deposited on the 2D semiconductor with high-quality using a low-energy and low-temperature deposition process to minimize the growth impact to the 2D semiconductors. Such exploration requires the search on the vast material space, thus a synergistic effort of high-throughput first-principles calculations, machine learning technologies, and experiments is needed to accelerate the development process; (2) To explore better molecular crystal-based buffer, seeding layers or sacrificial layers. Currently, molecular crystals such as Sb_2O_3 or PTCDA can be directly grown on 2D semiconductor MoS_2 at low temperature, without bringing noticeable damage to MoS_2, thus serving as promising buffer/seeding layers for the ALD growth of high-performance high-k oxides such as HfO_2. Molecular crystals with better dielectric performance and compatible with consequent ALD growth are highly desired to further improve the device performance and scaling capability; (3) To have an improved understanding of the interface between buffer layers/2D semiconductors and also the interface between buffer layers and high-*k* materials. The interface properties such as defect properties, band alignments, leakage current, and interface stability are crucial to improve the integration performance, thus both experimental and computational efforts are required to elucidate these effects.

Optimistically speaking, with the extensive efforts on the exploration of high-*k* dielectrics for 2D semiconductors, high-performance interface could be achieved to meet the practical

requirements of advanced 2D electronics. Along with other breakthroughs such as the growth of 2D semiconductors, metal contact, doping, and device optimization, it is promising to realize high-performance 2D electronics.

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