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Dual-Loop Constant Voltage Regulation in Wireless Power Transfer Systems Using Phase-Shift and Duty Cycle Modulation

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Abstract: This study investigates the single transmitter and single receiver (STSR) with dual-output capability. This methodology utilizes dual half-wave rectification. Initially, the system topology of the STSR multi-channel voltage output is presented with the inductor-capacitor-capacitor-series (LCC-S) compensation topology, followed by an in-depth analysis of its double-channel voltage output characteristics. Through detailed analysis and empirical validation, the system is shown to maintain high efficiency and stable performance, making it well-suited for applications demanding reliable dual-voltage outputs under dynamic conditions.

Keywords: wireless power transfer; resonant converter; double outputs

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1. Introduction

Wireless power transfer (WPT) technology has emerged as a transformative solution to the challenges associated with wired power connections [1], particularly in applications requiring contactless energy transfer [2], such as electric vehicles (EVs) [3], autonomous robots [4], and medical implants [5]. The rapid growth of these applications has led to increased research on advanced WPT systems capable of efficiently delivering power over distances while maintaining high alignment tolerance and stability [6]. One promising approach within this domain is the development of multi-output WPT systems, which aim to provide power to multiple loads through a single transmitter simultaneously. This multi-output capability is highly desirable in settings where multiple devices or subsystems require concurrent charging, enabling operational flexibility and reducing the need for various power sources or receivers [7].

In particular, double-output WPT systems have gained attention for their ability to provide distinct dual-power channels within a unified architecture [8]. Such configurations are especially valuable in environments with spatial constraints or those where centralized power management is essential [9]. Double-output systems can reduce hardware redundancy, simplify installation, and enhance energy distribution within complex systems [10,11]. One of the principal challenges in these systems lies in maintaining stable voltage outputs across both channels, especially when subject to load variations [12]. Voltage fluctuations and load instability can significantly impact the performance of the connected devices, making stability a crucial design consideration for practical double-output WPT applications [13,14].

Current investigations are paying more attention to utilizing one transmitting coil and one receiving coil but with dual output channels [15]. In contrast, the proposed system fully utilizes both positive and negative half-waves of the AC signal by implementing distinct rectification circuits within a single receiving coil. Specifically, an active half-wave rectifier utilizing a MOSFET processes the negative half-wave, while a passive diode half-wave rectifier harnesses the positive half-wave, delivering stable dual outputs without

additional magnetic couplers, control schemes, or compensatory circuits [16]. This approach achieves efficient dual-output power transfer through a simplified configuration that maximizes energy extraction from each waveform phase, directly addressing the need for both compactness and reliability [17,18].

The presented work introduces a WPT system with dual rectification pathways, offering a highly efficient and stable dual-output power transfer solution in a compact and scalable architecture. Unlike existing solutions, which often rely on multiple receivers or complex high-order compensation networks, the proposed method employs a single receiver coil and active rectifiers to deliver multiple controllable outputs, leading to significant reductions in volume. This design not only improves spatial efficiency but also avoids cross-coupling between receivers, addressing key limitations in conventional systems [19].

2. Methods

The topology of the proposed single-input and dual-output system utilizing dual half-wave rectification is illustrated in Figure 1.

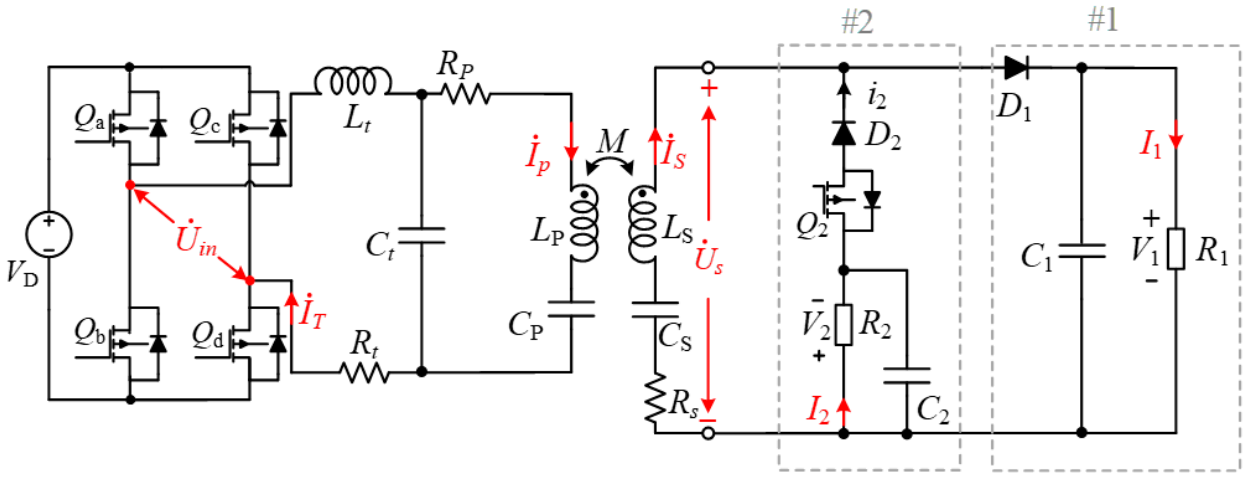

Figure 1. The circuit schematic of the proposed WPT system.

In this configuration, L_t, L_p, and L_s represent the compensation inductor, the transmitting coil, and the receiving coil, respectively, while R_t, R_p, and R_s denote the parasitic resistances of L_t, L_p, and L_s, respectively. Furthermore, C_t, C_p, and C_s are the compensating capacitors. Specifically, Diode D_1 is adopted to form a diode half-wave rectifier circuit for output channel #1, whereas Diode D_2 is adopted to form a controllable half-wave rectifier circuit for output channel #2. In particular, the voltage of V_1 is controlled by the primary inverter. And the control of the voltage V_{12} is realized by adjusting the conduction angle of the switching MOSFET Q_1. Then, capacitors C_1 and C_2 serve as filter capacitors connected in parallel with loads R_1 and R_2, respectively. As a result, the double output loops are labeled as #1 and #2.

The proposed WPT design, utilizing dual rectification pathways, provides a scalable and efficient solution for stable dual-output power transfer within a compact framework. By integrating two distinct rectification techniques, the system achieves dual-output functionality, surpassing traditional full-bridge rectifiers in both performance and controllability. As shown in Figure 2, during the positive half-wave cycle of the receiving end, the designed circuit topology is capable of supplying power to load R_1 via the diode half-wave rectification at the output channel #1. During this period, the output channel #1 is turned on while the output channel #2 is turned off, as illustrated in Figure 3. During the negative half-wave cycle of the receiving end, the system provides power to the load R_2 via the controllable half-wave rectifier circuit. During the negative half-cycle, MOSFET Q_1 is activated. The output channel #2 is turned on during this period while the output channel #1 is turned off,

as illustrated in Figure 4. Then, following filtration by capacitors C_1 and C_2, it then flows through load R_1 and R_2 to deliver the dual-power outputs.

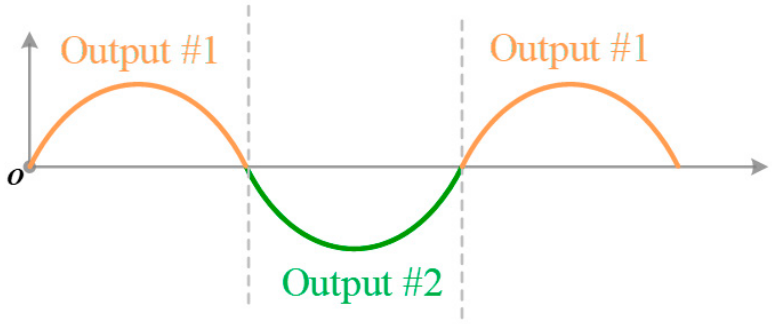

Figure 2. The output loops with respect to the rectification waves.

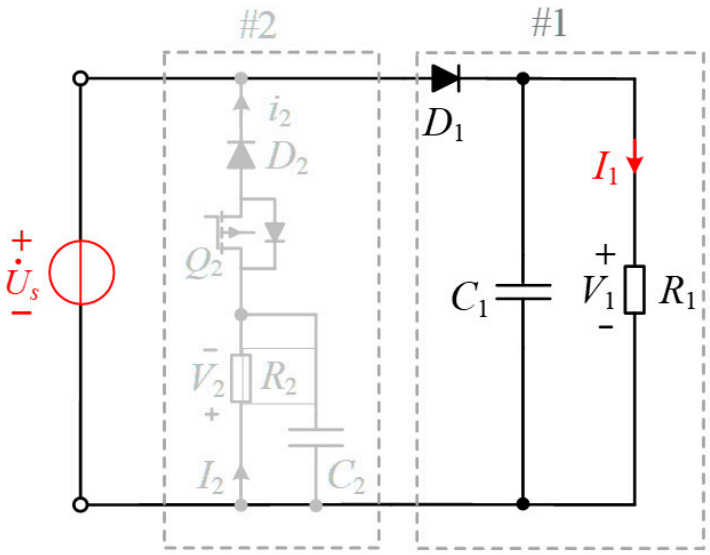

Figure 3. The simplified circuit diagram during the positive half-wave period through the output loop #1.

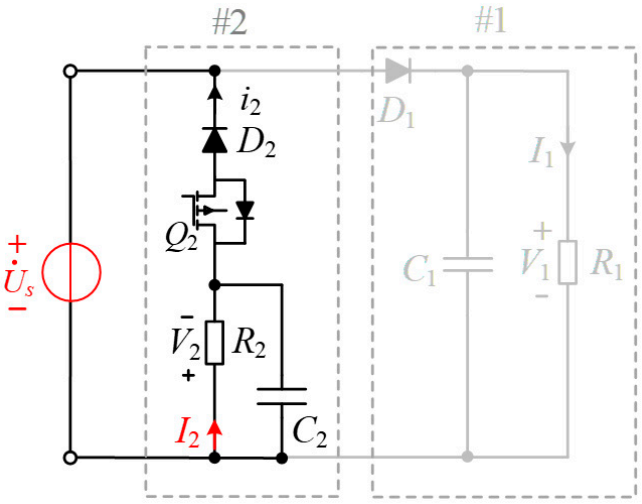

Figure 4. The simplified circuit diagram during the negative half-wave period through the output loop #2.

3. Mathematical Analysis

3.1. Overview of the Circuit

According to the system resonance conditions, the compensation capacitors C_t, C_p, and C_s should be satisfied as follows:

$$\begin{cases} C_t = \left(\omega^2 L_t\right)^{-1} \\ C_p = \left[\omega^2 \left(L_p - L_t\right)\right]^{-1} \\ C_s = \left(\omega^2 L_s\right)^{-1} \end{cases} \tag{1}$$

where ω is the operating frequency.

By applying Kirchhoff's laws and considering the resonance conditions of the system circuit, the following equation can be derived:

$$\begin{cases} \dot{U}_{in} = (j\omega L_t + R_t - j/\omega C_t)\dot{I}_t + j\omega L_t \dot{I}_t \\ 0 = \left(j\omega L_p + R_p - j/\omega C_p - j/\omega C_t\right)\dot{I}_p + j\dot{I}_t/\omega C_t - j\omega M\dot{I}_s \\ 0 = -j\omega M\dot{I}_p + (j\omega L_s + R_s - j/\omega C_s)\dot{I}_s + \dot{U}_s \\ \dot{U}_s = R_{eq}\dot{I}_s \end{cases} \tag{2}$$

where U_{in} is the output voltage of the inverter. I_{t} is the output current of the inverter. I_{p} is the current flowing through the transmitting coil. And R_{eq} is the equivalent resistance, which can be expressed as

$$R_{eq} = R_{eq1} \| R_{eq2} \tag{3}$$

where R_{eq1} and R_{eq2} are the equivalent resistance of the outputs #1 and #2, respectively. Then, the output voltage on the secondary side can be expressed as

$$\dot{U}_s = \frac{\omega^2 M L_t \dot{U}_{in} R_{eq}}{(R_{eq} + R_s)(2R_p R_t + (1/\omega C_t)^2) + R_t \omega^2 M^2} \tag{4}$$

The U_{s} is the rms value of the output voltage on the secondary receiving coil. And the output voltage of the half-wave rectification can be expressed as

$$V_1 = \sqrt{2}U_s - V_{df} - \frac{\Delta V}{2} \tag{5}$$

where ΔV is ripple voltage and V_{df} is the diode forward voltage drop. And the output voltage of loop #2 can be expressed as

$$V_2 = \frac{1}{2\pi}\int_0^{2\pi \cdot D_{\mathrm{Q2}}} \sqrt{2}U_s \sin(\omega t) d\omega t = \frac{\sqrt{2}U_s}{2\pi}\left(1 - \cos\left(2\pi D_{Q2}\right)\right) \tag{6}$$

where D_{Q2} is the duty cycle of the driving PWM signal on the MOSFET.

3.2. The Controlling Strategy

This paper utilizes a constant voltage control method, organized into inner and outer control loops, and is illustrated in Figure 5. The system comprises two distinct controllers: a primary controller on the primary side and a secondary controller on the secondary side. The primary controller's main function is to receive feedback from the secondary side, using this information to control the conduction state of the switching elements within the inverter. In parallel, the secondary controller is responsible for sampling and acquiring voltage signals, which are then transmitted to the primary controller. The primary controller analyzes these signals and adjusts the conduction state of the switching elements on the secondary side accordingly.

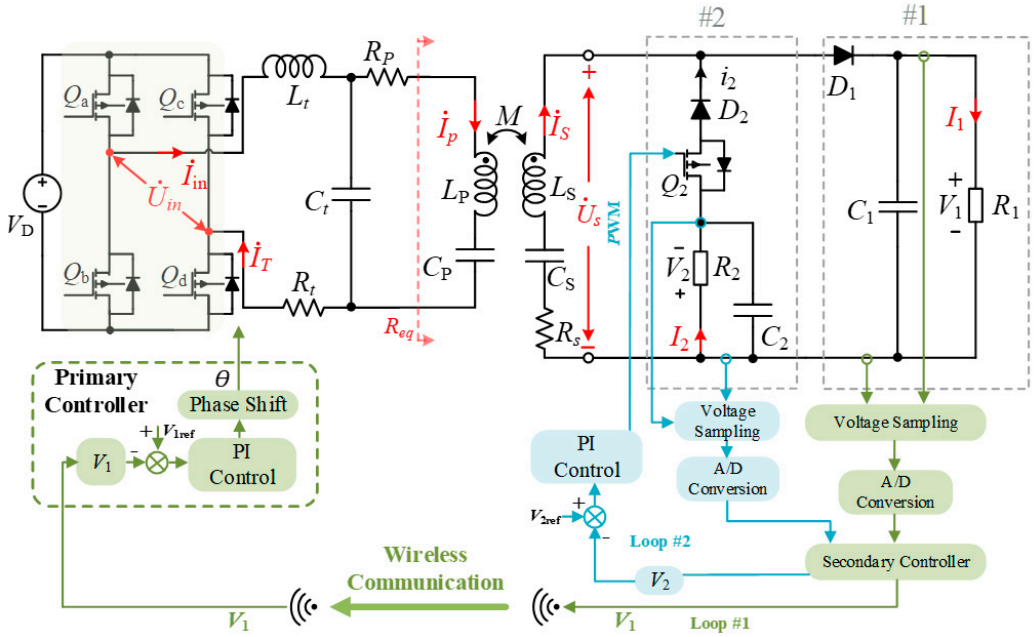

Figure 5. The overview of the diagram with the constant voltage output control strategy.

The system is designed to manage two controlled variables—denoted as V_1 and V_2—each requiring adjustable output levels. To achieve precise and independent control over these variables, the system employs two closed loops: one outer loop, designated as Loop #1, for adjusting V_1, and one inner loop, Loop #2, for regulating V_2.

This dual-loop configuration enables robust and adaptive control over double output channels, supporting consistent voltage regulation across varied load conditions and ensuring system stability and performance.

3.2.1. The Control of the Outer Loop #1

Firstly, the outer loop, designated as Loop #1, primarily regulates the output voltage V_1 by adjusting the input voltage U_{in}. Common methods for controlling U_{in} by the phase-shift control. Figure 6 illustrates the circuit configuration of the full-bridge inverter, accompanied by a timing diagram representing the phase-shift process. MOSFETs Q_a and Q_b operate in a complementary conduction state, as do Q_c and Q_d, as shown in Figure 7. When phase-shift control is applied, a phase-shift angle θ is introduced between the two bridge arms [20]. In the proposed method, maintaining in-phase voltage and current from the inverter ensures the zero phase angle (ZPA).

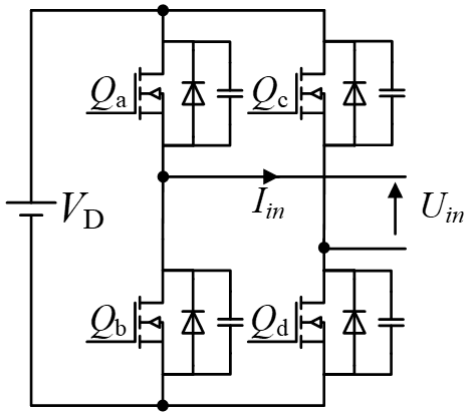

Figure 6. The circuit diagram of the full-bridge inverter.

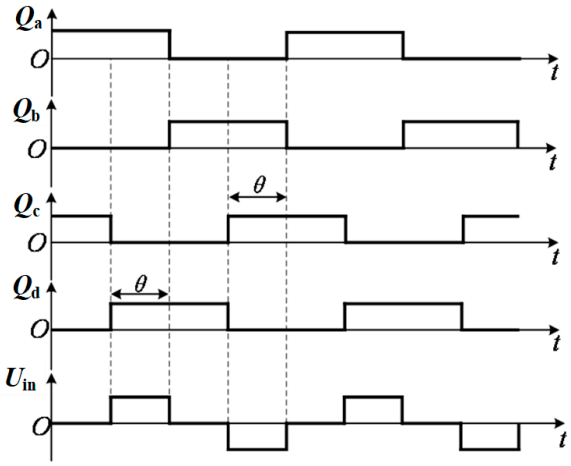

Figure 7. The phase-shift sequence in the full-bridge inverter circuit.

Following the application of the Fourier transformation, the fundamental wave can be obtained as [21]

$$U_{\text{in}} = \frac{4V_D}{\pi} \sin\frac{\theta}{2} \sin \omega t \tag{7}$$

And the related RMS value can be written as [22]

$$U_{\text{in}} = \frac{2\sqrt{2}V_D}{\pi} \sin\frac{\theta}{2} \tag{8}$$

The preceding formula demonstrates that the system can regulate the input voltage Uin by controlling the phase shift angle θ of the full-bridge inverter, thus achieving precise control of the output voltage V_1. The outer loop control strategy, depicted in the block diagram in Figure 8, illustrates this process.

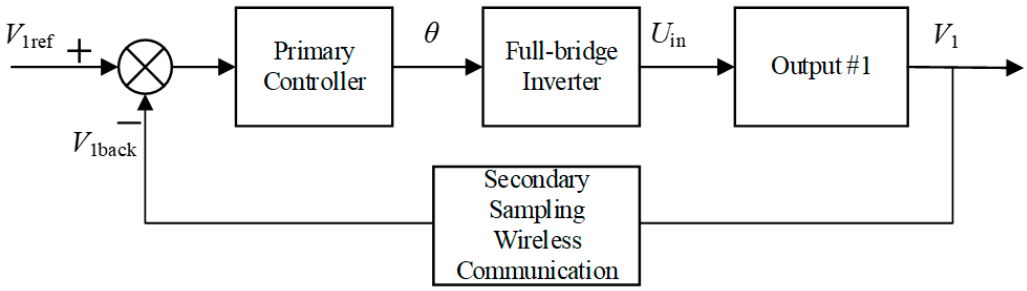

Figure 8. The block diagram of the outer loop #1 constant voltage control strategy.

In this setup, the secondary-side controller first samples the voltage across R_1 and transmits the voltage signal to the primary side via communication modules, such as antennas. Upon receiving the feedback signal $V_{1\text{back}}$, the primary-side controller compares it to the reference voltage $V_{1\text{ref}}$, producing an error signal, which is then processed by the primary-side PI controller. The controller calculates the appropriate phase shift angle θ based on this error and sends it to the full-bridge inverter. By adjusting the phase shift, the inverter modifies the system's input voltage U_{in} accordingly. The adjusted U_{in} influences the double-output WPT system, subsequently altering the voltage V_1 across R_1. This closed-loop feedback process enables constant voltage control of V_1, ensuring stable and reliable output in response to variations in load or system conditions.

3.2.2. The Control of the Inner Loop #2

The inner loops, designated as Loop #2, primarily regulate the output voltage V_2 by adjusting the conduction time of the switching elements within each respective loop. The

control scheme block diagram for Loop #B is presented in Figure 9. For constant voltage control within this loop, the secondary-side controller first samples the output voltage V_2, comparing it to predefined reference values within the controller. The resulting error signals are processed by a PI controller, which then generates control signals for the drivers of the corresponding switching elements in this loop. The control signal, represented as duty ratio D_{Q2}, determines the conduction times T_{on} of the switch. By modulating this conduction time, the system can effectively adjust the output voltages V_2, achieving stable, constant voltage control for each output. This approach ensures precise voltage regulation across multiple output channels, contributing to the system's overall reliability and performance in varied load conditions.

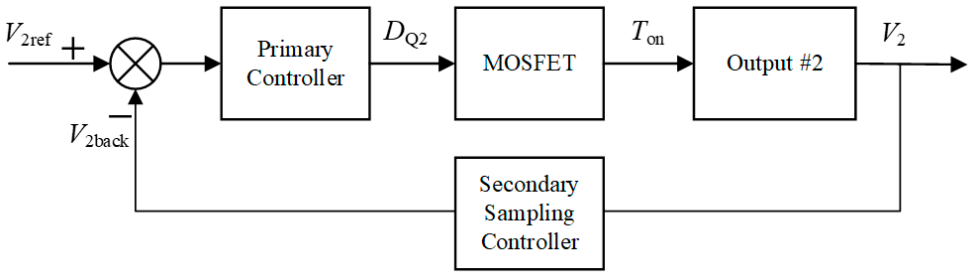

Figure 9. The block diagram of the inner loop #2 constant voltage control strategy.

4. Experimental Verification

An experimental prototype of the proposed inductive charging system is constructed, as shown in Figure 10. The inverter is based on the silicon carbide module CCS020M12CM2, controlled by the FPGA ALTERA Cyclone IV, and powered by a DC power supply (ITECH Auto Range DC Power Supply IT6726H), which serves as the high-frequency AC power source for the transmitter. Two electronic loads are used: ITECH DC IT8512A and ITECH IT8814B, which simulate real-world loading conditions. The compensating capacitors are constructed using PHE448 polypropylene film capacitors from KEMET. All experimental waveforms are captured using a KEYSIGHT DSO-X 3024T oscilloscope during the testing process.

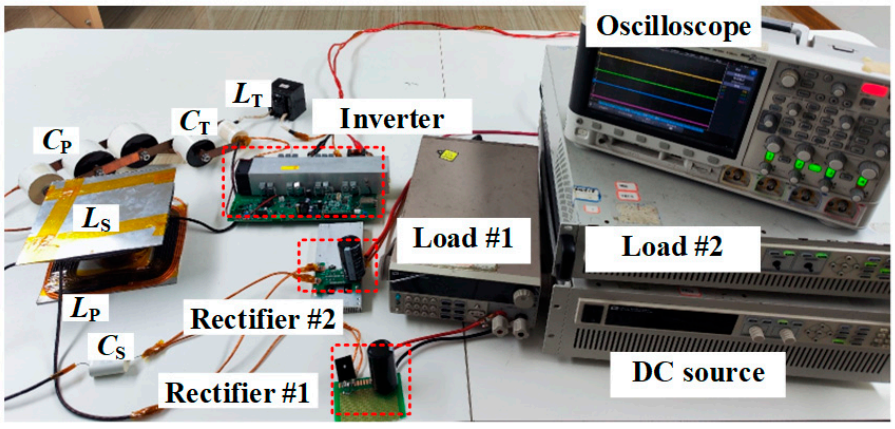

Figure 10. The picture of the proposed experimental setup.

Figure 11 illustrates the efficiency profile of the presented WPT system under varying load conditions, specifically across an extended resistance range for R_1 and R_2 from 5 Ω to 200 Ω. The three-dimensional surface plot highlights the variations in efficiency across the load range, with efficiency values dynamically influenced by the resistances of R_1 and R_2. The maximum efficiency achieved is 88.86%, while the minimum efficiency is 64.51%, indicating a promising power transfer capability in the proposed configuration.

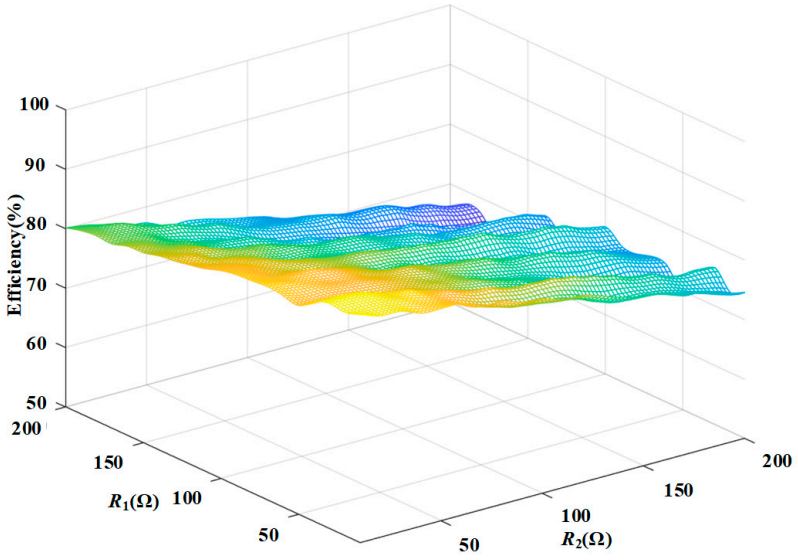

Figure 11. The diagram of efficiency under different load value conditions.

Figure 12 shows the oscilloscope waveform of the voltage and current characteristics of the proposed double-output WPT system. The output voltage of the inverter (U_{in}) is presented at a scale of 100 V per division, while the output current of the inverter (I_{in}) is depicted with a scale of 10 A per division. The output voltages (V_1 and V_2) for two channels are captured at 20 V per division each, clearly representing the system's electrical behavior under the given load conditions. In this figure, U_{in} and I_{in} are in the same phase, indicating that the entire system can realize ZPA in the system. Primarily, this figure includes detailed information on the switching period (11.78 µs), rise time (1.65 µs), and fall time (1.65 µs).

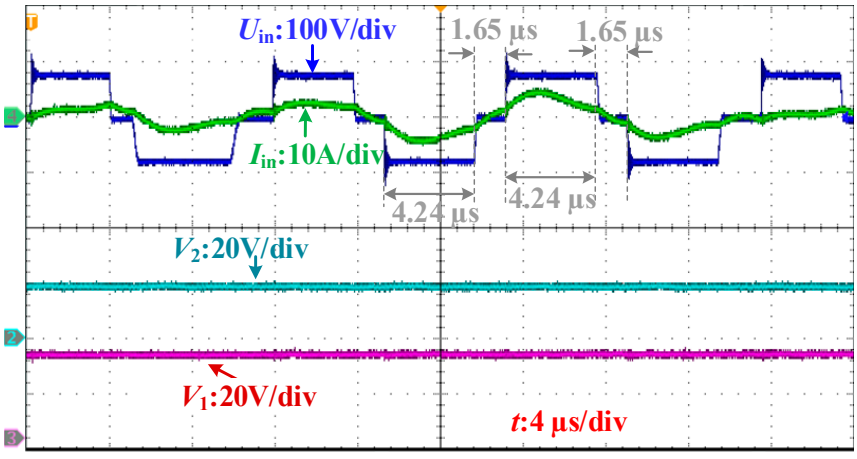

Figure 12. The core waveforms of the system.

Figure 13 presents the effect of changing load conditions for channel #1 (R_1) on the proposed double-output WPT system. The input voltage (U_{in}) is represented with a scale of 100 V per division, while the output voltages (V_1 and V_2) are shown at 20 V per division. In this figure, the load R_1 varies between 10 Ω and 20 Ω, with the changes indicated by the dashed red lines. This demonstrates the load-independence of the outputs. After the slight ripples, the output becomes reference values again. It shows the load-independent characteristics of the proposed system, making it better suited for practical applications where independent and stable power delivery to multiple loads is required.

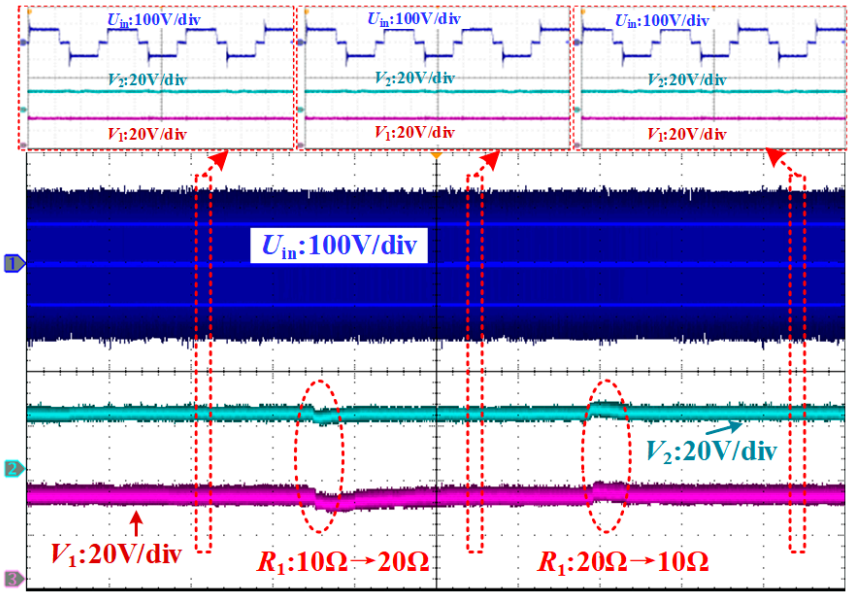

Figure 13. The dynamic response under the change of the load in channel #1.

Figure 14 illustrates the dynamic behavior of the proposed double-output WPT system under changing load conditions for channel #2 (R_2). In this figure, the load R_2 for channel #2 varies between 10 Ω and 20 Ω at different time intervals, marked by the dashed red lines. Notably, the output voltage for channel #1 (V_1) remains unaffected by the load variations in channel #2, demonstrating effective decoupling and independent regulation of the two output channels.

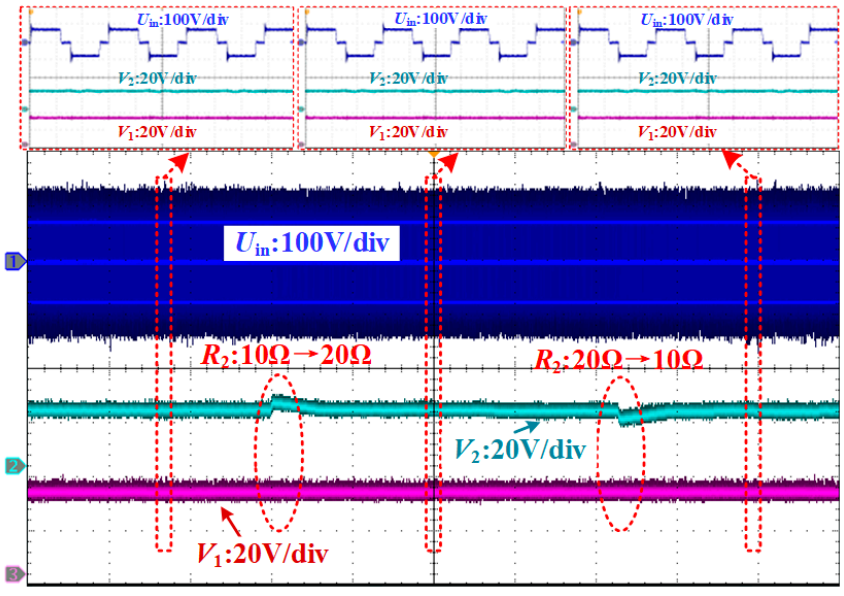

Figure 14. The dynamic response under the change of the load in channel #2.

Figure 15 shows the response of the proposed double-output WPT system to changes in the input voltage U_{in}. The input voltage is depicted with a scale of 100 V per division, while the output voltages for Channel #1 (V_1) and Channel #2 (V_2) are shown at 20 V per division. In this figure, the input voltage U_{in} is adjusted in steps between 80 V, 70 V, and back to 80 V, with these variations marked by dashed red lines. This figure highlights the stability of the output voltages on the input power supply, emphasizing the importance of regulated control to maintain reliable outputs for both channels.

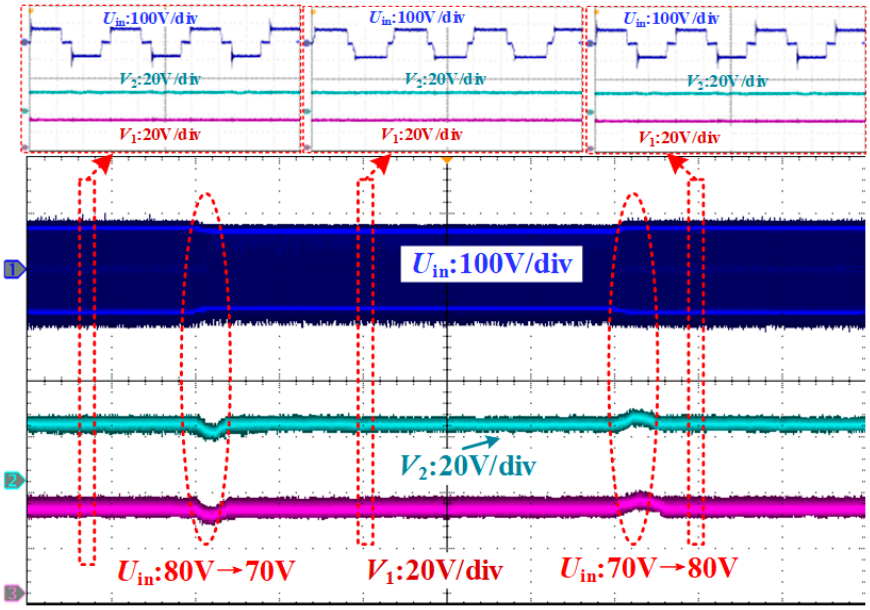

Figure 15. The dynamic response under the change of U_{in}.

5. Discussion

The proposed WPT design with dual rectification pathways provides a scalable and efficient solution for stable dual-output power transfer in a compact architecture. By utilizing two rectification methods, the system enables dual-output functionality, surpassing conventional full-bridge rectifiers. Table 1 shows the specific comparison with several existing solutions. In comparison to [7,23], the proposed method enables multiple outputs using a single receiver coil, thereby reducing both space and cost while mitigating the issue of cross-coupling between multiple receivers. In comparison to [24], the proposed method achieves multiple controllable outputs using active rectifiers rather than DC/DC converters, which saves the spatial volume. In contrast to [25], the proposed method enables multiple outputs without the need for many high-order compensation networks on the receiver side, i.e., T topologies, thereby significantly reducing the volume.

Table 1. Comparison with several existing solutions.

Paper	Approach	Efficiency	Applications	Characteristics
[7]	Multiple Magnetic Coil Design	84.5%	Automated Guided Vehicles	Single Inputs and Dual Outputs
[23]	Multiple Magnetic Coil Design	45.1%	Lighting	Multiple Inputs and Multiple Outputs
[24]	Multiple DC-DC converters	85%	Battery-Powered Electric Vehicles	Utilizing DC-DC Converters
[25]	Multiple Outputs Based on Double T Circuits	91.1%	DC Motor Drives or Flash Memory Drives	Utilizing the Resonant Networks
This paper	Dual Half-wave Rectifiers	88.86%	Consumer Electronics	Two Different Rectifiers

6. Conclusions

The proposed WPT design with dual rectification pathways offers a scalable and efficient solution for stable dual-output power transfer within a compact architecture. By employing two different rectification methods, the system achieves dual-output functionality, surpassing conventional full-bridge rectifiers in both performance and controllability.

The proposed design not only increases the number of output channels but also enhances control flexibility. Additionally, it has the capability to reduce system complexity and improve spatial utilization. This architecture's ability to reduce system complexity and enhance spatial utilization. Moreover, the maximum efficiency realizes 88.86% under varying load conditions, specifically across an extended resistance range for R_1 and R_2 from 10 Ω–50 Ω. By applying the proposed method, the system successfully maintains the stability of the output under the conditions of load variations, showing great potential in the utilization of dual-loop consumer electronics.

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Conflicts of Interest: The authors declare no conflict of interest.

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