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A New Three-Phase Hybrid Multilevel Topology with Hybrid Modulation and Control Strategy for Front-End Converter Applications

Muhammad Ali [1,*], Muhammad Talib Faiz [2], Muhammad Mansoor Khan [3], Vincent Ng [1] and Ka-Hong Loo [1,2]

[1] Centre for Advances in Reliability and Safety, New Territories, Hong Kong; vincent.ng@cairs.hk (V.N.); kh.loo@polyu.edu.hk (K.-H.L.)
[2] Department of Electronic and Information Engineering, The Hong Kong Polytechnic University (PolyU), Hung Hom, Hong Kong; talib.faiz@polyu.edu.hk
[3] Key Laboratory of Control of Power Transmission and Conversion, Ministry of Education, Shanghai Jiaotong University, Shanghai 200240, China; mansoor@sjtu.edu.cn
* Correspondence: ali.muhammad@cairs.hk

Abstract: This article presents a novel hybrid three-phase multilevel topology with a hybrid modulation and a control strategy for lower-medium voltage front-end converters. The proposed topology consists of a series arrangement of a three-phase full bridge and a packed U-cell. Each phase leg of the circuit comprises eight active switches and two DC link sources, which are connected to a shared DC bus voltage source, thus generating seven levels of output voltage. The active switches of the proposed topology are categorized based on voltage stresses and controlled using a low-frequency space vector PWM and high-frequency alternative phase opposition disposition PWM techniques. To validate the proposed topology and demonstrate the performance and effectiveness of the hybrid modulation and control schemes, simulations in MATLAB/Simulink and experiments on a custom-designed laboratory prototype have been carried out, and the results are discussed in detail. Moreover, a comprehensive comparison has been conducted among the relevant topologies, which reveals several advantages that include a reduced voltage and a current total harmonic distortion (THD) of 11.28% and 1.76%, respectively, minimized switch loss by 10.3 kW, improved efficiency by 0.26%, and decreased the component count with two levels increased in the output voltage.

Keywords: hybrid medium voltage multilevel converter; hybrid modulation and control; space vector pulse width modulation (SV-PWM); alternative phase opposition disposition pulse width modulation (APOD-PWM)

MSC: 93-05

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1. Introduction

The rise in electrical power demand and the dwindling supplies of nonrenewable energy sources make it essential to use existing resources more efficiently. Power converter technologies are used to adjust the type or level of power according to the load requirement. Among these, low-voltage power converters, which have a wide range of applications, tend to have lower power losses. However, as the voltage level increases, the power losses also increase significantly. Advanced power converter technologies and effective modulation and control strategies are essential to minimize these high power losses.

Considering medium-voltage (MV) converters, they are of great importance, as they exhibit a variety of applications such as MV motor drives [1], MV electric traction [2], utility-scale energy storage [3], and grid-connected renewable energy systems [4]. In MV converters, switching losses constitute a significant portion of the overall converter power losses. These power losses can be minimized by using fewer semiconductor devices or

reducing switching actions, thereby maximizing the converter's output power. Additionally, low harmonic distortions at these converters' input and output terminals are also essential to attain better converter performance. To achieve high efficiency, a classic two-level converter can be considered a practical option for medium-voltage applications based on the fact that it utilizes fewer semiconductor devices. However, the low switching frequency of these medium voltage semiconductor devices presents a challenge in meeting power quality standards, i.e., the harmonic distortions will not be within the permissible range (IEEE-519) [5]. This necessitates a large and costly LC output filter to minimize these harmonic distortions [6]. Researchers have explored alternative solutions, with a primary focus on multilevel converters.

Multilevel converters synthesize an output voltage utilizing several components and DC voltages as inputs. They aim to generate an output voltage waveform that closely resembles a sinusoidal waveform, reduce the stress on electrical components, and improve the system's efficiency. Conventional multilevel converters (MLCs) for MV applications include the neutral point clamped (NPC) converter [7–11], flying capacitor (FC) [7,8,12–14], and cascaded H-bridge (CHB) converters [15–18]. These topologies offer unique advantages, thus making them suitable for different applications based on the required performance characteristics. However, the high number of components used results in these converters' low efficiency and low reliability. Hence, proposing a topology configuration with high-efficiency and high-quality voltage and current waveforms is very important in medium-voltage converter applications [19]. Hybrid converters, which are combinations of conventional multilevel converters, have received great attention from researchers as a potential solution to address the said issues in MLCs, and numerous hybrid topologies for medium-voltage applications have been extensively discussed in the literature [20–26].

A hybrid configuration of an NPC converter with the cascaded H-bridge cell promises significant improvements for medium-voltage applications. Despite its potential benefits, the three-level neutral point clamped converter with a cascaded H-bridge cell suffers from uneven loss distribution, increased control complexity, and protection challenges for the high-stress clamping diodes [27]. The FC-based active neutral point clamped (ANPC) converter [28] is derived from the NPC topology and has similar characteristics with fewer semiconductor devices. Moreover, the ANPC topology overcomes the uneven loss distribution across semiconductor devices by replacing neutral point clamped diodes with active switches. An innovative hybrid neutral point clamped converter (H-NPCC) [29] combines the advantageous operating characteristics of different voltage source converter (VSC) topologies, namely NPC, ANPC, and T-type VSCs. It provides the flexibility to control the system using either a two-level or three-level approach. Compared to typical three-level converters, this converter configuration achieves higher efficiency and overcomes the issue of highly asymmetrical loss distribution under certain operating conditions. Consequently, it significantly increases the converter's output power capability and systems reliability. A new generalized hybrid multilevel converter (HMC) with N-cell T-type modules was presented in [30]. This configuration requires fewer power electronic devices to attain more output voltage levels, thus making it suitable for medium- and high-voltage applications. However, it does increase the component count and complexity associated with balancing the voltage of the DC-link capacitors. The T-type converter (T2C) topology, which has been discussed in [31–33], offers several advantages, including high efficiency and lower component requirements compared to the NPC topology in a two-level converter, as well as enhanced output quality in a three-level converter. In the case that the semiconductor devices fulfill the required breakdown voltage criteria, the T2C presents an appealing option as a substitute for the NPC in the NPC H-bridge topology. This is especially true when conduction losses significantly impact the preceding stage circuit [34]. However, it should be noted that the T2C has less redundancy and imposes greater demands for balancing the DC-link capacitors' voltage. An alternate converter—a modular multilevel converter—is derived by combining the topology with the identical cells discussed in [35].

The control of this converter is quite convenient. However, it requires several DC link capacitors and inductors.

Moreover, the selection of modulation and control schemes greatly influences these converters' overall performance and efficiency. The modulation scheme determines the desired number of switching operations that control the output waveforms of voltage and current and plays a crucial role in managing the converter's efficiency by minimizing the switching losses and THD ratios [36,37]. The modulation schemes employed in the control of MLCs can be categorized as low-frequency switching and high-frequency switching methods based on carrier frequencies. The commonly employed techniques for low-frequency switching are space vector pulse width modulation (SV-PWM) [38–40], selective harmonic elimination PWM (SHE-PWM) [41], and nearest-level control [42] approaches. Although SV-PWM and SHE-PWM are commonly employed in high-frequency switching, sinusoidal PWM (SPWM) is a common approach within this category [36,37,43]. Finite control set model predictive control (FCS-MPC), an advanced control technique, is also seen as a viable option for multilevel converters (MLCs) [44]. Furthermore, the hybrid control strategy, which is based on model predictive control (MPC) to help lower switching losses, has been introduced in [24].

This article presents a novel approach for lower- to medium-voltage front-end converter applications. It introduces a hybrid three-phase multilevel topology with a hybrid modulation and control strategy. The proposed configuration consists of a series arrangement comprising a three-phase full bridge and a packed U-cell, thus generating seven levels of output voltage. Each phase leg of the circuit comprises eight active switches and two DC link sources, which are connected to a shared DC bus voltage source to produce the required voltage levels. The active switches are categorized based on voltage stresses and controlled using suitable switching frequencies, thus employing low-frequency space vector pulse width modulation (SV-PWM) and high-frequency alternative phase opposition disposition pulse width modulation (APOD-PWM) techniques. To validate the proposed topology and demonstrate the performance and effectiveness of the hybrid modulation and control schemes, simulations in MATLAB/Simulink and experiments on a custom-designed laboratory prototype have been carried out, and the results are discussed in detail. This study compares the proposed hybrid multilevel topology with relevant topologies, thus revealing several advantages that indicate the hybrid multilevel converter is a suitable candidate for medium-voltage applications. These advantages include (i) reduced voltage and current total harmonic distortion (THD), (ii) minimized switch loss, (iii) improved efficiency, and (iv) decreased component count with increased output voltage levels.

This article is organized as follows: Section 2 details the proposed topology configuration, including its operating principle and the switched equivalent mathematical expressions. Section 3 elaborates on the hybrid modulation technique employed in the converter. Section 4 addresses the current control technique using synchronous reference frame control. In Section 5, the performance of the proposed converter is validated by simulation and experimental results. A detailed comparative analysis with relevant topologies is presented in Section 6. Finally, this article is concluded in Section 7.

2. Proposed Converter Configuration

The proposed hybrid multilevel converter schematic shown in Figure 1 mainly consists of two parts: a three-phase full bridge and a packed U-cell. The three-phase full bridge consists of three half-legs, with each leg comprised of two alternately connected active switches, i.e., Q_1 and Q_4 (phase A). A main DC bus voltage E is connected in parallel to the three half-legs. As the switches operate alternately, they will produce voltages at the output (Y) having two levels, i.e., ±E. The packed U-cell connected in series consists of six active switches (Q_{lh},Q_{mh}, and Q_{nh} and Q'_{lh}, Q'_{mh}, and Q'_{nh}, respectively) and two DC link sources V_{hdc1} and V_{hdc2} (phases a, b, and c are subscripted as h). The DC links have an equal voltage of $V_{hdc1} = V_{hdc2} = V_{dc} = 0.27E$, which produces a five-level output voltage at the terminal (v_{YZ}), i.e., $\pm 2V_{dc}$, $\pm 1V_{dc}$, and 0. The five levels in the output voltage of the

packed U-cell are ensured by the different switching modes. Also, the packed U-cell has redundancy in the switching state for $\pm 1V_{dc}$ and 0 output voltage levels and has a unique state for $\pm 2V_{dc}$ voltage level, as illustrated in Figure 2.

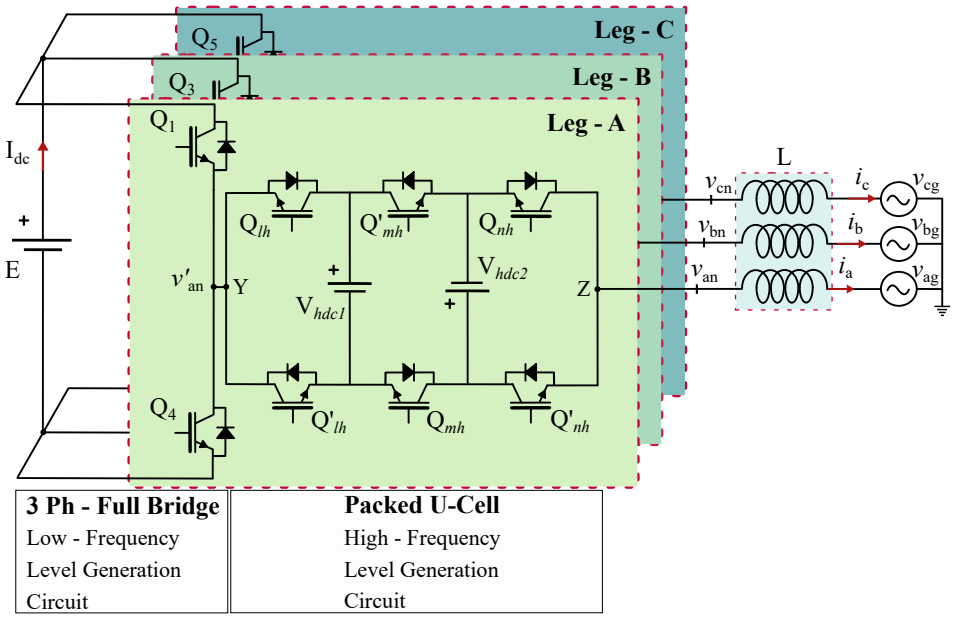

Figure 1. Proposed hybrid MLC circuit configuration.

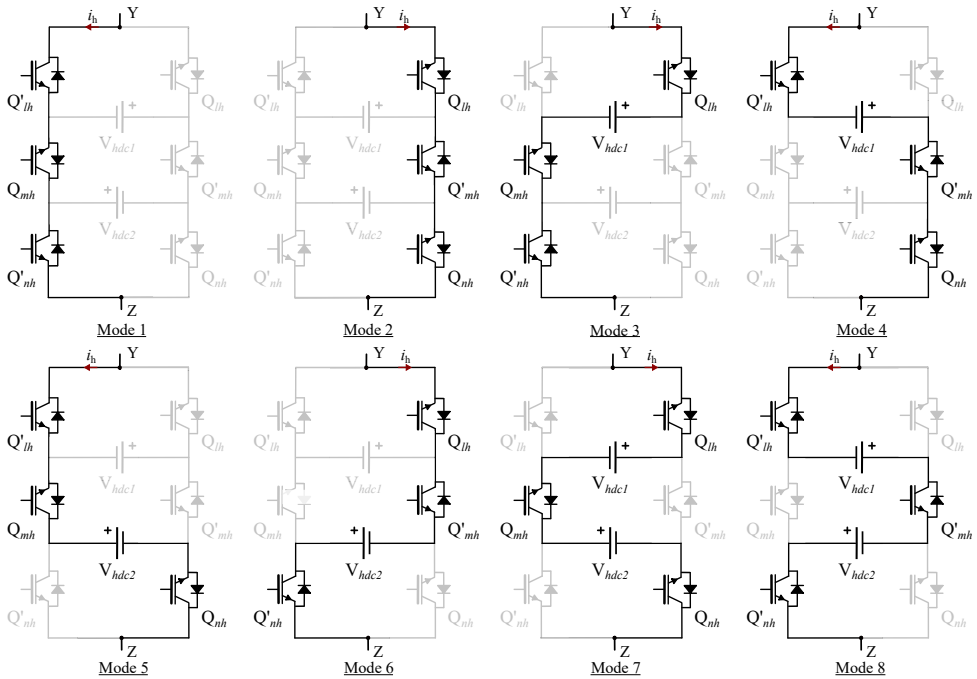

Figure 2. Packed U-cell mode of operations.

A switched equivalent model of the converter realizing the AC-side dynamics depicted in Figure 1 can be equated as Equation (1).

$$\frac{di_h}{dt} = \frac{1}{L}(Q_{xh}V_{hdc1} + Q_{yh}V_{hdc2} \mp Q_z E \pm v_{hg}) \tag{1}$$

where $v_{hg} = V\sin(wt)$ is the 50 Hz grid voltage, Q_z is the switching action and L is the inductor for A phase leg of a three-phase full bridge, whereas Q_{xh} and Q_{yh} are the packed U-cell switching actions (phases a, b, and c are subscripted as h), which are equated as

Equations (2) and (3):

$$Q_{xh} = Q_{lh}Q_{mh} - Q'_{lh}Q'_{mh} \tag{2}$$

$$Q_{yh} = Q_{mh}Q_{nh} - Q'_{mh}Q'_{nh} \tag{3}$$

3. Hybrid Modulation Technique

The selection of a PWM strategy substantially influences switch loss within a given topology. PWM techniques involve approximating the converter output voltage levels based on a reference voltage. This study specifically aims to develop a modulation scheme that optimizes switch operation by considering their voltage stress, thus leading to reduced switching losses. Specifically, switches that handle high voltage stress should operate at a low switching frequency, while switches with lower voltage stress operate at a comparatively higher switching frequency. Therefore, the PWM technique is split into two parts: one for the three-phase full bridge and another for the series-connected packed U-cell. In the three-phase full bridge configuration, where switches endure high voltage stress, operate at low switching frequency, and limit the number of pulses per fundamental cycle. The switches in the packed U-cell are further classified based on their voltage stress, thus distinguishing between the high-voltage switches in the middle leg and the low-voltage switches in the outer leg. These categorizations will be elaborated on in a subsequent Section 3.2.

3.1. Modulation Strategy for Three-ph Full Bridge

Considering the three-phase full bridge shown in Figure 1, the switches bear high voltage stress. Therefore, SV-PWM, as a low-frequency switching modulation technique, is studied. For various switching combinations of a three-phase full bridge, the resulting output active state vectors correspond to vectors V_1–V_6 in the $\alpha\beta$ coordinates, whereas vectors V_0 and V_7, having zero magnitudes, are positioned at the center, as shown in Figure 3. To apply space vector modulation, the first step is to sample a reference signal, denoted as $\vec{V}_{ref}$, at a frequency fs, where Ts represents the sampling period (Ts = 1/fs). The reference signal can be derived from three distinct phase references through the $\alpha\beta$ transform, as expressed by Equations (4)–(8).

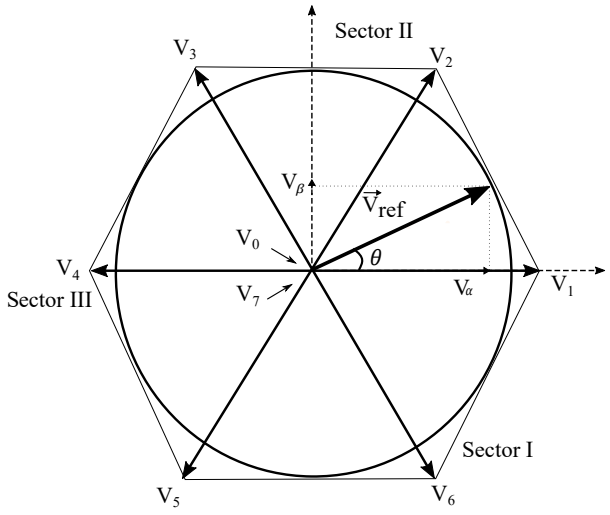

Figure 3. SV-PWM technique for three-phase full bridge circuit.

$$\vec{V}_{ref} = V_\alpha + V_\beta = \frac{2}{3}(V_a + V_b e^{j\frac{2\pi}{3}} + V_c e^{-j\frac{2\pi}{3}}) \tag{4}$$

$$V_\alpha = \frac{2}{3}(V_a + V_b \cos\frac{2\pi}{3} + V_c \cos\frac{2\pi}{3}) \tag{5}$$

$$V_\beta = \frac{2}{3}(V_b \sin\frac{2\pi}{3} - V_c \sin\frac{2\pi}{3}) \tag{6}$$

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{7}$$

$$|\ \vec{V}_{ref}\ | = \sqrt{V_\alpha^2 + V_\beta^2} \tag{8}$$

$$\theta = \tan^{-1}(\frac{V_\beta}{V_\alpha}) \tag{9}$$

where θ is the angular displacement of the reference signal, which can be equated as Equation (9).

Different approaches are available for selecting the order of the vectors and determining which zero vector(s) to utilize. The choice of strategy impacts both the harmonic characteristics and the losses associated with switching. The SV-PWM modulation technique proposed in this study involves dividing the hexagon into three sectors. Within each sector, there are three active vectors. Considering sector I, the active state vectors V_6, V_1, and V_2, and the zero state vectors V_0 and V_7 are applied for a duration of on-time period T_1 and off-time period T_0, respectively. The on-time duration T_1 and the off-time duration T_0 can be expressed in terms of their angle and are given in Equations (10)–(12):

$$T_1 = 120^\circ \times M_f \tag{10}$$

$$T_0 = 120^\circ \times (1 - M_f) \tag{11}$$

$$M_f = \frac{\sqrt{3}|\ \vec{V}_{ref}\ |}{E} \tag{12}$$

where M_f represents the modulation index of a three-phase full bridge, whereas E represents the magnitude of the DC bus voltage. M_f is a key factor in determining the time intervals T_1 and T_0 associated with applying active and zero vectors. Since the fundamental component of a three-phase full bridge remains in phase with the grid voltage, any changes in the M_f will lead to variations in the on-time and off-time durations. Figure 4 depicts pole voltages of the switches (Q_1, Q_3, and Q_5) of the three-phase full bridge at different modulation indexes.

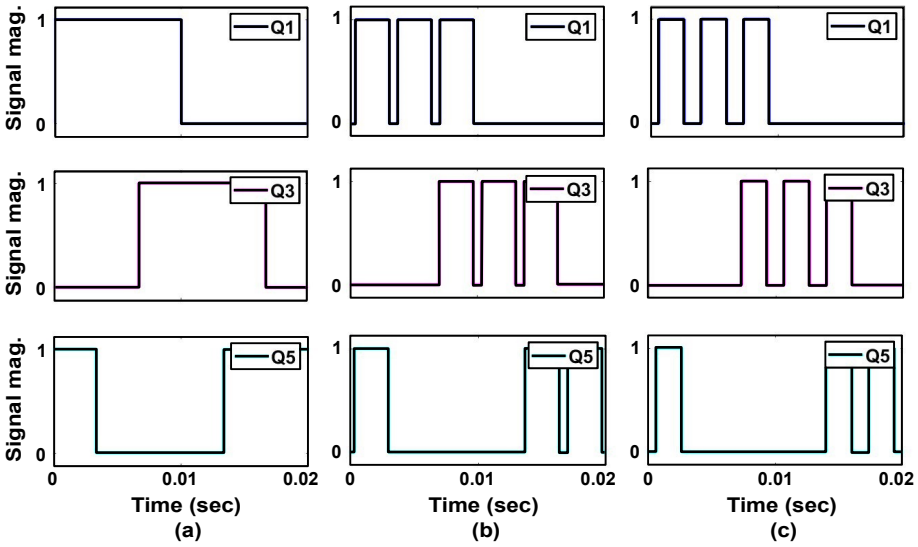

Figure 4. Pole voltages of the switches (Q_1, Q_3, and Q_5) of three-phase full bridge. (**a**) at M_f = 1, (**b**) at M_f = 0.9, and (**c**) at M_f = 0.8.

3.2. Modulation Strategy for Packed U-Cell

Considering the converter's design aspect, the packed U-cell consists of three pairs of active switches that complement each other. These active switches are divided into categories based on the voltage stresses they handle, i.e., high-frequency active switches and low-frequency active switches. The middle complement pair switches in the packed U-cell, namely (Q_{mh} and Q'_{mh}), which experience a high voltage stress of $2V_{dc}$. These switches are operated at a switching frequency of 250 Hz, which helps to minimize switching loss. On the other hand, the outer complement pair switches, namely (Q_{lh}, Q_{nh}, and Q'_{lh}, as well as Q'_{nh}), in the packed U-cell bear a low voltage stress of V_{dc}. As a result, these switches operate at a switching frequency seven times higher than the middle complement pair switches, as depicted in the Figure 5.

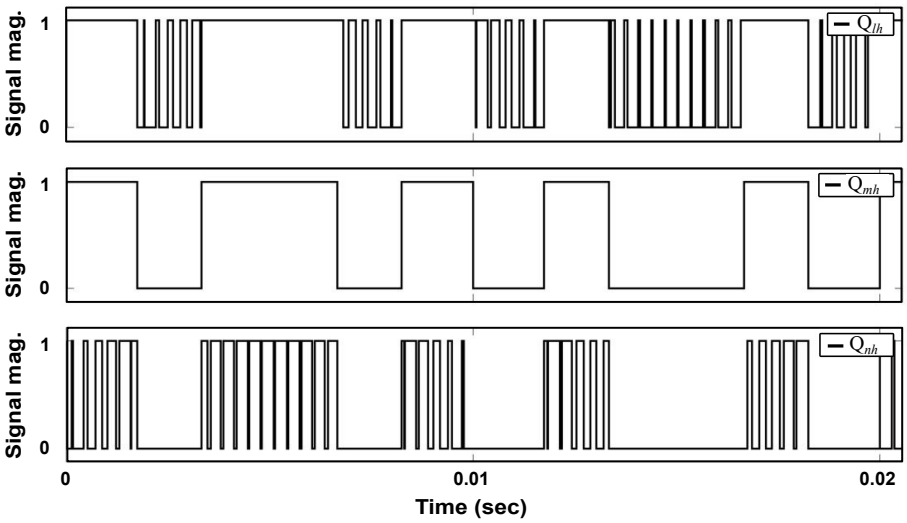

Figure 5. Switching actions for packed U-cell.

For the packed U-cell, an APOD-PWM modulation technique is adopted, as shown in Figure 6, which has an equivalent carrier frequency of 3.2 kHz. This modulation technique is employed to generate voltage levels. However, the effective frequency of the APOD-PWM is 1.6 kHz. This low effective frequency is beneficial, as it helps distribute switch losses more evenly throughout the system.

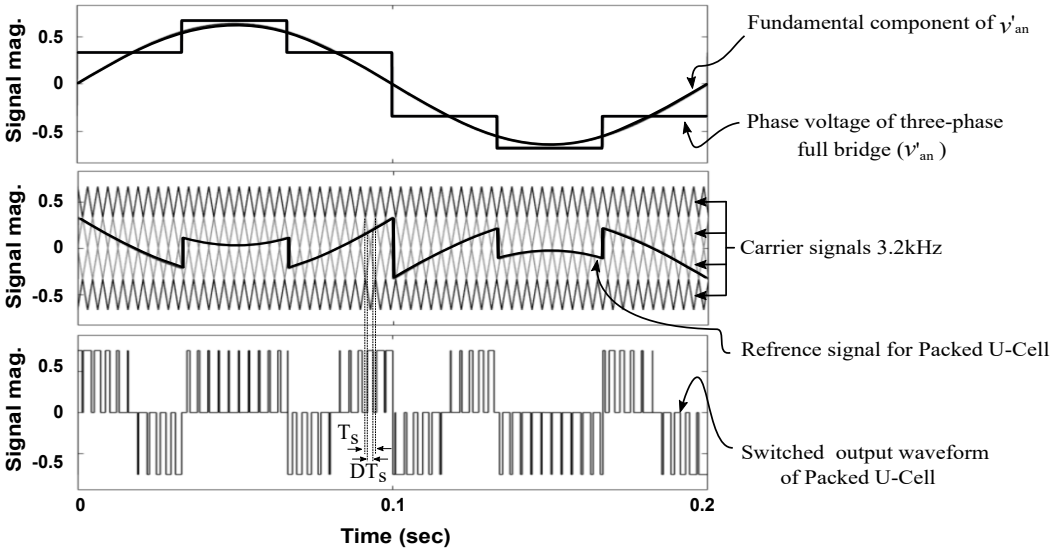

Figure 6. APOD-PWM strategy deployed to packed U-cell converter.

The magnitude of the reference signal has an impact on the output voltage of the packed U-cell. Since the packed U-cell functions as a cascade filter, the reference signal for this module is derived by subtracting its fundamental component from the phase output voltage. In this particular case, a modulation index $M_f = 1$ is assumed for the three-phase full bridge converter. As a result, the packed U-cell's reference signal produces three output voltage levels, which are depicted as the switched output waveform of the packed U-cell in Figure 6.

The mathematical expression of the output *a*-phase leg voltage can be expressed by Equation (13) through Equation (16).

$$v_{an} = v'_{an} - v_{YZ} \tag{13}$$

$$v'_{an} = \frac{4}{3\pi}\mathrm{E}\sum_{r}^{\infty}\frac{1}{r}(\cos(\frac{\pi}{3}r + \theta_f) + M_f)(\sin(r\omega t)) \tag{14}$$

$$v'_{an_{fundamental}} = \frac{4}{3\pi}\mathrm{E}(\cos(\frac{\pi}{3} + \theta_f) + M_f)(\sin(\omega t)) \tag{15}$$

$$v_{YZ} = v'_{an} - v'_{an_{fundamental}} \tag{16}$$

The θ_f value is determined by the T_0 duration of SV-PWM calculated in the three-phase full bridge converter. This off-time interval T_0 is subject to change based on the modulation depth M_f of the three-phase full bridge converter, while r represents harmonic component order.

The output voltage levels of the packed U-cell, with lower DC link voltage requirements for harmonic minimization, will be accommodated within the fundamental converter output voltage. This results in an overall multilevel phase voltage (*a*-phase leg), with a nonuniform voltage step presented in Table 1, and is illustrated by Figure 7.

Table 1. AHMMC converter output phase voltage (v_{an}).

Angle	v_{YZ}	v'_{an}	$v_{an} = v'_{an} - v_{YZ}$
$0 \le \theta \le \theta_1$	V_{dc}	$\frac{1}{3}\mathrm{E}$	$\frac{1}{3}\mathrm{E} - V_{dc}$
$\theta_1 \le \theta \le \theta_2$	$-V_{dc}$	$\frac{1}{3}\mathrm{E}$	$\frac{1}{3}\mathrm{E} + V_{dc}$
$\theta_2 \le \theta \le \pi/2$	V_{dc}	$\frac{2}{3}\mathrm{E}$	$\frac{2}{3}\mathrm{E} - V_{dc}$

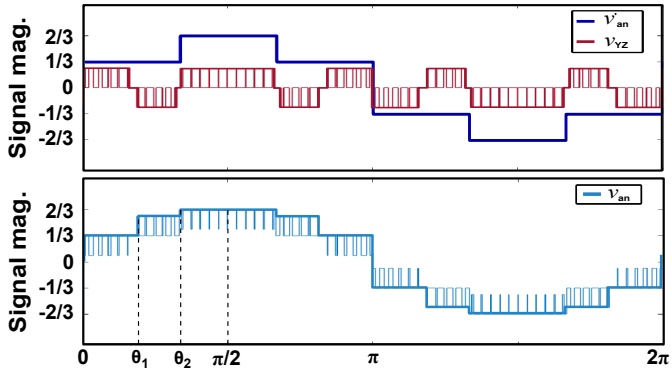

Figure 7. Proposed converter output phase voltage (v_{an}).

3.3. Modulation Range

The maximum output voltage of the packed U-cell, when employing the SV-PWM modulation strategy, is dependent on the modulation index M_f of the three-phase full bridge. The choice of modulation index range significantly impacts the required DC link's voltage for effective harmonic minimization.

When the maximum modulation index M_f is set to 1, the sum of the DC link's voltage, i.e., V_{hdc1}+ V_{hdc2}, must be $(\frac{1}{3})$E, where E is the DC bus voltage. However, if the modulation

index of the fundamental converter is slightly reduced to M_f = 0.95, the total DC link's voltage required for minimizing the harmonics generated by the fundamental converter becomes ($\frac{1}{2}$)E. Figure 8 depicts the sum of the DC link's voltage requirement at different modulation indexes.

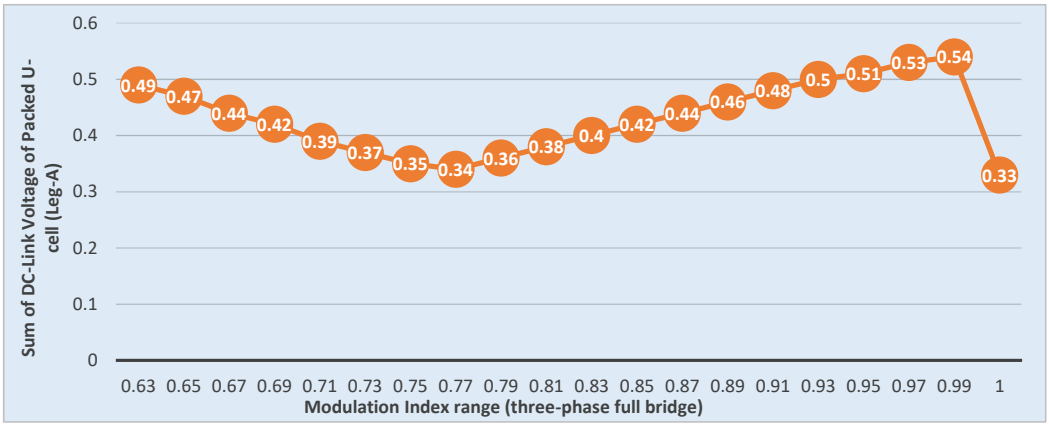

Figure 8. The sum of DC link's voltage requirement at different modulation indexes.

Decreasing the total DC link's voltage requirements for harmonic compensation minimizes the voltage stress on the semiconductor switches. This approach offers an advantage compared to adjusting the switching frequency based on the system design, as it helps to reduce the overall voltage stress on the components.

3.4. Switch Losses

The switch losses of any topology can be categorized into conduction losses and switching power losses. Grouping the total power switch losses P_T by different power converter topologies is a reasonable approach, as it allows for a more detailed and meaningful comparison of the losses across various converter configurations. The proposed topology studied in this paper consists of 24 power switches with antiparallel diodes. The switch loss model has been implemented in the MATLAB–Simulink environment given in [45,46].

The conduction losses P_{cd} in a power converter are determined by the power dissipated through the power switches p_{sw} and their corresponding diodes d. The direction of the current flow plays a crucial role in the calculation of these conduction losses. The P_{cd}, at any given instant across an active power switch (p_{sw}) and its corresponding diode (d), can be calculated using the given Equation (17) through Equation (19).

$$P_{c\_(np_{sw})} = \frac{1}{2\pi}\int_0^{2\pi}\left[(n_{p_{sw}} \times v_{p_{sw}})i_{cond} \cdot Z_l\right]d(\omega t) \tag{17}$$

$$P_{c\_(nd)} = \frac{1}{2\pi}\int_0^{2\pi}\left[(n_d \times v_d)i_{cond} \cdot Z_l\right]d(\omega t) \tag{18}$$

$$P_{cd} = P_{c\_(np_{sw})} + P_{c\_(nd)} \tag{19}$$

where $n_{p_{sw}}$ and n_d are the semiconductor device count, and $v_{p_{sw}}$ and v_d are their associated voltage drops during the conduction state, respectively. whereas, i_{cond} is the conduction current, and Z_l is the switching action of the active switch.

The switching losses of the active switch can be evaluated for each turn-on and turn-off transition that occurs during a reference period. The total switching losses over this reference period can then be determined using the following Equations (20) and (21):

$$P_{sw} = P_{sw\_ON} + P_{sw\_OFF} \tag{20}$$

$$= \sum_{j=1}^{2n+2}\left[\frac{1}{6}v_{x(j)} \cdot i_{cond} \cdot (t_{ON} + t_{OFF})f_{sw(j)}\right] \tag{21}$$

where $v_{x(j)}$ and $f_{sw(j)}$ are the blocking voltage and the switching frequency of the active semiconductor devices, respectively.

The total power switch losses, denoted as P_T, across the power converter can be computed as the sum of the conduction losses P_{cd} and the switching losses P_{sw}, as shown in the following Equation (22):

$$P_T = P_{cd} + P_{sw} \tag{22}$$

3.5. Total Harmonic Distortion

The total harmonic distortion (THD) is defined as the ratio of the equivalent root mean square (RMS) voltage of all the harmonic frequencies (from the 2nd harmonic on) over the RMS voltage of the main frequency of the signal (fundamental frequency) that is calculated using Equation (23).

$$THD = \frac{\sqrt{\sum_{m=2}^{\infty} V_m^2}}{V_f} \tag{23}$$

where V_m and V_f are the RMS voltage values of the m^{th} harmonic and fundamental frequency, respectively. It is important to note that while this equation uses voltage as the parameter, the same mathematical definition can be applied to the current THD as well by replacing the voltage terms with their corresponding current values. The calculation of the voltage THD involves performing a Fourier analysis on the voltage waveform, which determines the magnitudes of the fundamental and harmonic components. The amplitudes of these individual frequency components are determined using the Fourier analysis, as given in Equation (13) through Equation (16). This information is then used to compute the voltage THD using the Equation (23).

4. Control Scheme

This control strategy's main objective is to ensure that the necessary voltage is provided to achieve the desired output current. This control approach operates through two main pathways: the three-phase full bridge, which offers the fundamental component support in the feedforward path, and the packed U-cell, which supports controlling harmonics and achieving fast current response. These pathways are shown in Figure 9. The current control is specifically implemented in the packed U-cell, as these cells deliver high-frequency support. As a result, the system can swiftly react to sudden changes in the grid voltages.

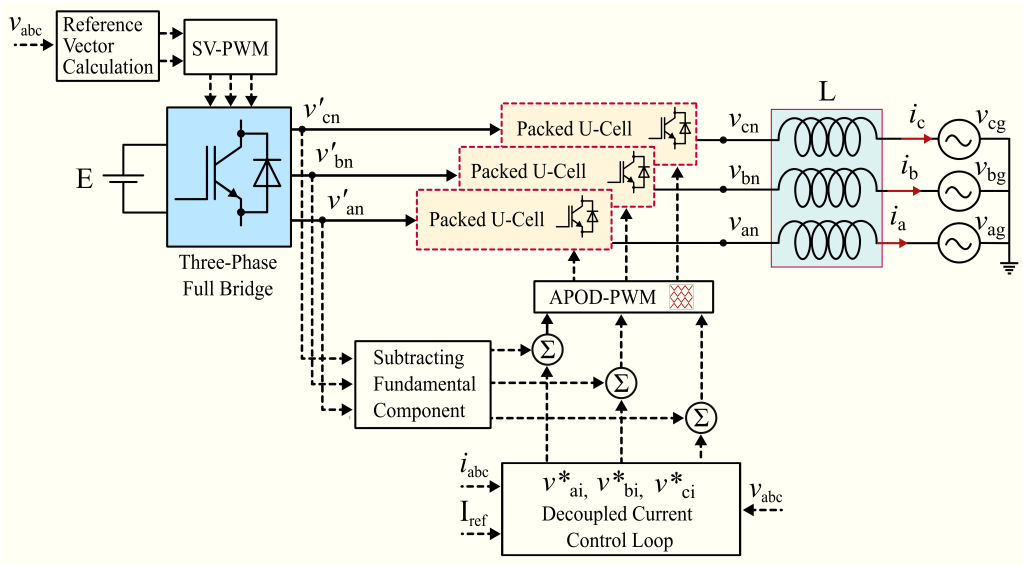

Figure 9. Overall control approach deployed to the proposed converter.

Feedback Control Mechanism

The performance of a converter system is heavily dependent on the effectiveness of its current control. Robust current control is essential to ensure a fast transient response and satisfactory steady state behavior. One widely adopted approach is current control in the synchronous reference frame (SRF), also known as the dq coordinate system [47].

The SRF-based current control offers several attractive features that have made it a popular choice in most pulse-width modulation (PWM) schemes. The dq coordinate transformation allows for the decoupling of the AC current components, thus enabling independent control of the active and reactive power components. This simplifies the design of the current regulators and facilitates the implementation of advanced control algorithms.

Furthermore, the SRF-based current control enables the use of proportional–integral (PI) regulators, which are relatively easy to tune and provide good steady state performance. The transformation to the dq frame also helps mitigate the effects of grid frequency variations, as the control variables become DC quantities in the steady state. Referring to Figure 1, the following current–voltage equation Equation (24) is deduced by ignoring the resistive components.

$$\begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} - \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{24}$$

The Park transformation matrix, given in the reference [48] and expressed as Equation (25) to Equation (27), facilitates the conversion of the three-phase voltage and current into their corresponding d–q components.

$$T_{\mathrm{P}} = \sqrt{\frac{2}{3}}\begin{bmatrix} \sin(\omega t) & \sin(\omega t - \frac{2}{3}\pi) & \sin(\omega t + \frac{2}{3}\pi) \\ \cos(\omega t) & \cos(\omega t - \frac{2}{3}\pi) & \cos(\omega t + \frac{2}{3}\pi) \end{bmatrix} \tag{25}$$

Therefore

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = T_P \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \tag{26}$$

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = T_P \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{27}$$

Given a balanced three-phase condition, when the voltage vector $\vec{V}$g aligns with the d axis, the corresponding v_q component will be zero. Applying the d–q transformation, the active power and reactive power can be expressed as follows:

$$P = \frac{3}{2}\Big[(v_d i_d) + (v_q i_q)\Big] \tag{28}$$

$$Q = \frac{3}{2}\Big[(v_q i_d) - (v_d i_q)\Big] \tag{29}$$

The active power P and reactive power Q can be effectively regulated by independently controlling the i_d and i_q components of the current vector. The current commands I_d^* and I_q^* in the respective axes are expressed by equations (Equation (30)) and (Equation (31)):

$$I_d^* = \frac{p^*}{v_d} \tag{30}$$

$$I_q^* = \frac{q^*}{v_q} = 0 \tag{31}$$

The active and reactive power components are denoted as p^* and q^*, respectively. To ensure system operation at a unity power factor, setting $q^* = 0$ is necessary.

As shown in Figure 10, the active and reactive current references, I_d^* and I_q^*, can be directly derived from the grid's active and reactive power p^* and q^*, respectively. The control loop utilizes the d- and q-axis grid voltage components, v_d and v_q, as well as the filter inductor L.

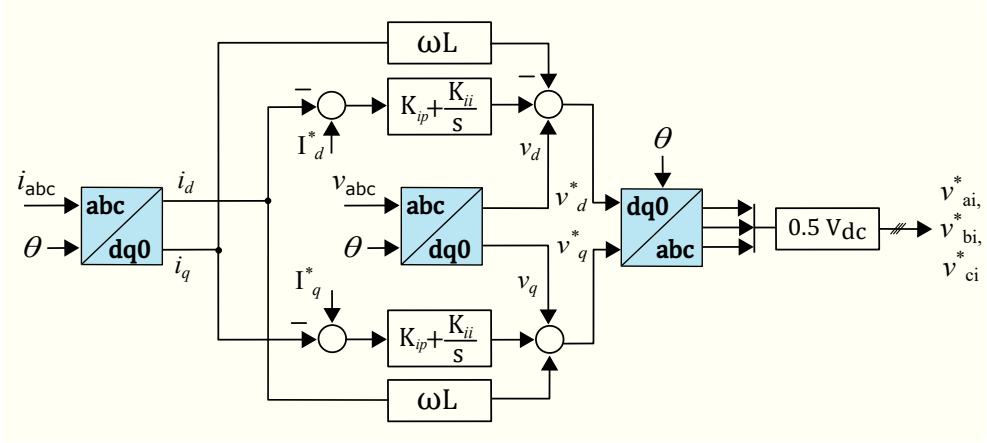

Figure 10. Current control implementation in the stationary frame of reference (d–q transformation).

Based on these input variables, the d- and q-axis voltage references for the system, v_d^* and v_q^*, can be calculated using Equation (32):

$$\begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix} = \begin{bmatrix} v_d \\ 0 \end{bmatrix} + \begin{bmatrix} 0 & -\omega L \\ \omega L & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + K_{ip} \begin{bmatrix} I_d^* - i_d \\ I_q^* - i_q \end{bmatrix} + K_{ii} \int \begin{bmatrix} I_d^* - i_d \\ I_q^* - i_q \end{bmatrix} dt \quad (32)$$

where K_{ip} and K_{ii} are the proportional and integral gain of the current control. The d and q axes are rotating with an angular velocity equal to ω. Control signals v_{ai}^*, v_{bi}^*, and v_{ci}^*, which are attained after inverse d–q to abc transformation, are then utilized to drive the packed U-cell shown in Figure 9.

5. Results and Discussion

5.1. Simulation Results

The study conducted a simulation of the proposed hybrid MLC configuration given in Figure 1, using the MATLAB/Simulink platform. The parameters of the proposed topology configuration are listed in Table 2. The simulation settings were carefully adjusted to ensure consistency between the simulation findings and the experimental results.

Table 2. The proposed hybrid MLC system parameters.

Parameter	Symbol	Value
Inductor	L	0.7 mH
DC-link source	V_{dc}	85 V
Packed U-Cell	PWM_{freq}	3.2 kHz
Grid Voltage (rms)	V_{hg}	110 V
Grid Current (rms)	I_s	10.5 A
DC Source Voltage	E	300 V
3-Ph Full bridge	SW_{freq}	150 Hz

The outer-leg complement pair of switches in the packed U-cell (Q_{lh}, Q_{nh}, and Q'_{lh}, as well as Q'_{nh}) are operated at a switching frequency of 3.2 kHz, thus resulting in an effective switching frequency of 1.6 kHz. This selection of the switching frequency offers several benefits to the hybrid MLC configuration, including reduced current ripple, smaller inductor size, and lower overall system costs, thereby enhancing the system's performance and cost-effectiveness. The considered value for the DC-bus voltage was set to E = 300 V, while the DC link voltage required for harmonic compensation by the packed U-cell was kept slightly higher, i.e., V_{dc} = 85 V. This slight increase in the DC link voltage ensures coverage of the entire range of the modulation index to mitigate the harmonics produced by the three-phase full bridge, as shown in Figure 8.

The Figure 11 depicts the output voltage waveform and its corresponding harmonic spectrum at the maximum modulation index of a single leg (Leg-A) of the proposed converter, as depicted in Figure 1. The terminal voltage v'_{an} of the three-phase full bridge generates a staircase waveform by employing a low switching frequency, which helps to minimize switching losses. However, this results in harmonics that violate the permissible range according to IEEE standard 519. To address the power quality issue, a packed U-cell was used as a cascade filter with a switching frequency of 3.2 kHz. This packed U-cell generates an output voltage v_{YZ} that contains only the harmonics, thus effectively filtering out the unwanted harmonics when added to the three-phase full bridge. As a result, the overall output voltage v_{an} becomes a seven-level output with harmonics that fall within the permissible range specified by the IEEE standard, i.e., an individual harmonic < 5%.

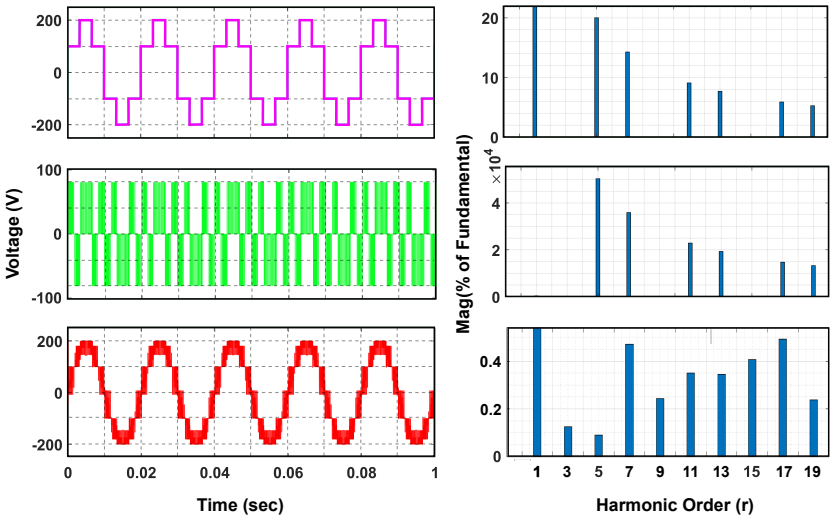

Figure 11. Output voltage waveform and its corresponding harmonic spectrum at M_f = 1.

Figure 12 shows the three-phase multilevel terminal voltage of the proposed converter at a maximum M_f. In Figure Figure 12a, the line voltage is depicted as $v_{L-L} = \sqrt{3}\, v_{an}$, while Figure 12b illustrates the seven-level phase voltage v_{an} of the converter.

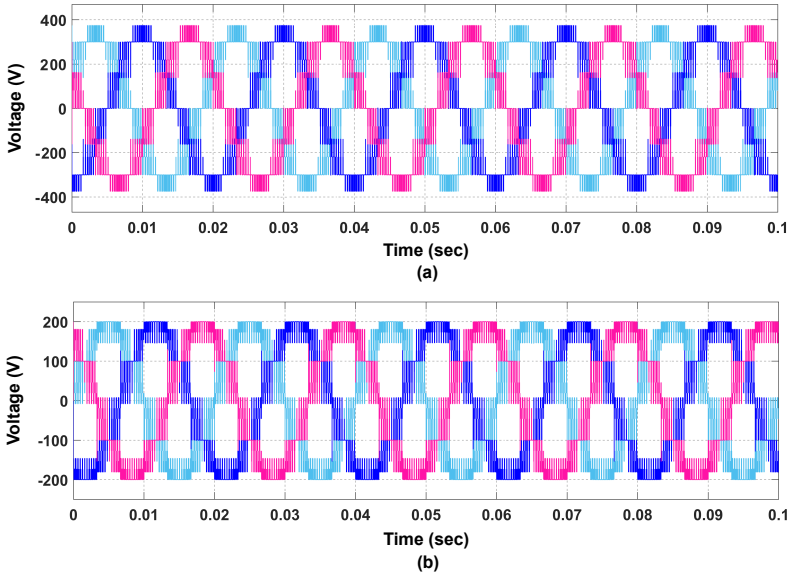

Figure 12. Three-phase multilevel output voltage of the proposed converter at M_f = 1: (**a**) line voltage and (**b**) phase voltage.

Figure 13 shows the three-phase multilevel terminal voltage of the proposed topology at M_f = 0.9. In Figure 13a, the line voltage is given, while Figure 13b shows the phase voltage v_{an} of the converter.

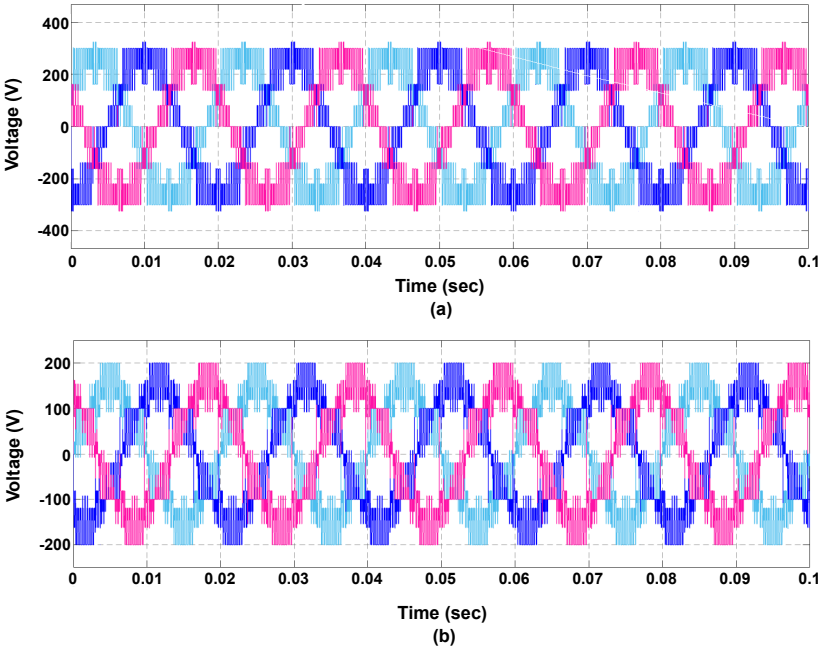

Figure 13. Three-phase multilevel output voltage of the proposed converter at M_f = 0.9: (**a**) line voltage and (**b**) phase voltage.

The proposed converter's output voltage and current waveforms are shown in Figure 14. Figure 14a shows the phase voltages, whereas Figure 14b illustrates the converter's current. It is evident from the waveform that the current control in the dq reference coordinates tracked its reference value as the amplitude varied from 50% to a 100% power rating.

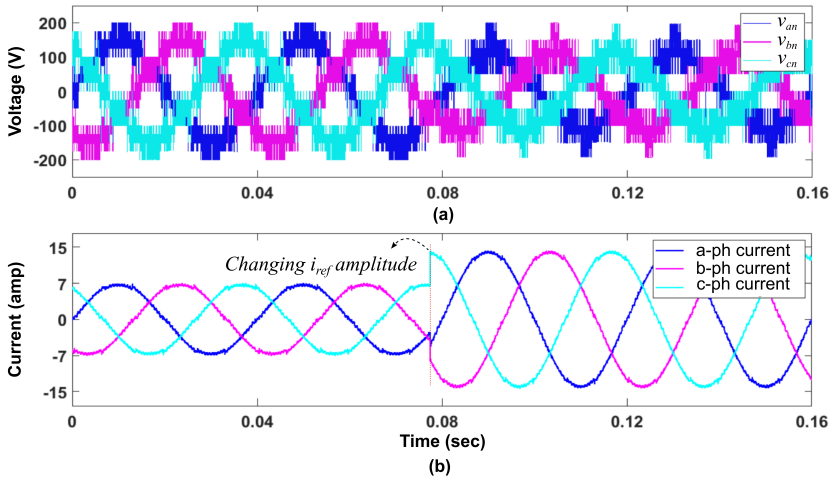

Figure 14. Output voltage and current waveforms of the proposed converter at various power amplitudes: (**a**) Phase voltage waveform. (**b**) Current waveform.

5.2. Experiment Results

As shown in Figure 15, a low-voltage laboratory setup was used to experimentally validate the proposed hybrid MLC topology and its modulation and control strategy. A custom control board was designed and fabricated to realize the control scheme in practice, thus incorporating a control unit (TMS320C28346 Delfino™, by Texas Instruments (Dallas, TX, USA)), a programmable logic device (EPM570 ALTERA®, field-programmable gate array (FPGA) by Altera Corporation (San Jose, CA, USA)), and analog to digital conversion AD7656 by Analog Devices (Norwood, MA, USA). Moreover, a laboratory setup of the proposed converter was constructed, thus consisting of two power boards, with each equipped with six insulated-gate bipolar transistors (IGBTs), as well as voltage and current sensors. The converter was connected to a 110V RMS grid to emulate realistic operating conditions. As detailed in the following section, the experimental findings exhibit a strong agreement with the simulation waveforms.

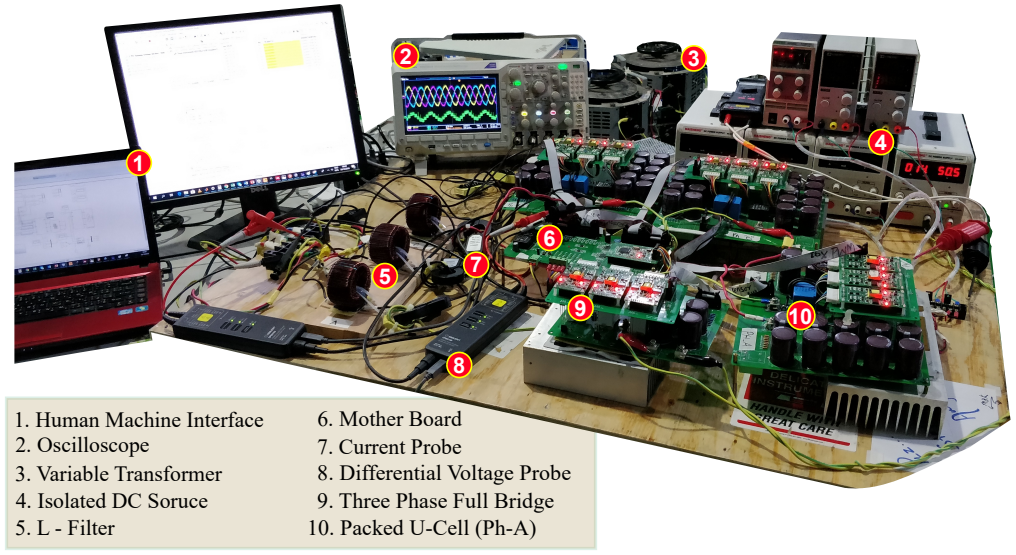

Figure 15. Prototype of the proposed hybrid MLC for experimental validation.

Figure 16 depicts the experimental waveforms of the proposed hybrid MLC (Multilevel Converter). Each waveform is accompanied by its corresponding Fast Fourier Transform (FFT) analysis, which were generated in MATLAB from real-time experimental data. The output voltage of the three-phase full bridge v'_{an} exhibited significant harmonic components due to the low switching of high-voltage stressed switches in a module to

minimize switching losses. However, the harmonics produced by the three-phase converter v_{YZ} were significantly high, which were effectively filtered out by the packed U-cell connected in series. As a result, the overall output voltage v_{an} of the hybrid MLC adheres to the harmonics range specified by IEEE standards.

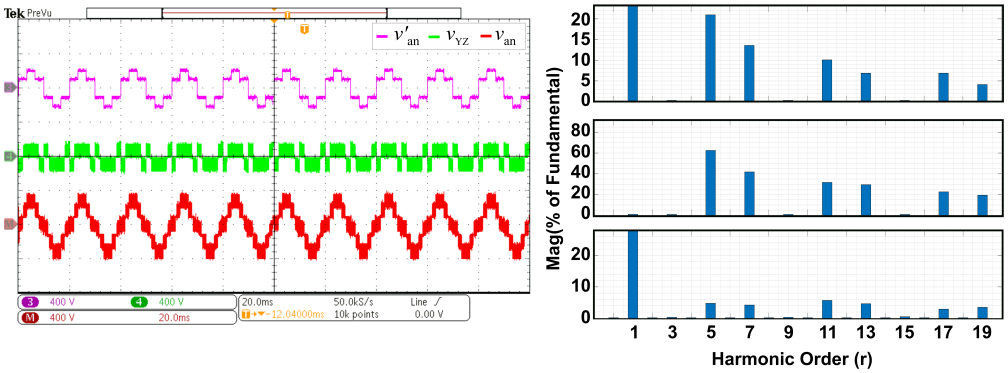

Figure 16. Fast Fourier Transform (FFT) analysis of the experimental waveforms of the proposed hybrid configuration.

Figure 17 illustrates the experimental results of the proposed three-phase hybrid multilevel converter output voltage at a maximum M_f of 1. In Figure 17a, the line voltage waveform is depicted as v_{L-L}= $\sqrt{3}$ v_{an}, while Figure 17b illustrates a seven-level phase voltage waveform v_{an} of the converter. Similarly, Figure 18 shows the experimental results of the proposed three-phase hybrid multilevel converter output voltage at an M_f of 0.9. In Figure 18a, the line voltage is depicted, while Figure 18b illustrates the phase voltage v_{an} of the converter.

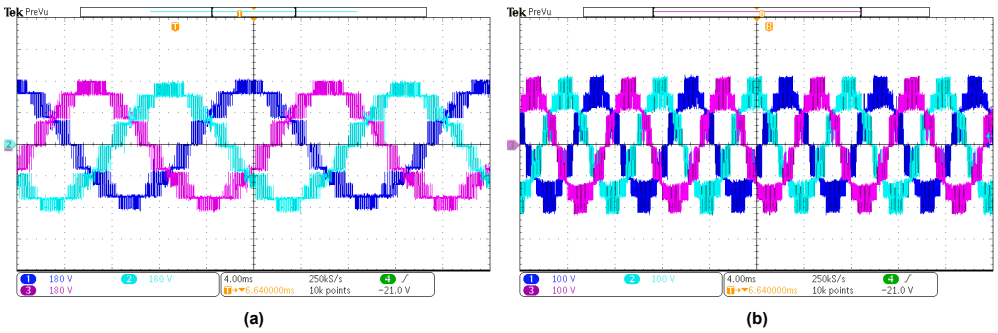

Figure 17. Experimental results of three-phase multilevel output voltage at M_f=1: (**a**) line voltage waveform and (**b**) phase voltage waveform.

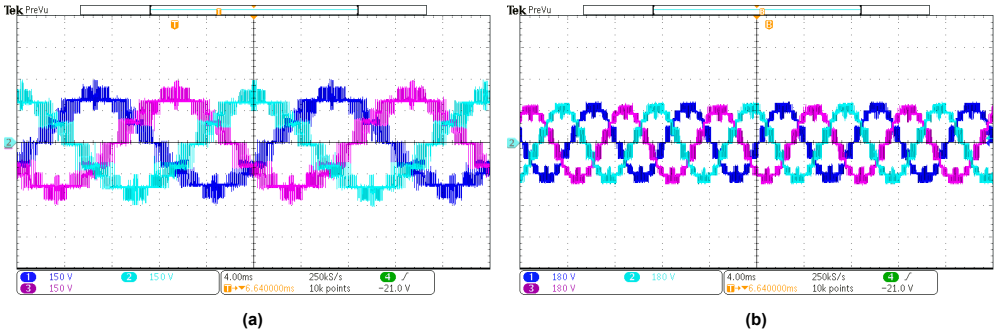

Figure 18. Experimental results of three-phase multilevel output voltage at M_f=0.9: (**a**) line voltage waveform and (**b**) phase voltage waveform.

The proposed converter's experimental terminal voltage waveforms and current waveforms are shown in Figure 19. Figure 19a shows the experimental phase voltage

waveform, whereas Figure 19b illustrates the experimental converter's current waveform. Notably, the experimental waveforms demonstrate that the current control in the dq reference coordinates effectively tracked its reference value as the power amplitude varied from 50% to 100% of the rating. Furthermore, the experimental waveforms closely align with the simulation results, thus indicating a clear match between the two.

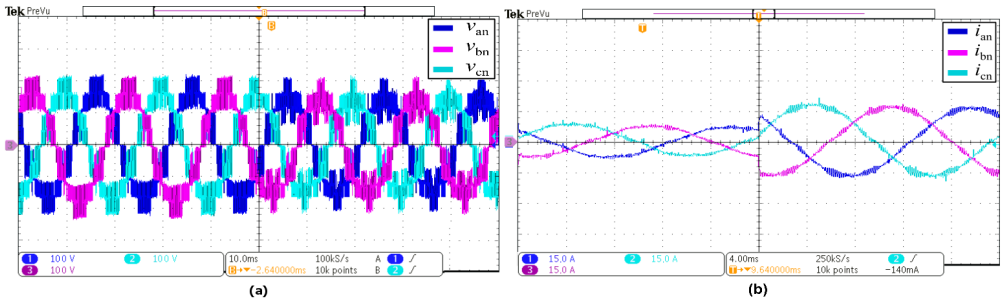

Figure 19. Experimental result of the proposed converter output voltage and current at various power amplitudes: (**a**) Phase voltage waveform. (**b**) Current waveform.

6. Comparative Analysis

Selecting an appropriate topology and the semiconductor components for a specific application is crucial from a technical aspect. Various procedures and comparisons have been carried out [49,50]. For instance, the industrial drives market offers a range of equipment solutions that employ different topologies and semiconductor technologies. Some designs utilize the traditional 3L NPC VSC with IGCTs, while others adopt this approach using IGBTs [49]. This section highlights the proposed converter scheme's performance and efficiency by comparing it with other medium-voltage converters, i.e., the five-level FC-based ANPC and the MMC, which are commercially well known, while other possible and noncommercial configurations are also discussed.

6.1. Comparison Based on Voltage and Current THD

A five-level FC-based ANPC converter [28] utilizing carrier-based PWM has been simulated in MATLAB/Simulink, with the parameters listed in Table 3. It was assumed that the DC link capacitors C1 and C2 and the flying capacitors (C3) were initially charged to 2 kV and 1 kV, respectively. The topology was connected to a common DC bus of 4 kV. For grid-connected applications, a carrier frequency of approximately 3 kHz was used for the carrier-based PWM [51]. The measured phase voltage waveform and its associated harmonic spectrum are shown in Figure 20a. In terms of percentage, the THD of the phase voltage came out to 25.85%. The current control loop, which was composed of the feedforward and the proportional feedback control loop, was deployed. The current THD percentages of 7.67%, 5.13%, and 2.49% were achieved while operating the converter at 25%, 50%, and 100% power ratings, respectively.

The second selected five-level MMC converter discussed in [35] was also analyzed in this study with identical power and voltage conditions under phase shift PWM. The carrier frequency of the phase shift PWM was considered to be 1.6 kHz. The measured phase voltage waveform and its harmonic spectrum are shown in Figure 20b. In terms of percentage, the THD of the phase voltage came out to 33.36% due to the bigger step size. The current THD percentages of 12.6%, 6.11%, and 3.06% were achieved while operating the converter at 25%, 50%, and 100% power ratings, respectively.

Table 3. Simulation model parameters of the converters.

Parameters	Value
Grid Voltage	2.6 kV (rms)
Converter Current	1000 Amp (rms)
DC Bus Voltage	4 kV
DC Link Capacitor C_1, C_2 (FC-ANPC)	2 kV
FCs C_3 (FC-ANPC)	1 kV
Submodule Capacitor (MMC)	2 kV
DC Sources V_{hdc1}, V_{hdc2} (Proposed Hybrid MLC)	0.82 kV
L	0.6 mH
FC-ANPC Converter $freq_{pwm}$	3.2 Hz
Proposed Hybrid MLC $freq_{pwm}$	3.2 Hz
MMC Converter $freq_{pwm}$	1.6 kHz

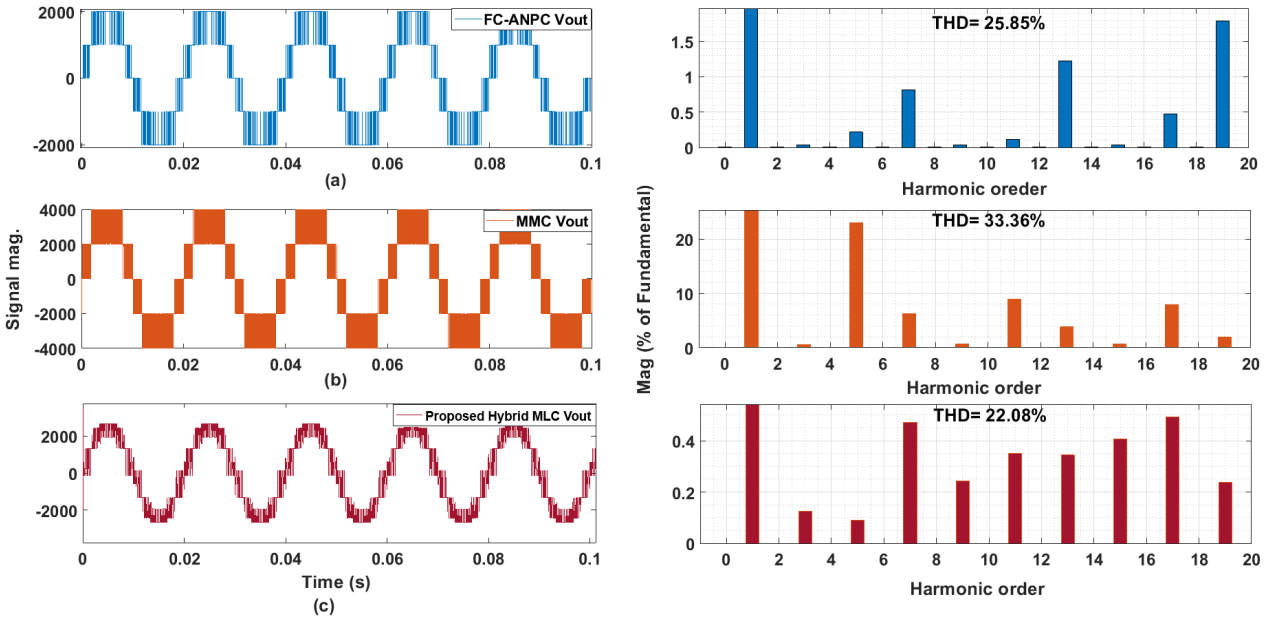

Figure 20. Converters' phase output voltages with their respective harmonic spectrums: (**a**) FC-based ANPC topology. (**b**) MMC topology. (**c**) Proposed hybrid MLC topology.

To evaluate the performance of the proposed converter with similar power conditions, the proposed hybrid MLC topology under the hybrid modulation and control method was simulated in the MATLAB/Simulink environment. The hybrid control strategy implements the APOD-PWM control method with a 3.2 kHz carrier frequency. The measured phase voltage waveform and its harmonic distortion spectrum are shown in Figure 20c. Due to the smaller step size, as discussed in Section 3 and Section 3.2, the percentage THD of the phase voltage came out to 22.08%. The current THD percentages of 5.31%, 2.83% and 1.38% were achieved while operating the converter at 25%, 50%, and 100% power ratings, respectively. The current THD values for the converters mentioned, operating at various power ratings, are provided in Figure 21. This figure illustrates that the proposed hybrid MLC converter exhibited a lower current THD compared to the FC-based ANPC and MMC converter topologies discussed in this study.

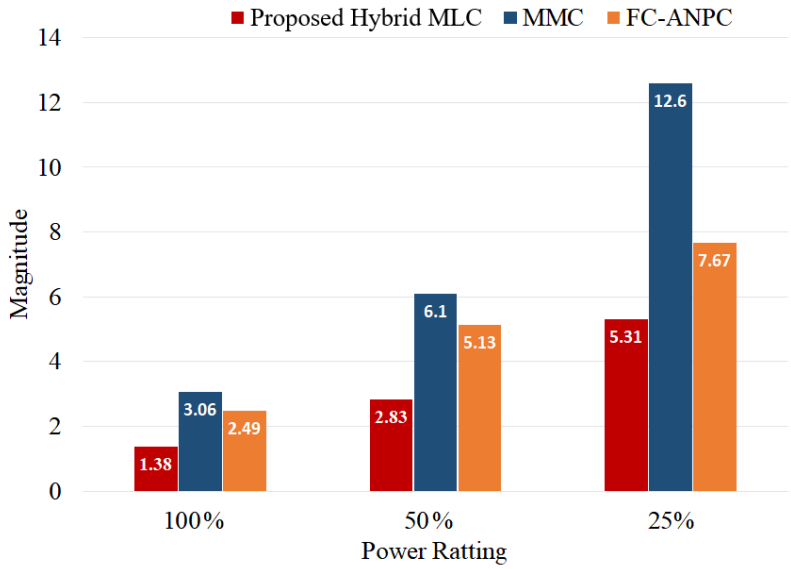

Figure 21. The current THD values of converters operating at various power ratings.

6.2. Comparison Based on Converter Switch Loss and Efficiency

To quantify the feasibility of the proposed hybrid MLC topology, this section will compare the power semiconductor loss and efficiency with the FC-based ANPC and the MMC configurations. The selected topologies were compared using power semiconductor devices available at various voltage levels, as detailed in Table 4. In this study for switch loss calculation, IGCTs were used in the case that the device voltage stress was greater than 2.5 kV due to their lower conduction losses, wherein the maximum power output was fixed at 4 MW. The detailed switch loss model has been implemented in the MATLAB–Simulink environment given in [45,46], with the converter systems parameters listed in Table 3. The power losses associated with semiconductor devices, such as IGCTs, IGBTs, and antiparallel diodes, have been categorized into conduction losses and switching losses.

Table 4. Device selection for semiconductor loss calculation.

Device Type			Stress	Device Number	Device Parameters	
A	IGBT Module	IGBT Diode	820 V	FF1400R12IP4P	1200 V_{CES} 1200 V_{RRM}	2.05 $V_{CE_{sat}}$ 1.85 V_F
B	IGBT Module	IGBT Diode	1000 V	FF1800R17IP5	1700 V_{CES} 1700 V_{RRM}	2.1 $V_{CE_{sat}}$ 1.7 V_F
C	IGBT Module	IGBT Diode	2200 V	FZ1200R33KF2C	3300 V_{CES} 3300 V_{RRM}	4.3 $V_{CE_{sat}}$ 2.8 V_F
D	IGCT		3200 V	5SHY42L6500	4000 V_{DC}	1.8 V_{T0}
	Diode		3200 V	DD1200S45KL3	4500 V_{RRM}	2.5 V_F

NOTE: V_{CES} = collector–emitter voltage; $V_{CE_{sat}}$ = collector to emitter saturation voltage; V_{RRM} = repetitive peak reverse voltage; V_F = forward voltage; V_{T0} = threshold voltage.

The efficiency of any converter topology is determined by the power loss due to semiconductor switches utilized to attain the desired characteristics. The MMC configuration was simulated under phase shift PWM with a 3.2 kHz carrier frequency, thus resulting in an equivalent switching frequency of 1.6 kHz per arm with reduced switch loss. Figure 22 depicts the proposed hybrid MLC's measured switch loss and efficiency, which is compared with the FC-based ANPC and the MMC topologies. It has been observed that the efficiency of the proposed hybrid MLC configuration was marginally reduced (0.06%)

compared to the FC-ANPC and 0.26% higher than the MMC configuration. This indicates the effectiveness of the proposed hybrid MLC topology and confirms it as a viable option for medium-voltage applications.

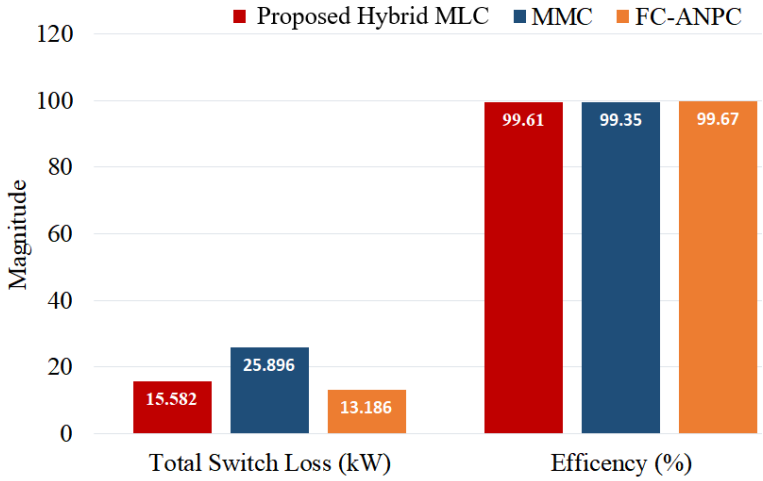

Figure 22. Switch loss and efficiency of converters.

6.3. Comparison Based on Component Count

The overall cost of a converter configuration is determined by the number of components used in its topology. By carefully analyzing the component count associated with different converter topologies, one can make an informed decision about which topology is the most economical for any specific application. Therefore, it is important to consider the converter configuration that achieves more levels in the output voltage while using the fewest components. Table 5 provides information regarding the component counts for each discussed converter configuration in Section 1, along with the corresponding total output voltage levels. In [30,35,52], a higher number of components was used, thus resulting in a five-level voltage. On the other hand, the topology described in [29] employed fewer components but created a three-level voltage; similarly, in [28], they utilized the same number of components but generated a five-level voltage. In contrast, the proposed converter configuration, similar to the topology configuration in [33], utilized the minimum number of components while achieving a seven-level voltage at the terminal.

Table 5. Converter topologies components' count and output voltage levels.

Topology/Leg	Active Switch	Diode	Voltage Source	Inductor	Terminal Voltage Level
H-bridge+NPC [52]	8	2	3	1	5
FC-based ANPC [28]	8	-	3	1	5
H-NPCC [29]	6	2	2	1	3
T-type-HMC [30]	10	-	4	1	5
MMC [35]	8	-	4	2	5
T2C-HB [33]	8	-	3	1	7
Proposed Hybrid MLC	8	-	3	1	7

7. Conclusions

This article introduced an innovative hybrid three-phase multilevel topology and a hybrid modulation and control strategy specifically designed for lower- to medium-voltage front-end converters. The proposed topology configuration combines a packed U-cell in series with a three-phase full bridge that generates seven levels of output voltage. The desired voltage levels were achieved by utilizing eight semiconductor devices and

two DC link sources per leg connected to a common main DC bus voltage. The control of the active switches was optimized by implementing suitable switching frequencies using low-frequency SV-PWM and high-frequency APOD-PWM techniques. Furthermore, a comprehensive comparison with relevant topologies demonstrated that the proposed hybrid topology offered several advantages. These include (i) reduced voltage and current total harmonic distortion (THD), (ii) minimized switch loss, (iii) improved overall efficiency, and (iv) a decreased component count, while achieving increased output voltage levels. The simulation and experimental results from a laboratory prototype were provided, thus confirming the effectiveness of the proposed hybrid MLC configuration and its hybrid modulation and control strategy. The proposed solution is a promising approach to utilize existing energy resources in medium-voltage converter applications efficiently.

Author Contributions: Conceptualization, M.A. and M.M.K.; methodology, M.T.F.; software, M.A. and M.M.K.; validation, M.A. and M.M.K.; formal analysis, M.A. and M.T.F.; investigation, M.T.F.; resources, M.M.K.; data curation, M.A.; writing—original draft preparation, M.A.; writing—review and editing, M.A. and V.N.; visualization, M.T.F. and V.N.; supervision, M.M.K., V.N. and K.-H.L.; writing—review and editing, project administration, funding acquisition, M.M.K., V.N. and K.-H.L. All authors have read and agreed to the published version of the manuscript.

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