RESEARCH ARTICLE | APRIL 11 2008

# Single electron tunneling and Coulomb blockade effect in $Hf\,Al\,O\,/\,Au$ nanocrystals/HfAlO trilayer nonvolatile memory structure

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*Appl. Phys. Lett.* 92, 143117 (2008)
https://doi.org/10.1063/1.2908961

# Single electron tunneling and Coulomb blockade effect in HfAlO/Au nanocrystals/HfAlO trilayer nonvolatile memory structure

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(Received 27 January 2007; accepted 25 March 2008; published online 11 April 2008)

Single electron tunneling and Coulomb blockade effect have been observed in the HfAlO/Au nanocrystals/HfAlO trilayer floating gate nonvolatile memory structure. This trilayer floating gate memory structure exhibits a significant memory window, and resonant tunneling current peaks and Coulomb staircase are obtained at 20 K low temperature. Compared to the ordinary single electron devices, this is the first time that a clear single electron tunneling oscillation has been observed in the floating gate memory structure. This resonant tunneling phenomenon in floating gate memory may open a door toward application as single electron device. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2908961]

Recently, extensive work has been carried out to realize the nonvolatile memory (NVM) devices using metal nanoclusters.[1,2] As the quantum confined structures have potentials to fulfill the demands for small size, low current, and enough on/off voltage gap, many metals such as Au, Ag, Pt, W, and Co are currently under investigation as the potential candidates as the storage node material for NVM.[2,3] On the other hand, according to the Semiconductor Roadmap,[4] the development of the flash memory industry is going to implement high-*k* materials, and a new type of memory made use of single electron device (SED) based on Coulomb blockade effect is coming beyond 2010. The Coulomb blockade effect was first suggested by Gorter in 1951,[5] who explained earlier experiments by van Itterbeck and co-workers. However, it remained unnoticed until 1986, when Averin and Likharev proposed the fabrication of single electron transistor.[6] Later, Fulton and Dolan experimentally confirmed the existence of charging effects in small circuits of planar tunnel junctions.[7] The concept of manipulating the Coulomb blockade effect into memory cell was first proposed in the beginning of the 1990s.[8] From then on, countless experiments have been performed to realize the single electron memory in room temperature.[9–11] From the work of Weinmann *et al.*,[12] in addition of the Coulomb blockade, spin selection rules strongly influence the low temperature transport which can lead to negative differential conductance. In addition, researchers from IBM in the 1970s expected nonlinear conductance in a superlattice, but they only observed a slight decrease in the current as a function of the applied voltage. Later on they developed the idea "resonant tunneling" effect.[13] This effect tells that the tunneling probability depends only on the energy as the tunneling current flows between equal energy states.

Because of spatial confinement and quantum fluctuation, direct study of the electronic state of SED were usually accomplished by conventional scanning tunneling microscope[9] (STM) or fabricating an ultrathin-film transistor with channel and gate lengths in nanometer scale.[10] Since these structures permit the measurements of the energy required for adding successive charge carriers, they can be used to investigate the energy-level spectra of small electronic systems,[11,14,15] which can be considered as a convolution of consequence of random matrix theory[14] and Coulomb blockade effect. Though such measurements are effective means for verifying the Coulomb blockade effect and providing spectroscopic measurement of electronic eigenstates in nanometer-scale metal particles, the application on large scale application in flash memory by SED is being hindered since the use of STM or electron-lithography to fabricate SEDs one by one is time consuming and incompatible with current technology.

In this letter, we report unusual current-voltage characteristics in the floating gate memory structure, which contains numerous Au nanocrystals (NCs) embedded in HfAlO dielectric layer, where Coulomb blockade staircase and single electron tunneling oscillations have also been observed. In the latter session, we propose an explanation based on the understanding in the Coulomb blockade effect and resonant tunneling for correlated electrons.

Au NCs embedded HfAlO/Au NCs/HfAlO trilayer structure on Si substrate was fabricated by pulsed-laser deposition at 550 °C with 2.0 Pa of oxygen partial pressure. Structural characteristic of this trilayer structure was characterized by means of high-resolution transmission electron microscopy (HRTEM), and the memory effect in the Au NCs embedded capacitors were characterized by capacitance voltage (*C-V*) measurements by Agilent 4294A impedance analyzer. Apart from conventional electrical characterization of floating gate memory, this structure has also been put into low temperature for electron tunneling characterization.[2]

From Fig. 1, the HfAlO/Au NCs/HfAlO trilayer structure on *p*-Si substrate can be clearly seen. The Au NCs are uniformly distributed between the HfAlO control layer and the tunnel layer. The thicknesses of the tunnel layer and the control layer are about 15 and 20 nm, respectively. The interface between the HfAlO tunnel layer and the silicon substrate is mainly due to the oxygen diffusion into the sample after postdeposition annealing. The inset shows the plane-view TEM image of the trilayer structure, which can be seen that the self-organized and uniformly distributed Au NCs are spherical in shape, where the range of diameter of Au NCs is from 3 to 4 nm, with the density of about $1.6\times10^{12}$ cm$^{-2}$.

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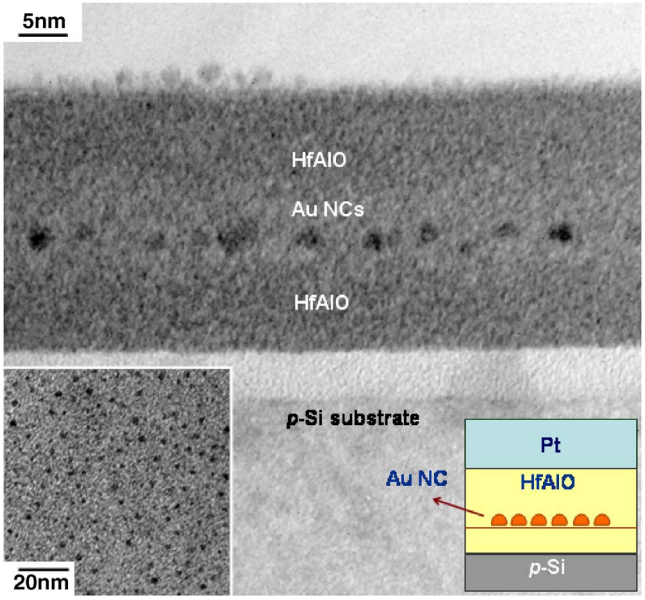


FIG. 1. (Color online) Cross-sectional HRTEM image of the trilayer floating gate memory structure, where Au NCs are evenly distributed in HfAlO matrix. The inset shows the plane-view HRTEM image of the Au NCs.

Figure 2 shows the typical high-frequency (1 MHz) capacitance-voltage (*C-V*) curves measured at room temperature from the trilayer structure with Au NCs. The *C-V* relations were obtained with gate voltage swept from accumulation to inversion and reverse at room temperature. The counterclockwise loops are resulted from the substrate injection of charges into the NCs.[16] As the control sample without Au NCs shows a negligible *C-V* hysteresis loop, it is assumed that the influence of oxide trap charges or mobile ions is negligible in the following discussion. As calculated from equations proposed by Tiwari *et al.*[1] and Kim *et al.*,[17] during the sweeping from −12 to 12 V, the corresponding stored charge density is $3.0\times10^{13}$ cm$^{-2}$, which is enough for the potential application as NVM.

Figure 3 shows the *I-V* curves of the capacitor structure (with and without Au NCs) at positive bias (i.e., "write" state) and at different temperatures of 20 and 50 K. Coulomb blockade effect can be observed in the trilayer structure in

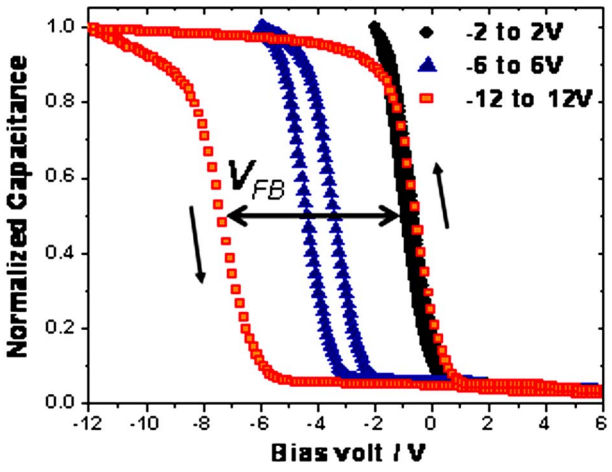


FIG. 2. (Color online) *C-V* hysteresis loops of the trilayer structure. The flat band voltage shift ($V_{FB}$) as indicated is 3.08 V, corresponding to the stored charge density of $3.0\times10^{13}$ cm$^{-2}$.

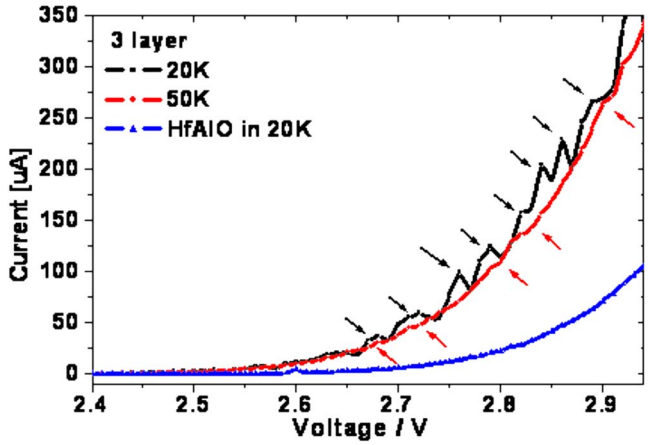


FIG. 3. (Color online) *I-V* curves at 20 and 50 K, showing the steps and the peaks in conductance. For the control layer, with only HfAlO, there are no steps or peaks that can be observed.

the figure, indicated by the periodically modulated current as the bias voltage increases. It is apparent that the curve of the control layer (without Au NCs) does not show any steps in the *I-V* curve, suggesting that the Au NCs are responsible for the Coulomb blockade effect. From the *I-V* curve at 20 K, an average Coulomb voltage can be determined as $\Delta V=31$ mV which corresponds to the Coulomb capacitance $C=5.1$ aF from $\Delta V=e/C$. It is interesting to notice that peaks instead of flat steps are observed in the *I-V* curves as shown in Fig. 3. We believe that it is due to the interplay of resonant tunneling and Coulomb blockade effect. To understand this phenomenon, an analytical calculation has been carried out based on a nearly free electron model.[15]

In the analytical calculation, the volume of the nanoclusters can be calculated by assuming that each nanocluster is aggregated into a hemisphere, therefore, $V=(2\pi/3)r^3$, where $r$ is the radius of Au NCs. The estimated number of atoms is in the order of $10^3$, which is calculated from $V/(a^3/4)$, where $a$ is the lattice parameter of Au that equals to 4.08 Å.[18] By directly applying the nearly free electron model,[15] the mean spacing of independent-electron spin-degenerated energy levels was estimated by

$$\delta E \sim \frac{2\pi^2\hbar^2}{mk_FV},$$

where $m$ is the electron mass and $k_F$ is the Fermi wavevector ($1.20\times10^8$ cm$^{-1}$ for Au).[18] With the mean size of Au NCs of 3.5 nm, the estimated mean level spacing is 2.9 meV. With this 2.9 meV mean level spacing in the Au NCs to be larger than thermal energies $k_BT$ and therefore experimentally resolvable, a simple estimation shows that the measurement must be carried out under 23 K. In our measurement, we can only observe resonant tunneling and Coulomb blockade effect at 20 K, as shown in Fig. 3. It is apparent that there are still tunneling current peaks that appear when the temperature is at 50 K and those peaks can be correlated to those observed at 20 K. However, some peaks are missing because the Coulomb blockade effect is more difficult to be observed as the quantum fluctuation $kT$ increases. It is observed that the tunneling current of the *I-V* curve at 20 K is larger than that at 50 K since the tunneling process becomes more feasible when temperature decreases.

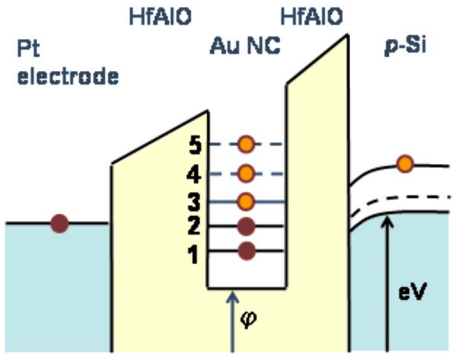


FIG. 4. (Color online) Schematic potential landscape of the trilayer structure. The 0D states in Au NC are denoted by levels 1–5.

To further discuss about the tunneling process when the zero-dimensional (0D) states in the Au NCs are on resonance, we assume that all the free electrons in Au NCs are at the same quantum state at low temperature during measurements, i.e., coherent transmission,[19] and exclude all the stray resistance. Resonant tunneling through the Au NCs, which behave as 0D quantum dot, is illustrated in the schematic potential landscape in Fig. 4, which is based on the argument provided by van der Vaart *et al.*[20] The figure shows a few of the 0D states in the dot and the electrostatic potential is tuned in order that the electron has sufficient energy to overcome the charging energy between Au and Si. The finite bias voltage $V$ gives an electron three choices to tunnel into, i.e., either one of the unoccupied levels 5, 4, or 3. This tunneling increases the electrostatic potential $\varphi$ by the charging energy, and when the incoming electron relaxes to the ground state (level 3), it can tunnel via the level 3 to the Pt electrode. The current through the dot is resonantly enhanced only when the two 0D states in the dot and the $p$-Si match with energy, so the staircases appear in discrete voltages.

In summary, resonant oscillations and Coulomb blockade have been observed in HfAlO/Au NCs/HfAlO trilayer memory structure. Since this process is a convolution of Coulomb blockade effect and the trilayer floating gate structure, the $I$-$V$ characteristics are different from the ordinary single electron tunneling inside quantum well. In addition, this single electron resonant tunneling effect suggests that a floating gate memory can be used as a SED.

The authors gratefully acknowledge Dr. F. G. Shin for his helpful conversation and gratitude goes to Dr. Y. W. Wong and Dr. Y. Fan for their technical support. This work was supported by the Hong Kong Research Grant Council (No. PolyU 5006/04P).

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