RESEARCH ARTICLE | JUNE 03 2008

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Appl. Phys. Lett. 92, 223105 (2008)
https://doi.org/10.1063/1.2936847

Study of tunneling mechanism of Au nanocrystals in HfAlO matrix as floating gate memory

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(Received 17 December 2007; accepted 4 May 2008; published online 3 June 2008)

A floating gate memory structure containing HfAlO control gate, self-organized Au nanocrystals (NCs), and a HfAlO tunnel layer has been fabricated by pulsed-laser deposition. Owing to the charging effects of Au NCs, a significant threshold voltage shift has been obtained and the memory window up to 10.0 V and stored charge density up to $1\times10^{14}/\mathrm{cm}^2$ has been achieved. Fowler–Nordheim tunneling mechanism is used to analyze the capacitance-voltage characteristics of the trilayer memory structure, and it is found that higher density and smaller size of the Au NCs result in a higher tunneling coefficient and a larger memory window. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2936847]

Due to strong demands for increasing information storage, nonvolatile memory devices have emerged to attract a great deal of attention and extensive research has been carried out to realize the nonvolatile memory (NVM) using metal nanocrystals (NCs).[1,2] As the quantum confined structures have potentials to fulfill the demands for small size, low current, and enough on/off voltage gap, many metals, such as Au, Ag, Pt, Ni, Co, etc. are currently under investigation as a potential candidate as the storage node material for NVM.[2,3] Among the reported metals being studied as storage nodes, Au is chosen because of several reasons.[4,5] For instance, it is chemically more stable compared to other metals, yet the energy perturbation is smaller.[3] In addition, the relatively large work function of Au NCs makes a deep quantum well between the control oxide and tunnel oxide, which is desirable as the floating gate for charge trapping. It can also enhance the process of Fowler–Nordheim (F-N) tunneling which is the major mechanism for write.[6,7] For erase, even direct tunneling is more sensitive to the barrier width than the barrier height. Using Au NCs could reduce the leakage current by two to four order of magnitudes.[3]

The motivation for integrating the Au NCs with HfAlO is its potential for implementation in the advanced complementary metal-oxide-semiconductor technology with high-*k* gate dielectrics. HfAlO is chosen as the tunnel and control layers, owing to its good thermal stability[8] and large potential for high-*k* gate dielectrics, and also its unique band asymmetry in the programing and retention modes.[9] In addition, the crystallized nature of HfO_2 makes it difficult to identify the Au NCs. Thus, in this letter we only report the result with HfAlO dielectric as the tunneling and control layers.

There has been a lot of work on the formation and electrical properties of Au NCs,[2,4,9] and there is also plenty of research on the write/erase mechanisms where Au NCs are used as floating gate memory nodes.[10,11] However, there is not much emphasis being put on comparing the experimental results of memory characterizations with the F-N tunneling mechanisms, and hence optimizing the formation of the Au NCs in the trilayer floating gate memory. In fact, the tunneling mechanism is not well addressed yet in such floating gate memory system. In this letter, we investigate the effect of tunneling probability on the charge into the Au NCs by different biasing voltages.

In this study, HfAlO/Au NCs/HfAlO trilayer structure on the *p*-type Si wafer was fabricated by pulsed-laser deposition (PLD) followed by postdeposition thermal annealing. After it was etched by HF acid, approximately 15 nm thick HfAlO layer as a tunneling oxide was deposited by PLD at 550 °C; while the laser fluence used was $5\ \mathrm{J/cm}^2$. Then a very thin layer of Au NCs was deposited, and finally about 30 nm thick HfAlO layer as control oxide was sequentially deposited. Au NCs are formed by PLD owing to the collision of Au atoms with Ar atoms where 6 Pa Ar gas pressure has been used. The quenching effect and relatively low substrate temperature results in the formation of Au NCs instead of Au thin films. Different Au growth temperatures (300 and 550 °C) have been used. The samples were finally annealed at 850 °C for 30 min in N_2 ambient, and Pt dot electrodes with a diameter of 200 μm were subsequently deposited. The trilayer structure was investigated by high-resolution transmission electron microscope (HRTEM), and the memory characteristics of Au NCs embedded capacitors were characterized by capacitance-voltage (*C-V*) measurement with HP4294A.

Figure 1(a) shows cross-sectional TEM image of the HfAlO/Au NCs/HfAlO trilayer structure on *p*-Si substrate. One can see that the Au NCs are uniformly distributed between the HfAlO control layer and the tunnel layer. The thicknesses of the tunnel layer and the control layer are about 15 and 30 nm, respectively. The interface between the HfAlO tunnel layer and the silicon substrate is mainly due to the oxygen diffusion into the sample after postdeposition annealing. Different condition deposited Au NCs show negligible difference in the cross-sectional TEM images, so we only show one typical TEM image here. Figures 1(b) and 1(c) are the plane-view TEM images of samples with Au NCs deposited at 300 and 500 °C, respectively. It is apparent that most of the Au NCs are spherical in shape and their mean diameters are 4 and 6 nm, with the density of 4.0×10^{12} and $1.6\times10^{12}\ \mathrm{cm}^{-2}$, respectively.

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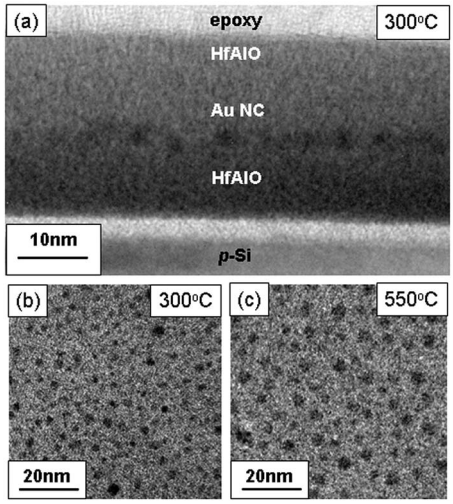

FIG. 1. (a) Cross-sectional HRTEM image analysis of trilayer nonvolatile memory structure with Au NCs embedded in the HfAlO and plane-view TEM images of samples with Au NC fabricated at (b) 300° C and (c) 550° C.

Figure 2 shows the high-frequency (1 MHz) *C-V* curves measured from the trilayer structure grown at different conditions. The *C-V* relations were obtained at room temperature with gate voltage swept from accumulation to inversion and then reverse with an ac oscillation level of 500 mV. The counterclockwise loops are resulted from the substrate injection of charges into the NCs.[6,11] From the figure, the storage charge density could be calculated based on the formula given by Tiwari[1] and Kim *et al.*[12] The largest flatband voltage shift (ΔV_{FB}) obtained is larger than 10.0 V, corresponding to the stored charge density up to 1×10^{14} cm^{-2}, which is one of the largest values that have ever been reported. As the control sample without Au NCs shows a negligible *C-V* hysteresis loop, it is assumed that the influence of oxide trap charges or mobile ions is negligible in the following discussion.

From the *C-V* curves of the two samples, we found that a relatively lower growth temperature (300 °C) of NCs results in a larger memory window. This can be interpreted that higher temperature (550 °C) increases the surface mobility, and the formation of larger Au NCs would be more favorable. As the cluster size increases, the density decreases and therefore there may be fewer charges being stored. In addition, the *C-V* loops are less shifted to the negative direction compared to the control sample, suggesting that the electrons

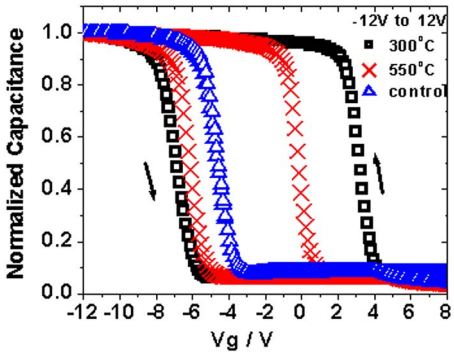

FIG. 2. (Color online) *C-V* hysteresis of the trilayer nonvolatile memory structure under +12 gate voltage operation with Au NCs embedded in the HfAlO fabricated at 300 and 550° C, and control sample.

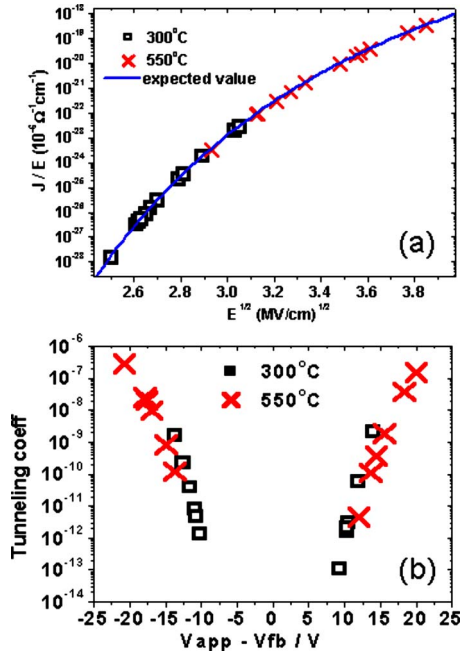

FIG. 3. (Color online) (a) Tunneling coefficients against applied voltage during erase (negative applied voltage) and write (positive applied voltage) of the trilayer memory structure with Au NCs embedded in the HfAlO fabricated at 300 and 550° C. (b) F-N plots of experimental (symbols) and calculated (line) currents using a barrier height between HfAlO and Au.

are injected to the Au NCs during writing, and the effect of holes injection is minimized.

Figure 3(a) shows the F-N plots of experimental (symbols) and calculated (line) currents using a barrier height between HfAlO and Au. It can be seen the high voltage assisted tunneling process, obtained from experimental results, fits the calculated values well and this proves that the tunneling mechanism in this structure is mainly by F-N. Figure 3(b) shows the relation between the tunneling coefficient and voltage (*T-E*). One can see that the curves are basically symmetrical with "positive" and "negative" electric field, where the positive and negative represent different polarizations of the electric fields. From Fig. 3(b), it can also be seen that the slopes for the two curves are different, suggesting that although Au NCs are used in both structures, the values of effective mass and energy barrier height may be different. The reason is that as the thickness of the HfAlO varies from sample to sample, the effective mass of the electrons are different. Also, as the sizes and densities of the Au NCs are different as seen from the plane-view TEM images, the value of energy barrier height varies as well due to the size-related quantum confinement and Coulomb blockade effects.

Since there has been plenty of discussions about how to obtain the F-N tunneling equation,[13,14] the derivation of the F-N tunneling equation is only briefly introduced here. In order to find the tunneling probability by an easier approach, only the barrier height measured between the Fermi surface and the conduction band of the dielectric is considered; while the misalignment of the dielectric due to the metal electrodes is excluded (refer to Fig. 4).[15] It is assumed that the floating gate layer can provide enough available states so that electrons can tunnel in or out of the dielectric completely. From time independent Schrödinger equation and Wentzel–Kramers–Brillouin approximation,[13] tunneling probability can be obtained as

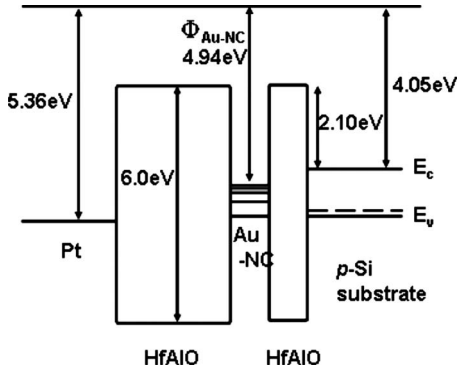

FIG. 4. Energy band diagram schematic of nanofloating gate structure with Au NCs and HfAlO at flatband condition.

$$T = \frac{\Psi(L)\Psi^*(L)}{\Psi(0)\Psi^*(0)} = \exp\left(-\frac{4}{3}\frac{\sqrt{2qm^*}}{\hbar}\frac{\phi_B^{3/2}}{E}\right),$$

where ϕ_B is the barrier height measured from the Fermi surface in the metal to the conduction band of the dielectric (refer to Fig. 4); while in the electric field $E=\phi_B/L=(V_{app}-V_{fb})/t_{ox}$, V_{app} and V_{fb} are the applied voltage and flatband voltage shift, respectively.

From this equation, it is apparent that the tunneling coefficient exponentially depends on the electric field with a relation of $E=b/\ln T$, where b is a constant which is a function of ϕ_B. This equation implicitly tells that the tunneling coefficient depends on the electron effective mass (m^*), the geometrical property (t_{ox}) of dielectric layer, and the intrinsic property of the metal NCs (ϕ_B). Though the tunneling coefficient seems to be independent of the geometrical property of the Au NCs, in which the geometrical properties are usually governed by the growth condition, the change in size and density of the Au NCs may lead to the change of ϕ_B due to the quantum confinement and Coulomb blockade effects.

In order to investigate the retention characteristic of this memory floating gate structure, the memory capacitors were first charged for 20 s at a bias voltage of 10 V. Then, the capacitance decay measurements were carried out at flat band bias voltages of zero and 3 V, respectively, for the samples with Au NCs deposited at 300 and 550 °C. The normalized capacitance-time (C-t) curves are shown in Fig. 5. One can see that after 10^4 s of stress, the decayed capacitance for the memory capacitor with Au NCs deposited at 500 °C is only 10%, suggesting very good charge retention characteristic. However, for the sample with Au NCs fabricated at 300 °C, the drop in capacitance after 10^4 s of stress is about 25%. We believe that the possible reasons for this difference in retention are due to the lateral channel leakage mechanism, proposed by Kim *et al.*[12] and the Coulomb repulsion in NCs, proposed by Winkler *et al.*[16] From the plane-view TEM images, we can see that the mean distance in the NCs deposited in 300 °C are shorter, leading to relatively larger leakage from lateral channel formed by Au NCs. In addition, the smaller Au NC size in this sample

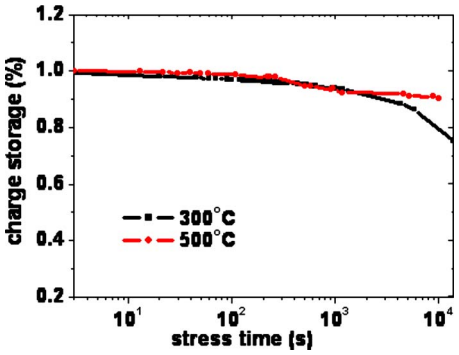

FIG. 5. (Color online) Normalized capacitance decay characteristics for samples with Au NCs fabricated at 300 and 500° C.

results in relatively stronger quantum confinement and Coulomb blockade effects, also leading to poor retention. The C-V and T-E results suggest that, generally, a larger C-V loop of the sample corresponds to a larger tunneling probability but maybe a poorer retention of the memory effect.

This work was supported by the Hong Kong Research Grant Council (No. PolyU 5006/04P) and PolyU internal grant (No. G-YE74). Lee is grateful to the financial support of PolyU postdoctoral fellow grant (No. G-YX83).

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