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Pseudo-diode based on protonic/electronic hybrid oxide transistor

Yang Ming Fu,^{1,2} Yang Hui Liu,³ Li Qiang Zhu,^{1,2,a)} Hui Xiao,^{1,2} and An Ran Song^{1,2}

¹Key Laboratory of Graphene Technologies and Applications of Zhejiang Province, Ningbo Institute of Materials Technology and Engineering, Chinese Academy of Sciences, Ningbo 315201, Zhejiang, People's Republic of China

²University of Chinese Academy of Sciences, Beijing 100049, People's Republic of China

³Department of Applied Physics, The Hong Kong Polytechnic University, Hung Hom, Kowloon, Hong Kong

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Current rectification behavior has been proved to be essential in modern electronics. Here, a pseudo-diode is proposed based on protonic/electronic hybrid indium-gallium-zinc oxide electric-double-layer (EDL) transistor. The oxide EDL transistors are fabricated by using phosphorous silicate glass (PSG) based proton conducting electrolyte as gate dielectric. A diode operation mode is established on the transistor, originating from field configurable proton fluxes within the PSG electrolyte. Current rectification ratios have been modulated to values ranged between ~ 4 and $\sim 50\,000$ with gate electrode biased at voltages ranged between -0.7 V and 0.1 V. Interestingly, the proposed pseudo-diode also exhibits field reconfigurable threshold voltages. When the gate is biased at -0.5 V and 0.3 V, threshold voltages are set to ~ -1.3 V and -0.55 V, respectively. The proposed pseudo-diode may find potential applications in brain-inspired platforms and low-power portable systems. Published by AIP Publishing. <https://doi.org/10.1063/1.5012966>

I. INTRODUCTION

In recent advancements of condensed matters, ionic/electronic hybrid brings promising strategies to enrich physics and device functions.^{1–4} In ionic-liquid or ionic-gel electrolyte gated transistors (EGTs), mobile ions within the electrolytes are coupled with carriers within solid-state semiconductor channels. Because of the strong ionic/electronic coupling effect, such EGTs can operate at low voltages (typically < 2 V).^{5,6} Due to the inherent priorities for ion gating behaviors, EGTs has been proposed for chemical biosensing⁷ and neuromorphic device applications.^{8,9} On the other hand, unidirectional electric current flow has been proved to be essential in modern electronics.^{10,11} Conventionally, such asymmetric current occurs at asymmetric interfaces, such as p-n junctions and metal/semiconductor interfaces, exhibiting rectification behaviors. Meanwhile, current-rectification behavior can also be realized on a metal-oxide-semiconductor field-effect-transistor (MOSFET) by connecting gate and drain electrode.¹² However, the rectification characteristics for these techniques cannot be altered once the devices have been made. Recently, with the developments of nanofabrication techniques, synthetic nanopores with various shapes have been prepared.¹³ Ionic current rectification behaviors have been observed. Moreover, field-effect reconfigurable nanofluidic ionic diodes have been proposed.¹⁴ It should be noted here that solid-state devices with reconfigurable current rectification behaviors are meaningful for solid-state electronic systems. In our previous work, solid-state electrolyte gated oxide electric-double-layer (EDL) transistors have been fabricated, demonstrating good transistor performances.^{15,16} Moreover, the solid-state oxide EDL transistors have been proposed for artificial synapse applications, demonstrating brain-inspired synaptic responses.^{17,18}

In the present work, a pseudo-diode operation mode was reported on a protonic/electronic hybrid oxide EDL transistor. Due to a strong EDL effect, field reconfigurable rectification behaviors have been observed. Interestingly, the proposed pseudo-diode also exhibits field reconfigurable threshold voltages. The pseudo-diode may find potential applications in brain-inspired platforms and low-power portable systems.

II. EXPERIMENTAL DETAILS

Indium gallium zinc oxide (IGZO)-based EDL transistors were fabricated at room temperature. First, nanogranular phosphorous silicate glass (PSG) films were deposited on ITO glass substrates by plasma enhanced chemical vapor deposition (PECVD) using SiH_4/PH_3 mixture and O_2 as reactive gases. The thickness of the PSG film was estimated to be $2.8\text{ }\mu\text{m}$. Then, $\sim 35\text{ nm}$ thick patterned IGZO films acting as channels were sputtered on the PSG electrolyte by using IGZO ceramic target (mole ratio, $\text{In}_2\text{O}_3:\text{Ga}_2\text{O}_3:\text{ZnO} = 1:1:1$) in Ar ambient with a metal shadow mask. Next, patterned ITO source/drain electrodes were sputtered on the IGZO patterns using ITO ceramic target with another metal shadow mask. The size of the ITO pattern is $150\text{ }\mu\text{m} \times 1500\text{ }\mu\text{m}$. The deposition conditions for both IGZO patterns and ITO patterns are as follows: a RF power of 100 W , a pressure of 0.5 Pa , and an Ar gas flow rate of 14.0 sccm . Figure 1(a) illustrates the schematic diagram of the IGZO transistor. Inset shows the optical image of the device. Channel width (W) and length (L) are 1.5 mm and 0.1 mm , respectively. Frequency dependent specific capacitance and proton conductivity of the nanogranular phosphorous silicate glass (PSG) film were characterized by a Solartron 1260A impedance analyzer using a sandwiched ITO/PSG/ITO testing structure. Electrical performances of the PSG gated IGZO EDL transistors were characterized by using a semiconductor parameter analyzer (Keithley 4200 SCS). All the measurements were carried out in a shielded probe station

^{a)}E-mail address: lqzhu@nimte.ac.cn

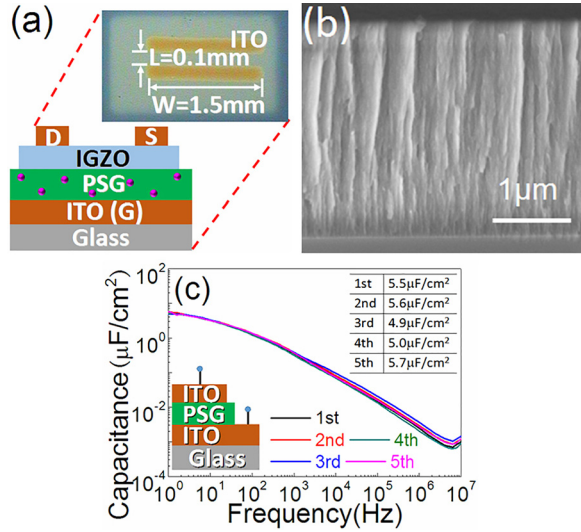


FIG. 1. (a) Schematic diagram of IGZO transistor. Inset is the optical image of the device. (b) Cross-sectional SEM image of the PSG electrolyte films. (c) Five frequency-dependent capacitance curves of the PSG electrolyte. Lower-left inset: A sandwiched ITO/PSG/ITO testing structure. Top-right inset: Obtained EDL capacitances from five curves.

in air ambient with air relative humidity at $\sim 60\%$ at room temperature.

III. RESULTS AND DISCUSSION

Figure 1(b) illustrates the cross-sectional scanning electron microscopy (SEM) image of the PSG film on a Si (100) substrate. It is observed that the PSG film is quite porous. Figure 1(c) shows five frequency-dependent capacitance curves of the PSG electrolyte. The five curves approach each other very well, indicating good stabilities. It is observed that the specific capacitance increases with decreased frequency. Maximum capacitances are observed at 1 Hz due to the formation of EDL at the PSG/ITO interface. Top-right inset lists the extracted EDL capacitances from the five curves. The average EDL capacitance is $\sim 5.3 \mu\text{F}/\text{cm}^2$. As comparison, conventional thermally grown SiO_2 film is quite dense. The capacitance of the thermally grown SiO_2 with the same thickness is calculated to be only $\sim 1.2 \text{ nF}/\text{cm}^2$. Due to the existences of nanochannels, H_2O molecule will be absorbed within the nanogranular PSG electrolyte film. Thus, a big amount of Si-OH bonds and P-OH bonds exist within the PSG film. Under external electric field, mobile protons will be produced within the PSG electrolyte. These protons will migrate through a sequence of hopping between hydroxyl groups. They will accumulate at the PSG/ITO interface, forming an EDL layer. The huge EDL capacitance for the PSG film indicates its strong electrostatic modulation behaviors.

Figure 2(a) illustrates transfer curves (I_{ds} vs V_{gs}) of the IGZO EDL transistor measured for 10 times. V_{ds} is fixed at 1.5 V. V_{gs} is swept from -1.0 V to $+1.5 \text{ V}$ and then back. The voltage sweep rate is set to 50 mV/s . The measured transfer curves approach each other well, indicating stable device performances. A clear anticlockwise hysteresis of $\sim 0.2 \text{ V}$ is observed between forward and backward sweeps.

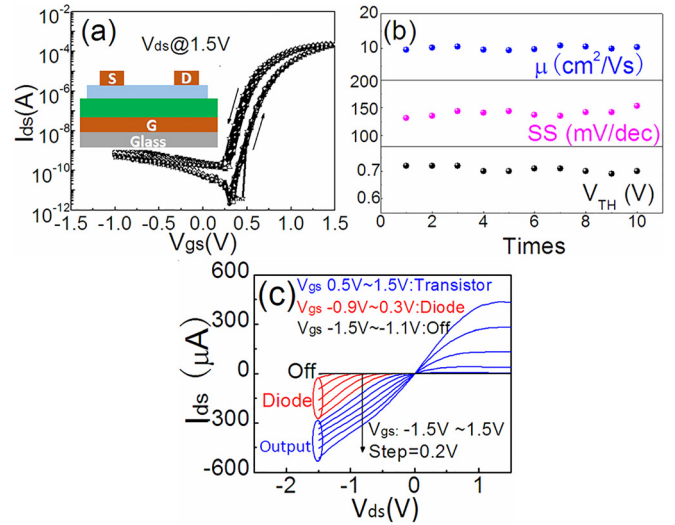


FIG. 2. Electrical performances of IGZO EDL transistor. (a) Transfer characteristics measured for 10 times. (b) Electrical parameters obtained from (a). (c) Output characteristics.

Such hysteresis is ascribed to mobile protons within the PSG electrolyte film. Figure 2(b) illustrates the calculated electrical parameters, including threshold voltage (V_{TH}), subthreshold swing (SS), and field-effect mobility (μ). These parameters are quite stable. The average values for V_{TH} , SS, and μ are estimated to be $\sim 0.71 \text{ V}$, 140 mV , and $10.1 \text{ cm}^2/\text{Vs}$, respectively. Figure 2(c) illustrates output curves (I_{ds} vs V_{ds}) of the IGZO transistor. Conventionally, V_{ds} is swept at positive voltages for n-type oxide transistors. In our case, V_{ds} is swept from -1.5 V to $+1.5 \text{ V}$. V_{gs} is biased at voltages ranged between -1.5 V and 1.5 V with a step of 0.2 V . When V_{ds} is swept from 0 V to 1.5 V , typical n-channel field effect characteristics with good pinch-off and saturation behaviors are exhibited. While when V_{ds} is swept from -1.5 V to 0 V , no saturation behaviors are observed. When V_{ds} is scanned at negative direction, protons tend to accumulate at the PSG/IGZO interface, depending on V_{gs} value. For V_{gs} below -1.1 V , the absolute V_{ds} value is not high enough to induce the accumulation of protons at the PSG/IGZO interface. Thus, the channel current is very low. While for V_{gs} ranged between -0.9 V and 1.5 V , channel current will increase more and more with the increased absolute V_{ds} value due to the accumulation of protons at the PSG/IGZO interface. Interestingly, when V_{gs} ranges between -0.9 V and 0.3 V , the transistor exhibits typical diode-like behaviors with current-rectification characteristics.

Here, a pseudo-diode is proposed. The drain and source electrodes are deemed as two electrodes of the pseudo-diode. The bottom gate is deemed as a modulatory terminal. Figure 3(a) shows I-V curves of the pseudo-diode with the modulatory terminal biased at different voltages ranged between -0.7 V and 0.3 V with steps of 0.2 V . Currents are estimated to be below 5 nA for drain bias (V) at 1.5 V , while it increases significantly at negative drain biases, indicating the current rectification behaviors. The results mean that the diode forward direction is from source to drain. For a modulatory terminal biased at 0.1 V ($V_{\text{m}} = 0.1 \text{ V}$), the rectification ratio ($R = |I_{-\text{V}}/I_{+\text{V}}|$, where $V = 1 \text{ V}$) is estimated to be ~ 50000 .

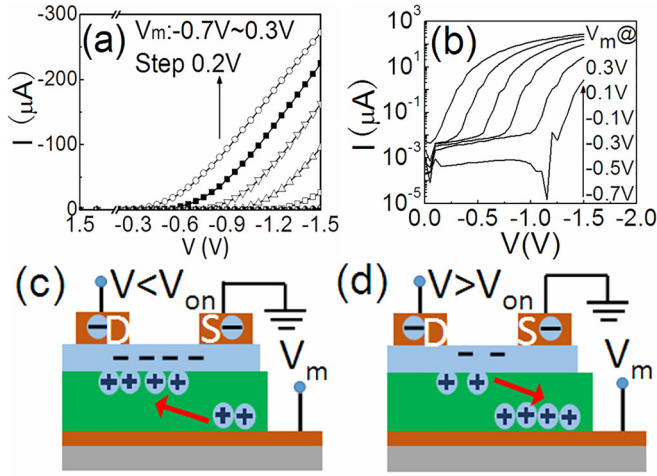


FIG. 3. (a) I-V curves of the pseudo-diode with the modulatory terminal biased at different voltages. (b) Log scale I-V curves of the pseudo-diode. Working mechanism of the pseudo-diode when drain bias is (c) below and (d) above V_{on} .

While for $V_m = -0.7$ V, the rectification ratio is estimated to be only ~ 4 . Conventionally, the rectification ratio will not change for typical p-n junction diode. In our case, current rectification is related to field-configurable proton fluxes within the PSG electrolyte. Such field-configurable rectification ratio is meaningful for portable applications. Furthermore, turn-on voltage (V_{on}) is estimated by extrapolating the linear portion of the I-V curves to $I = 0$. For conventional Si-based p-n junction diode, the turn-on voltage (V_{on}) is as high as ~ 0.7 V. In our case, V_{on} value can be modulated by biasing the modulatory terminal. For $V_m = -0.5$ V, V_{on} is estimated to be ~ -1.3 V, while for $V_m = 0.3$ V, V_{on} decreases to only ~ -0.55 V. The decreased V_{on} value is interesting for portable applications. Figure 3(b) shows log scale I-V curves of the pseudo-diode at negative drain biases. For p-n junction based diode, there is a relation below

$$I = A \exp\left(-\frac{qV}{\eta kT}\right),$$

where A is a constant, and η is an ideal factor ranged between 1 and 2. For the proposed pseudo-diode, η is estimated to be ~ 1.6 .

The working mechanism of the pseudo-diode is discussed as follows. When the modulatory terminal is biased at voltages below 0.3 V ($V_m < 0.3$ V), the IGZO transistor operates at the depletion region [as shown in Fig. 2(a)]. Therefore, the channel current is quite small at positive drain bias (V). Interestingly, protons will tend to accumulate at the PSG/IGZO interface at negative drain bias (V) depending on V_m value. If the absolute V_m is too big, i.e., $V_m < -1.1$ V, the absolute V value is not high enough to overcome V_m and induce the accumulation of protons at the PSG/IGZO interface. Thus, the channel current is very small. When V_m shifts to positive direction, some protons will get accumulated at the PSG/IGZO interface with drain bias below a certain negative value (i.e., $V < V_{on} < 0$) [as shown in Fig. 3(c)]. Thus, carrier density in the IGZO channel will increase due to the EDL effects, which results in the increased channel current.

When V_m shifts to positive direction further, protons will get easier to accumulate at the PSG/IGZO interface for negative V values. In other words, the absolute V_{on} value decreases ($V_{on} < 0$). When the drain bias is above V_{on} ($V > V_{on}$), protons within PSG electrolyte will accumulate at the PSG/gate interface [as shown in Fig. 3(d)]. Therefore, the IGZO channel is depleted and the channel current is quite small.

Dynamic current rectification behavior of the pseudo-diode is further demonstrated by applying pulsed square-shaped bias with a pulsed amplitude of $V_+ = 1$ V and $V_- = -1$ V. Figure 4(a) shows a transient response of the pseudo-diode on a sequence of square-shaped drain biases with the modulatory terminal biased at 0.1 V. It is observed that the current is ~ 20 μA when the drain bias is -1 V, while it decreases to ~ 0.4 nA when the drain bias is 1 V. Thus, the rectification ratio is estimated to be $\sim 5 \times 10^4$. Figure 4(b) illustrates the dynamic rectification ratio as a function of pulse-cycles at different V_m values. It is observed that the rectification ratio decreases from $\sim 5 \times 10^4$ to ~ 1.7 when the V_m value shifts from 0.1 V to -0.9 V. There are almost no changes in the rectification ratio with the increased cycles, indicating the good stabilities of the pseudo-diode.

Due to the inherent properties for proton gating, the device cannot work when the frequency is very high. In our previous work, the characteristic time of proton gating of PSG electrolyte is estimated to be tens ms.¹⁷ Therefore, a delay time will be observed on the dynamic current rectification behavior. Because of the field-configurable proton fluxes and EDL coupling effect within PSG film, it can be concluded that the proposed pseudo-diode can operate only at a low-frequency (up to tens Hz) when the size of the device is optimized. It is interesting to note here that such frequency is high enough for brain-inspired platform applications. In biological nervous systems, the frequency ranges from several Hz to several tens Hz for synaptic responses. Thus, the proposed pseudo-diode may also find potential applications in brain-inspired platforms. Furthermore, though the current rectification behavior was established on the proposed pseudo-diode, it cannot be used in light-emitting diodes and solar cells because of the inexistence of p-n junctions. For conventional

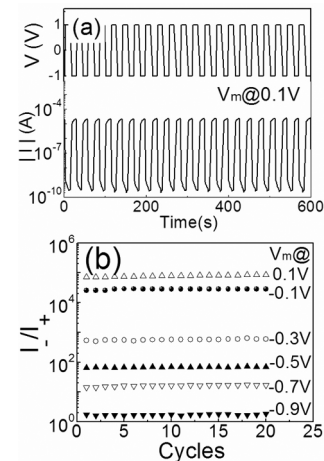


FIG. 4. (a) Transient response of the pseudo-diode on a square-shaped drain bias (V) with the modulatory terminal biased at 0.1 V. (b) Dynamic rectification ratio as a function of pulse-cycles at different V_m values.

p-n junction based diodes, the turn-on voltage (V_{on}) will not change. While for the present pseudo-diode, V_{on} can be regulated to different values by biasing the modulatory terminal, which is helpful for extending the device function. For example, V_{on} is modulated to only ~ -0.55 V with the modulatory terminal biased at 0.3 V. Thus, a small energy collector may be obtained for portable applications when the proposed pseudo-diode is connected to a piezoelectric device. Thus, the proposed pseudo-diode may also find potential applications in portable sensors, small energy generator, etc.

IV. CONCLUSIONS

In summary, a protonic/electronic hybrid pseudo-diode was proposed based on a PSG electrolyte gated IGZO transistor. The rectification ratios can be modulated between $\sim 50\,000$ and ~ 4 with the modulatory terminal biased at voltages between 0.1 V and -0.7 V. The current rectification behaviors are related to field configurable proton fluxes within the PSG electrolyte film. Moreover, field reconfigurable threshold voltages were also observed on the proposed pseudo-diode. Since there is no p-n junction within the pseudo-diode, it cannot be used in optoelectronic devices. However, with a high rectify ratio, the pseudo-diode may have potential applications in low-power portable systems.

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- ¹K. Ueno, S. Nakamura, H. Shimotani, A. Ohtomo, N. Kimura, T. Nojima, H. Aoki, Y. Iwasa, and M. Kawasaki, *Nat. Mater.* **7**, 855 (2008).
- ²L. J. Li, E. C. T. O'Farrell, K. P. Loh, G. Eda, B. Ozyilmaz, and A. H. C. Neto, *Nature* **529**, 185 (2016).
- ³J. Pu, K. Funahashi, C.-H. Chen, M.-Y. Li, L.-J. Li, and T. Takenobu, *Adv. Mater.* **28**, 4111 (2016).
- ⁴N. Lu, P. Zhang, Q. Zhang, R. Qiao, Q. He, H. B. Li, Y. Wang, J. Guo, D. Zhang, Z. Duan, Z. Li, M. Wang, S. Yang, M. Yan, E. Arenholz, S. Zhou, W. Yang, L. Gu, C. W. Nan, J. Wu, Y. Tokura, and P. Yu, *Nature* **546**, 124 (2017).
- ⁵S. H. Kim, K. Hong, W. Xie, K. H. Lee, S. P. Zhang, T. P. Lodge, and C. D. Frisbie, *Adv. Mater.* **25**, 1822 (2013).
- ⁶H. T. Yuan, H. Shimotani, J. T. Ye, S. Yoon, H. Aliah, A. Tsukazaki, M. Kawasaki, and Y. Iwasa, *J. Am. Chem. Soc.* **132**, 18402 (2010).
- ⁷N. Liu, Y. H. Liu, P. Feng, L. Q. Zhu, Y. Shi, and Q. Wan, *Appl. Phys. Lett.* **106**, 073507 (2015).
- ⁸P. Gkoupidenis, N. Schaefer, B. Garlan, and G. G. Malliaras, *Adv. Mater.* **27**, 7176 (2015).
- ⁹W. T. Xu, S.-Y. Min, H. Hwang, and T.-W. Lee, *Sci. Adv.* **2**, e1501326 (2016).
- ¹⁰T. Choi, S. Lee, Y. J. Choi, V. Kiryukhin, and S. W. Cheong, *Science* **324**, 63 (2009).
- ¹¹S. Ho, H. Yu, and F. So, *Appl. Phys. Lett.* **111**, 212103 (2017).
- ¹²K. Souri, Y. Chae, F. Thus, and K. Makinwa, *IEEE Int. Solid-State Circuits Conf.* **12**, 222 (2014).
- ¹³I. Vlasiouk and Z. S. Siwy, *Nano Lett.* **7**, 552 (2007).
- ¹⁴W. Guan, R. Fan, and M. A. Reed, *Nat. Commun.* **2**, 506 (2011).
- ¹⁵W. Dou, L. Q. Zhu, J. Jiang, and Q. Wan, *Appl. Phys. Lett.* **102**, 093509 (2013).
- ¹⁶L. Q. Zhu, J. Y. Chao, and H. Xiao, *Appl. Phys. Lett.* **105**, 243508 (2014).
- ¹⁷N. Liu, L. Q. Zhu, H. Xiao, C. J. Wan, Y. H. Liu, and J. Y. Chao, *ACS Appl. Mater. Interfaces* **7**, 6205 (2015).
- ¹⁸J. Wen, L. Q. Zhu, Y. M. Fu, H. Xiao, L. Q. Guo, and Q. Wan, *ACS Appl. Mater. Interfaces* **9**, 37064 (2017).