RESEARCH ARTICLE | MARCH 26 2024

Improved breakdown performance in recessed-gate normally off GaN MIS-HEMTs by regrown fishbone trench

JiaQi He ; PeiRan Wang ; FangZhou Du ; KangYao Wen ; Yang Jiang ; ChuYing Tang ; ChenKai Deng ; MuJun Li ; QiaoYu Hu ; Nick Tao; Peng Xiang; Kai Cheng ; Qing Wang ; Gang Li ; HongYu Yu

Appl. Phys. Lett. 124, 132104 (2024)
https://doi.org/10.1063/5.0193734

Applied Physics Letters ARTICLE pubs.aip.org/aip/apl

Improved breakdown performance in recessed-gate normally off GaN MIS-HEMTs by regrown fishbone trench

Cite as: Appl. Phys. Lett. **124**, 132104 (2024); doi: 10.1063/5.0193734
Submitted: 23 December 2023 · Accepted: 5 March 2024 ·
Published Online: 26 March 2024

JiaQi He,[1,2] PeiRan Wang,[1] FangZhou Du,[1] KangYao Wen,[1] Yang Jiang,[1] ChuYing Tang,[1] ChenKai Deng,[1] MuJun Li,[1] QiaoYu Hu,[1] Nick Tao,[3] Peng Xiang,[4] Kai Cheng,[4] Qing Wang,[1,5,a)] Gang Li,[2,a)] and HongYu Yu[1,5,a)]

AFFILIATIONS

[1]School of Microelectronics, Southern University of Science and Technology, Shenzhen 518055, China
[2]Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong
[3]Maxscend Microelectronics Company Limited, Wuxi 214072, China
[4]Enkris Semiconductor Inc., Suzhou 215123, China
[5]Engineering Research Center of Integrated Circuits for Next-Generation Communications, Ministry of Education, Southern University of Science and Technology, Shenzhen 518055, China

[a)]**Authors to whom correspondence should be addressed:** wangq7@sustech.edu.cn; gang.w.li@polyu.edu.hk; and yuhy@sustech.edu.cn

ABSTRACT

This work develops a regrown fishbone trench (*RFT*) structure in selective area growth (SAG) technique to fabricate recessed-gate normally off GaN metal–insulator–semiconductor high electron mobility transistors (MIS-HEMTs). The *RFT* structure effectively modulates the electric field at high drain and gate biases, thus allowing the device to feature improved off-state and gate breakdown performance with a high positive V_{th} of 2 V. The simulated carrier concentration and electric field distributions reveal the mechanism of electric field weakening by *RFT* architecture. Meanwhile, the current collapse phenomenon is significantly suppressed, and the gate voltage swing is also enlarged. The maximum gate drive voltage of 9.2 V for 10-year reliability of *RFT* GaN MIS-HEMT, together with the improved linearity and block voltage, broadens the applications of SAG devices. Furthermore, the *RFT* structure also provides an etching-free method for fabricating normally off GaN MIS-HEMTs with multi-dimensional gates.

GaN high electron mobility transistors (HEMTs) with normally-off properties are potential candidates for commercial product applications for fail-safe consideration and cost saving on circuit design.[1,2] Compared with the p-GaN gate device, the recessed-gate normally off metal–insulator–semiconductor HEMT (MIS-HEMT) features a larger threshold voltage (V_{th}) and gate breakdown voltage (BV).[3–5] Generally, the AlGaN barrier on the gate region is etched to deplete (fully recessed) or reduce (partially recessed) the two-dimensional electron gas (2DEG) for the positive V_{th}, while the induced etching damage could limit the interface and on-state properties. To mitigate this issue, an etching-free recessed-gate AlGaN/GaN regrown process by metal-organic chemical vapor deposition (MOCVD), called selective area growth (SAG), has been applied to improve the device performance.[6,7]

The SAG partially recessed GaN MIS-HEMTs are usually fabricated on the initial wafer with an ultrathin-barrier AlGaN/GaN heterojunction, showing superior channel mobility and on-state resistance (R_{on}) than the fully recessed devices.[8,9] Generally, the gate dielectric of SAG GaN MIS-HEMT is deposited by atomic layer deposition (ALD), such as Al_2O_3 and ZrO_2, where the low interface states and current leakage enhance the operational reliability.[10,11] However, the regrown sidewalls of recessed-gate are usually under a high electric field intensity due to the recess-first procedure, and the lack of modulation terminals leads to the degenerated breakdown and dynamic performance of SAG GaN MIS-HEMT. Therefore, most of the state-of-the-art SAG recessed-gate devices feature off-state $BV < 250$ V, which could be only applied to low-power electronics.[12–14]

It has been reported that the particular trench shape could reduce the electric field crowding at the gate region, such as the GaN tri-gate HEMTs or Fin-FETs, thus increasing the device BV.[15–17] The fishbone or tree-like channel FETs were also used to supply process advantages.[18,19]

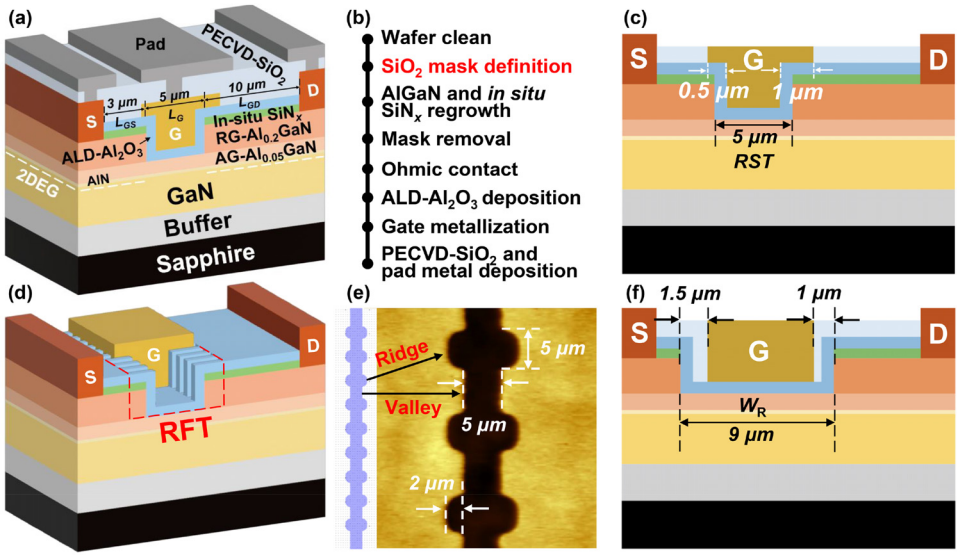

FIG. 1. (a) Schematics and (b) device fabrication process of SAG recessed-gate GaN MIS-HEMT; (c) cross section view of *RST* device with gate metal covering the two sidewalls of the trench; (d) schematics of *RFT* recessed-gate GaN MIS-HEMT; (e) regrowth mask shape and AFM image of *RFT*; and (f) cross section view of *RFT* device in ridge region with the spaces between gate metal and sidewalls.

In order to broaden the application fields of SAG devices, an improved regrown fishbone trench (*RFT*) for partially recessed GaN MIS-HEMT was developed in this study. The *RFT* and regrown straight trench (*RST*) structures were shaped by SiO_2 mask by plasma-enhanced chemical vapor deposition (PECVD), and the fabricated recessed-gate GaN MIS-HEMTs with the gate dielectric of ALD-Al_2O_3 showed excellent normally off and breakdown performance. The modulated electric field by *RFT* structure helped to suppress the current collapse, and the gate voltage swing was also increased compared to that of the *RST* device. The flat transconductance (G_m) profile showed the great linearity. In addition, the improved time-dependent dielectric breakdown (TDDB) performance reveals the gate driver design flexibility and robust gate reliability of *RFT* GaN MIS-HEMTs.

The SAG MIS-HEMTs were fabricated on an initial 4-in. 5-nm-$Al_{0.05}GaN$/AlN/GaN/buffer/sapphire wafer. The *RST* and *RFT* structures were defined by various shapes of PECVD-SiO_2 regrowth masks. The 20-nm-regrown (*RG*)-$Al_{0.2}GaN$ and 10 nm *in situ* SiN_x were deposited on the patterned wafer surface by MOCVD. After the SiO_2 mask removal by buffered oxide etch (BOE), the Ohmic contact was formed by Ti/Al/Ti/Au metal stack annealing at 830 °C for 45 s in an N_2 ambient. Next, a 20-nm-Al_2O_3 insulating layer was deposited with the sources of ozone and TMAl at 300 °C by ALD, and a Ni/Au gate metal was evaporated by E-beam to form the gate stacks. Finally, a 200-nm PECVD-SiO_2 layer was applied to protect the device surface. As shown in Figs. 1(a)–1(c), the *RST* device featured the gate width (W_G), gate length (L_G), distance of gate-to-source (L_{GS}), and distance of gate-to-drain of 100/3/5/10 μm, with an extension distance of 0.5 and 1 μm toward the source and drain side, respectively. Figure 1(d) demonstrates the schematic of the *RFT* device, where the shape of the regrowth mask and the atomic force microscopy (AFM) image of $Al_{0.2}GaN/Al_{0.05}GaN$ *RFT* structure are shown in Fig. 1(e). The length of both valley and ridge is 5 μm, and the width of the ridge (W_R) was 9 μm (2 μm extension for both sides), with the filleted corners at the junction of the ridge and valley regions. Figure 1(f) depicts that the gate metal did not cover the ridge sidewalls. The spaces among the source-to-gate sidewall, gate metal, and gate-to-drain sidewall were 1.5 and 1 μm, respectively, filled by the PECVD-SiO_2. The valley in *RFT* was the same as *RST* structures.

The transfer characteristics of the GaN recessed-gate MIS-HEMTs with various regrown trenches are plotted in Fig. 2(a) at V_{DS} of 5 V. Both the devices with *RST* and *RFT* structures showed a similar V_{th} of 2 V using a drain current criterion of 1 μA/mm, high on/off current ratio of 10^9, and high G_m of more than 100 mS/mm. However, G_m of the *RST* device rapidly decreased with V_G increasing, while the counterpart of *RFT* device featured broad plateaus of gate voltage swing, showing outstanding device linearity.[20] The interface state densities of O_3-Al_2O_3/AlGaN were expected to be lower than 10^{12} cm^{-2} eV^{-1}, resulting in the low V_{th} hysteresis for both devices.[21]

As plotted in Figs. 2(b) and 2(c), R_{on} of *RST* and *RFT* devices was 7.7 and 9.4 Ω·mm, respectively, and R_{on} of recessed-gate GaN MIS-HEMT can be expressed by the following equation:[10]

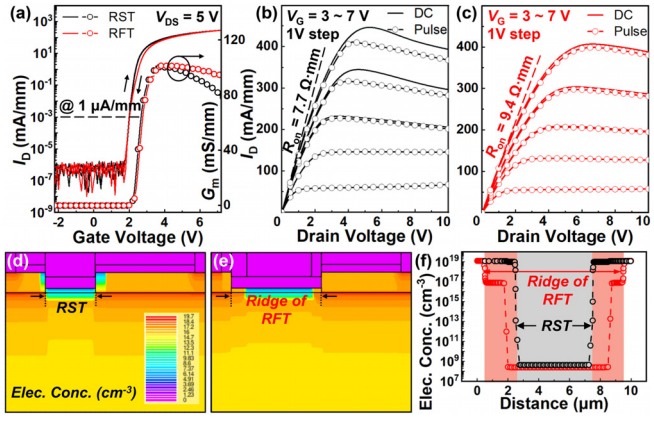

FIG. 2. (a) Double-sweep transfer and transconductance curves; *DC* (solid line) and pulsed (dot line) output characteristics for (b) *RST* and (c) *RFT*; simulated distribution of electron concentration for (d) *RST* and (e) ridge of *RFT*; and (f) extracted curves across the AlGaN/GaN interfaces.

$$R_{on} = 2R_c + R_{sh} \times (L_{GD} + L_{GS}) + R_{ch} \times L_G. \quad (1)$$

R_c and R_{sh} are the contact and sheet resistance (0.3 Ω·mm and 350 Ω/sq in this work), respectively. Thus, the channel resistance (R_{ch}) of the *RST* device is calculated to 510 Ω/sq. However, the resistance of the space (R_s) between the gate metal and sidewall of the *RFT* structure is larger than R_{ch}. R_{on} of the *RFT* device should be modified as follows:

$$R_{on} = \left[R_{sh} \times (L_{SD} - W_R) + R_{ch} \times L_{GR} + R_s \times (W_R - L_{GR})\right] \times R\% + \left[R_{sh} \times (L_{GD} + L_{GS}) + R_{ch} \times L_{GV}\right] \times V\% + 2R_c, \quad (2)$$

where L_{GR} and L_{GV} are the gate length on the ridge and valley regions of the *RFT* device, and *R*% and *V*% are the length ratio of ridge and valley to W_G, respectively. R_s is calculated to 1770 Ω/sq, leading to a higher R_{on} of the *RFT* device.

Figures 2(d) and 2(e) show the cross section view of electron concentration distribution of both the off-state devices, and the comparison of two gate trench structures is plotted in Fig. 2(f). The *RFT* device featured a weak control of 2DEG at the spaces between the gate metal and sidewalls, which confirmed the calculated result of R_s. This phenomenon implied that the rising rate of I_D could be smooth in high V_G driving situations, explaining the effective inhibition of G_m roll-off at high drain current.[22] In addition, the output characteristics were conducted under the pulsed gate voltage with a pulse width/period of 1/20 ms and the quiescent gate bias of (0 V, 20 V). The current collapse was observed in the *RST* device, while the *RFT* device only featured minimal dispersion between the *DC* and gate-pulsed output current.[11] It was speculated that the ridges of *RFT* along the gate-to-drain side significantly prevented the peak electric field on regrown sidewalls, which could suppress the tunneling electrons to the bulk and interface traps.

The I_D and I_G–V_D curves at $V_G = 0$ V in Fig. 3(a) illustrate that the off-state *BV* of the *RFT* device increased from 461 to 557 V, and the gate leakage was lower by more than one order of magnitude of the *RST* device. To explore the mechanism of these improved performance, the electric field distributions of off-state *RST* and *RFT* devices were simulated by TCAD. The SAG was a trench-first process, where the thick passivation layers were usually deposited after the gate metallization. Therefore, the gate metal wings of the *RST* device were close to the regrown barrier, and most of the peak electric field was located on the gate-to-drain side at off-state with V_{DS} higher than 500 V, as shown in Fig. 3(b). The maximum electric field on the *RG*-AlGaN was 1.326×10^7 V/cm, which, beyond the critical field strength (3.3×10^6 V/cm) of GaN, thus burned the device. However, the gate metal at the ridge of the *RFT* device was separated from the *RG*-AlGaN by PECVD-SiO_2, whose critical field strength was much higher than the GaN.[23] Figure 3(c) shows that the peak electric field was located on Al_2O_3 and SiO_2. Thus, the *AG*-AlGaN and *RG*-AlGaN were within the breakdown limitation. As a result, the *RFT* device features a higher off-state BV and lower gate current leakage by weakening the electric field along the gate-to-drain side.

The electric field distribution of SAG recessed-gate GaN MIS-HEMTs at $V_{DS} = 0$ V with a V_G higher than 15 V was also simulated. When a high gate bias was applied on the *RST* device, the peak electric field was located on the interface between Al_2O_3 and *RG*-AlGaN sidewall along the gate-to-source side, as demonstrated in Fig. 4(a). As for the *RFT* device [Fig. 4(b)], the peak electric field was located on the Al_2O_3 bulk, and the peak value was less than half of the counterpart of *RST*. It was also attributed to the buffer effect of PECVD-SiO_2 between the gate metal and regrown sidewall that weakened the electric field and conduction current.[24] Furthermore, the lateral electric field across the metal/Al_2O_3/AlGaN and metal/SiO_2/Al_2O_3/AlGaN structures is extracted and plotted in Fig. 4(c). The electric field at the interface of Al_2O_3/AlGaN sidewall has nearly reached the critical field strength of

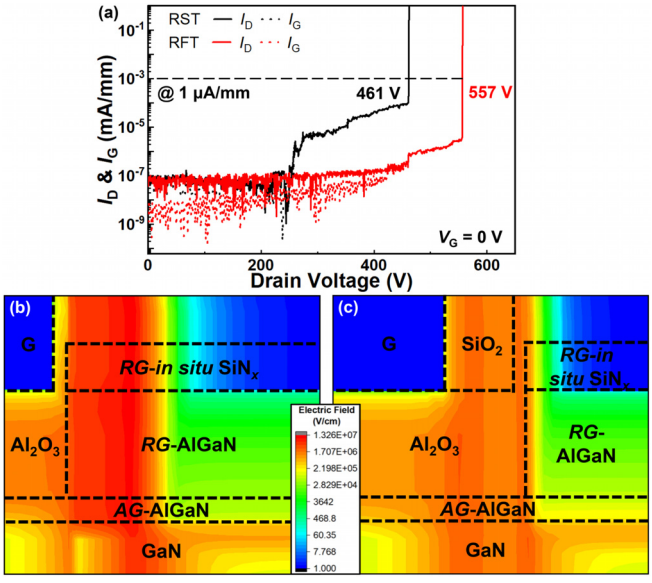

FIG. 3. (a) Off-state ($V_G = 0$ V) BV characteristics of recessed-gate GaN MIS-HEMTs with *RST* and *RFT* structures; simulated electric field distribution map at (b) *RST* and (c) ridge of *RFT* device with $V_G = 0$ V and $V_{DS} > 500$ V. Inset is the gradient color table of electric field (from red to blue indicates the strength from high to low).

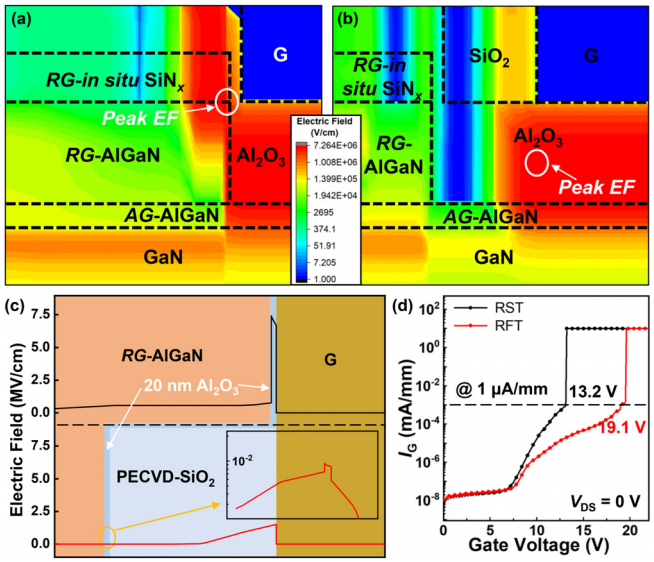

FIG. 4. Simulated electric field distribution map at (a) *RST* and (b) ridge of *RFT* device with $V_{DS} = 0$ V and $V_G > 15$ V; (c) electric field intensity exacted from the simulation mode on the gate-to-source side for *RST* device and ridge of *RFT* device, and inset is the enlarged image of electric field on Al_2O_3 region; and (d) I_G–V_G curves at $V_{DS} = 0$ V.

ALD-Al_2O_3, while introducing the *RFT* structure and PECVD-SiO_2 resulted in the three orders of magnitude lower peak value on Al_2O_3 and four times lower peak value on SiO_2, respectively. Figure 4(d) shows the measured I_G–V_G curves that the maximum V_G of 19.1 V for the *RFT* device was much higher than the 13.2 V for the *RST* device. The breakdown performance of fabricated devices verified the electric field models, indicating that the *RFT* structure could effectively modulate the electric field distribution in SAG recessed-gate GaN MIS-HEMTs.

To verify the device V_{th} reliability, a series of positive bias time instability (PBTI) measurements were conducted with the gate stress time of 0, 3, 10, 30, 100, 300, 1000, and 3000 s, respectively. The source and drain terminals were grounded during the continuous gate stress procedure, while the fast I_D-V_G tested at $V_{DS} = 1$ V. As plotted in Figs. 5(a) and 5(b), V_{th} showed a positive shift from 0 to 3000 s, and the maximum V_{th} shift of 0.35 V for *RFT* was lower than the *RST* device. It was also attributed to the weaken electric field along the gate-to-source side, which could decelerate the electrons drift from the 2DEG channel to aggregate in the gate center. Therefore, the *RFT* device featured better V_{th} stability under long-time stresses.

The TDDB tests were further performed for the two SAG recessed-gate GaN MIS-HEMTs to evaluate the device reliability. The V_G biases of 10, 11, 12 V and 15, 16, 17 V were stressed to the *RST* and *RFT* devices with source and drain grounded, respectively. As plotted in Figs. 6(a) and 6(b), the time-to-breakdown (t_{BD}) at a constant stress voltage showed a tight breakdown distribution with the Weibull slope β of 4.0 for *RST* and 3.5 for *RFT* devices, respectively. By using the linear model to predict the 10-year reliability, as shown in Figs. 6(c) and 6(d), the *RST* device featured a maximum gate drive voltage of 5.2 and 4.6 V at the failure rate of 63% and 1%, respectively, which are relatively low values that limited its application on the high-power switching system. However, thanks to the high maximum V_G and gently increasing gate leakage of the *RFT* device, the maximum gate drive voltage of 9.2 and 8.1 V at the failure rate of 63% and 1% was achieved, offering more gate driver design flexibility and robust gate reliability for the normally-off GaN MIS-HEMTs.[25] It was also verified that the reliability of SAG devices can be overcome by the regrown structure design.

Based on the SAG technique, an *RFT* structure for electric field modulation was adapted to fabricate normally off recessed-gate GaN MIS-HEMTs. A sheer fishbone trench was fabricated, and the calculated model was established by combining the carrier distribution simulation and device measurement. The *RFT* structure remarkably improved the off-state and gate breakdown performance with a high V_{th} of 2 V. The simulated electric field distributions for high gate and

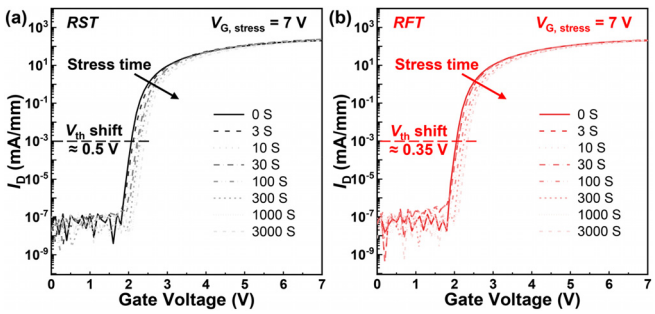

FIG. 5. Gate stress induced time instability on V_{th} for (a) *RST* and (b) *RFT* devices with a positive bias of 7 V from 0 to 3000 s.

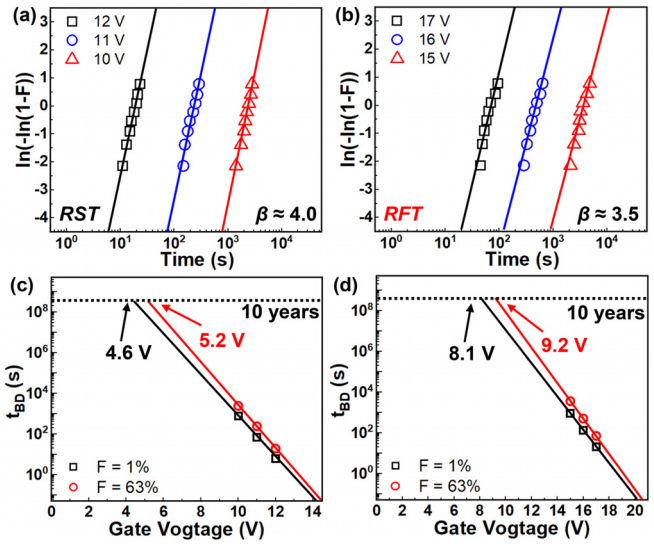

FIG. 6. Weibull distribution of the electric-field-dependent TDDB results for recessed-gate GaN MIS-HEMTs with (a) *RST* and (b) *RFT* structure; and 10-year-reliability prediction with 63% and 1% failure rate for (c) *RST* and (d) *RFT* devices.

drain biases clearly revealed the modulation mechanism of the *RFT* device. Meanwhile, the current collapse phenomenon was significantly suppressed by the electric field modulation, and the gate voltage swing of the *RFT* device could further improved by scaling the linewidth of the regrown mask. The long TDDB lifetime of *RFT* GaN MIS-HEMTs, together with the improved linearity and drive voltage, broadened the applications of SAG devices on radio frequency and medium-voltage electronics. The *RFT* architecture in this work also provided an etching-free method for fabricating normally off GaN MIS-HEMTs with multi-dimensional gates.

The authors acknowledge the assistance of SUSTech Core Research Facilities.

This work was supported by the National Natural Science Foundation of China (Grant No. 62122004), research on mechanism of source/drain Ohmic contact and the related GaN p-FET (Grant No. 2023A1515030034), study on the reliability of GaN power devices (Grant No. JCYJ20220818100605012), research on novelty low-resistance source/drain Ohmic contact for GaN p-FET (Grant No. JCYJ20220530115411025), research on high-reliable GaN power device and the related industrial power system (Grant No. HZQB-KCZYZ-2021052), and the Natural Science Foundation for Young Scientists of Jiangsu Province (Grant No. BK20210116).

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

JiaQi He: Conceptualization (lead); Data curation (lead); Methodology (lead); Software (equal); Writing – original draft (lead). **PeiRan Wang:** Software (equal). **FangZhou Du:** Formal analysis (supporting);

Investigation (supporting). **KangYao Wen:** Formal analysis (supporting); Methodology (supporting). **Yang Jiang:** Data curation (supporting); Resources (supporting). **ChuYing Tang:** Data curation (supporting); Methodology (supporting). **ChenKai Deng:** Methodology (supporting); Resources (supporting). **MuJun Li:** Formal analysis (supporting); Investigation (supporting). **QiaoYu Hu:** Investigation (supporting); Resources (supporting). **Nick Tao:** Project administration (supporting). **Peng Xiang:** Resources (equal). **Kai Cheng:** Project administration (supporting); Resources (supporting). **Qing Wang:** Funding acquisition (supporting); Project administration (supporting); Writing – original draft (supporting). **Gang Li:** Methodology (supporting); Supervision (supporting). **HongYu Yu:** Funding acquisition (lead); Project administration (lead); Supervision (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

REFERENCES

[1]M. Meneghini, C. D. Santi, I. Abid, M. Buffolo, M. Cioni, R. A. Khadar, L. Nela, N. Zagni, A. Chini, F. Medjdoub, G. Meneghesso, G. Verzellesi, E. Zanoni, and E. Matioli, J. Appl. Phys. **130**(18), 181101 (2021).

[2]J. He, W.-C. Cheng, Q. Wang, K. Cheng, H. Yu, and Y. Chai, Adv. Electron. Mater. **7**(4), 2001045 (2021).

[3]K. Deng, S. Huang, X. Wang, Q. Jiang, H. Yin, J. Fan, G. Jing, K. Wei, Y. Zheng, J. Shi, and X. Liu, Appl. Surf. Sci. **638**, 158000 (2023).

[4]M. Li, J. Wang, B. Zhang, Q. Tao, H. Wang, Q. Cao, C. Huang, J. Liu, J. Mo, and W. Wu, Solid-State Electron. **177**, 107927 (2021).

[5]J. He, K. Wen, P. Wang, M. He, F. Du, Y. Jiang, C. Tang, N. Tao, Q. Wang, G. Li, and H. Yu, Appl. Phys. Lett. **123**(10), 103502 (2023).

[6]L. He, L. Li, J. Zhang, Y. Ni, J. Zhang, Z. Liu, Q. Wu, and Y. Liu, paper presented at the 2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Nagoya, Japan, 2021.

[7]J. T. Asubar, S. Kawabata, H. Tokuda, A. Yamamoto, and M. Kuzuhara, IEEE Electron Device Lett. **41**(5), 693 (2020).

[8]L. He, F. Yang, Y. Yao, Y. Zheng, J. Zhang, L. Li, Z. He, Y. Ni, X. Gu, and Y. Liu, Jpn. J. Appl. Phys., Part 1 **59**(SA), SA0806 (2020).

[9]J. He, M. Hua, Z. Zhang, and K. J. Chen, IEEE Trans. Electron Devices **65**(8), 3185 (2018).

[10]J. Zhang, L. He, L. Li, Y. Ni, T. Que, Z. Liu, W. Wang, J. Zheng, Y. Huang, J. Chen, X. Gu, Y. Zhao, L. He, Z. Wu, and Y. Liu, IEEE Electron Device Lett. **39**(11), 1720 (2018).

[11]H. Jiang, C. W. Tang, and K. M. Lau, IEEE Electron Device Lett. **39**(3), 405 (2018).

[12]J. Zhang, L. He, L. Li, Y. Ni, T. Que, Z. Liu, W. Wang, J. Zheng, Y. Huang, J. Chen, X. Gu, Y. Zhao, L. He, Z. Wu, and Y. Liu, paper presented at the 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2018.

[13]L. He, F. Yang, L. Li, Z. Chen, Z. Shen, Y. Zheng, Y. Yao, Y. Ni, D. Zhou, X. Zhang, L. He, Z. Wu, B. Zhang, and Y. Liu, IEEE Trans. Electron Devices **64**(4), 1554 (2017).

[14]H. Jiang, R. Zhu, Q. Lyu, C. W. Tang, and K. M. Lau, Semicond. Sci. Technol. **36**(3), 034001 (2021).

[15]Y. Zhang, F. Udrea, and H. Wang, Nat. Electron. **5**(11), 723 (2022).

[16]L. Nela, J. Ma, C. Erine, P. Xiang, T.-H. Shen, V. Tileli, T. Wang, K. Cheng, and E. Matioli, Nat. Electron. **4**(4), 284 (2021).

[17]Y. Ma, M. Xiao, Z. Du, X. Yan, K. Cheng, M. Clavel, M. K. Hudait, I. Kravchenko, H. Wang, and Y. Zhang, Appl. Phys. Lett. **117**(14), 143506 (2020).

[18]L. Cao, Q. Zhang, Y. Luo, J. Gu, W. Gan, P. Lu, J. Yao, H. Xu, P. Zhao, K. Luo, Y. Wu, W. Bu, Z. Wu, and H. Yin, IEEE Trans. Electron Devices **69**(11), 5971 (2022).

[19]Y. Sun, X. Li, Z. Liu, Y. Liu, X. Li, and Y. Shi, IEEE Trans. Electron Devices **69**(1), 370 (2022).

[20]M. T. Azad, T. Hossain, B. Sikder, Q. Xie, M. Yuan, E. Yagyu, K. H. Teo, T. Palacios, and N. Chowdhury, IEEE Trans. Electron Devices **70**(11), 5570 (2023).

[21]J. He, Q. Wang, G. Zhou, W. Li, Y. Jiang, Z. Qiao, C. Tang, G. Li, and H. Yu, IEEE Electron Device Lett. **43**(4), 529 (2022).

[22]P.-F. Wang, M.-H. Mi, X. Du, Y.-W. Zhou, J.-L. Liu, Z.-H. Chen, S.-R. An, Y.-L. Chen, J.-J. Zhu, and X.-F. Zheng, Appl. Phys. Lett. **121**(7), 072110 (2022).

[23]P. Laukkanen, M. P. J. Punkkinen, M. Kuzmin, K. Kokko, J. Lång, and R. M. Wallace, Appl. Phys. Rev. **8**(1), 011309 (2021).

[24]B. K. Jebalin, A. S. Rekh, P. Prajoon, N. M. Kumar, and D. Nirmal, Microelectron. J. **46**(12), 1387 (2015).

[25]N. Sun, H. Huang, Z. Sun, R. Wang, S. Li, P. Tao, Y. Ren, S. Song, H. Wang, S. Li, W. Cheng, and H. Liang, IEEE Trans. Electron Devices **69**(1), 82 (2022).