Discover Applied Sciences

Research

Influence of N_2 plasma treatment on properties of black phosphorus devices in space electronic systems

Shenli Wang[1,2] · Zhigao Wang[1,2] · Xuan Wang[1,2] · Huan Xia[1,2] · Qian Wang[1,2] · Peng Duan[1,2] · Feiyu Leng[1,2] · Jing Tian[1,2] · Hao Huang[3] · Wai-Hung Ip[4] · Kai-Leung Yung[4]

Received: 26 November 2023 / Accepted: 22 May 2024
Published online: 30 May 2024

Abstract
In order to improve the country's comprehensive national strength and seize space resources, the implementation of new space systems requires the use of advanced technology in key applications of microelectronics. To further improve device performance, black phosphorus (BP) is used to overcome feature size limitations for its atomic thickness. BP has excellent physical properties such as in-plane anisotropy, thickness-dependent direct band gap and high carrier mobility. However, the performance control of phosphene is a major challenge in practical applications. In order to tune the BP performance, various theoretical and experimental studies on the doping mechanism and strategies of BP have been proposed and reported. In this work, the performance of BP can be effectively tuned by N_2 plasma treatment. By changing the power and processing time, the on-state current and mobility of the device can be effectively improved. This simple and efficient doping technique provides a valuable way to realize high performance BP thin film transistors.

Article Highlights

1. To seize space resources, the implementation of new space systems requires the use of advanced technologies in critical applications of microelectronics. Black phosphorus transistor is used to overcome feature size limitations for its atomic thickness with excellent physical properties.
2. For practical application, the performance of the black phosphorus transistor is effectively tuned by N_2 plasma treatment through changing the power and processing time. The results show that the on-state current and mobility of the device can be effectively improved
3. The N_2 plasma treatment is a simple, efficient and large-scale doping technique to control the properties of the transistor.

Keywords Black phosphorus · Transistor · N_2 plasma · Mobility · The on/off ratio

✉ Hao Huang, haohuang@hubu.edu.cn; Shenli Wang, 457858016@qq.com; Zhigao Wang, 794022273@qq.com; Xuan Wang, 1971119889@qq.com; Huan Xia, 1375205463@qq.com; Qian Wang, 328418994@qq.com; Peng Duan, 3806393277@qq.com; Feiyu Leng, 491369000@qq.com; Jing Tian, hao1988@126.com; Wai-Hung Ip, wh.ip@polyu.edu.hk; Kai-Leung Yung, kl.yung@polyu.edu.hk | [1]State Grid Hubei Extra High Voltage Company, Wuhan 430050, China. [2]Hubei Super-Energic Electric Power Co., Ltd., Wuhan 430050, China. [3]Hubei Key Lab of Micro-Nanoelectronic Materials and Devices, Faculty of Microelectronics, Hubei University, Wuhan 430062, China. [4]Department of Industrial and Systems Engineering, The Hong Kong Polytechnic University, Hong Kong 100872, China.

1 Introduction

In order to improve the country's comprehensive national strength and seize space resources, the space activities include space technology, space applications and space science has continued to develop [1, 2]. Among them, space technology refers to the comprehensive engineering technology that provides technical means and guarantee conditions for space activities. Space application refers to the use of space technology and space resources developed in the fields of scientific research, national economy, national defense construction, culture and education. Space resources refer to various environmental, energy and material resources available for human development and utilization outside the Earth's atmosphere, as well as material resources of celestial bodies such as high space position, high vacuum, ultra-low temperature, strong radiation, microgravity environment and solar energy outside the earth [3–5]. As space activities become more competitive, the new space systems requirements such as increased functionality and reduced volume make the need for advanced microelectronic devices even more urgent.

The core hardware chip of electronic equipment is completed with fundamental transistors after a variety of processes to realize multiple functions [6–8]. In order to meet the demand, it is necessary to reduce the feature size of transistors to improve the performance of the chips. When designing chips, it is common to integrate devices and circuits into the smallest possible area in order to produce cheaper, smaller, and faster electronic devices. With the continuous progress of the chip manufacturing process, the chip can be smaller and smaller, while becoming more powerful. But traditional Si device feature sizes have reached their limits. The size of the chip will also bring some problems, such as: increased production costs: if the size of the chip becomes larger, more materials are needed, and more manufacturing steps are required, which will increase the production cost. Heat dissipation problems: As the size increases, the heat generated by the chip will also increase, requiring a more powerful cooling system to cool the chip, which will make the device bulkier. Reduced integration: If devices and circuits are dispersed over a larger area, interference and signal loss between circuits will increase, affecting the performance and stability of the chip [9–13].

Therefore, in order to further improve device performance, it is necessary to find alternative materials for silicon or develop new principal devices. Among them, two-dimensional (2D) materials are candidates for a new generation because of their atomic thickness. In a wide variety of 2D materials, black phosphorus (BP) has excellent physical properties such as in-plane anisotropy, thickness-dependent direct band gap and high carrier mobility. Recent experiments have shown that few layer BP can be obtained by mechanical exfoliation for next-generation electronic and optical applications [14–17]. The band gap in BP depends on the number of layers, ranging from 0.3 eV in the bulk material to 2.0 eV in a single layer of phosphorene. [18–21] This wide band range is attractive because it fills the energy spectrum gap between zero-band gap graphene and relatively large band-gap transition metal disulfide compounds (TMDs), covering the visible to infrared range for optoelectronics [22–26]. In addition, BP is very attractive for electronic applications such as field-effect transistors (FETs). Few layers BP FETs are reported to have high carrier mobility, anisotropic transmission, high on/off ratio, and high operating frequency [27–29]. More encouragingly, recent work based on atomically thin hexagonal boron nitride packages with few layers of black phosphorus has resulted in mobility approaching 6000 cm^2/Vs at low temperatures [30], and Shubnikov-de Haas oscillations and the quantum Hall effects [30–35] have been observed. Since all of these results are based on a metal-oxide semiconductor (MOS) structure with few layers BP, regulating the quality of this structure has broad implications for future development. Moreover, with the development of space technology, the performance demand for future aerospace electronics is greater. [36–38] The performance control will provide a feasible way for future aerospace applications.

In this paper, we explored N_2 plasma treatment to regulate the performance of BP FET devices. Both the power and duration of N_2 plasma affect the performance of the device. In order to determine the appropriate processing conditions, firstly, the device is treated with different power for a fixed period of time to study the performance changes before and after processing, and then the most appropriate processing time is determined by changing the processing time under the optimal power to achieve the optimal device performance. This simple and efficient doping technique provides a valuable way to realize high performance BP thin film transistors.

2 Methods

The BP bulks used in our article were purchased from Dutch HQ Graphene company through the dealer. A small number of BP flakes are stripped from the bulk crystal and then transferred to a heavily doped silicon substrate covered with a 300 nm SiO_2 layer by using mechanical stripping method to place the BP on the substrate. Subsequently, source/drain

metal contacts are formed by electron beam lithography (EBL) and a 20 nm/50 nm thick Cr/Au metal deposition and lift-off processes. The completed BP FET device was first electrically measured using the Keithley 4200 semiconductor parameter analyzer in a vacuum atmosphere. The measured samples were treated with N_2 plasma with different power and duration. After treatment, BP FETs were again electrically characterized under vacuum conditions.

The schematic diagram and optical micrograph of a BP FET with channel length of 2 μm are shown in Fig. 1a, b, respectively. On a 300nm silicon dioxide sheet, the two-dimensional material will appear different colors depending on the thickness. By empirically determining the thickness represented by the color, a thinner material can be selected as the channel material of the device. Here, BP is generally selected with a thickness of about 10 nm. Because the BP device will be briefly exposed to the air during the N_2 plasma treatment. 10 nm black phosphorus can ensure the normal operation of the device during the whole experiment. Figure 1c, d are scanning electron microscope (SEM) images of BP devices. In SEM images, 2D materials and electrodes can be clearly seen. The device presents very clean channels and electrodes at large magnification.

3 Results and discussion

A clear characteristic of p-type transistor behavior can be seen in the transfer characteristics of the few layers BP FET, as shown by the black line in Fig. 2. The value of Vd in Fig. 2 is − 1 V. Before N_2 plasma processing, the six typical devices are chosen to shown in Fig. 2, which exhibits typical p-type transistor behavior. The prepared devices were divided into three groups and treated with 10W, 20W and 30W plasma, respectively. The N_2 plasma treatment duration is set to 30 s. After processing, the device still maintains p-type characteristics. However, the performance of the BP FETs after N_2 plasma treatment is not fixed. When the N_2 plasma power is 10W and 30W, the conduction current of the device is unstable, and the off-state current is not consistent. The performance of the device varies inconsistently after 10W and 30W plasma treatment. However, when the processing power is 20W, the on-state current (Ion) and off-state current (Ioff) increase significantly. The on/off ratio is reduced. Figure 2 shows the typical characteristics of the devices after different power treatment.

In order to observe the effect of plasma power on the performance of the device more clearly, the electrical characteristic parameters of several devices are extracted. One of the more important applications of FET in logic circuits is current switching, which is turned on or off by gate voltage control devices. Then the current ratio of the device in the on state and the off state is the switching ratio, that is, Ion/Ioff. When the device is in the on state, the size of the leakage

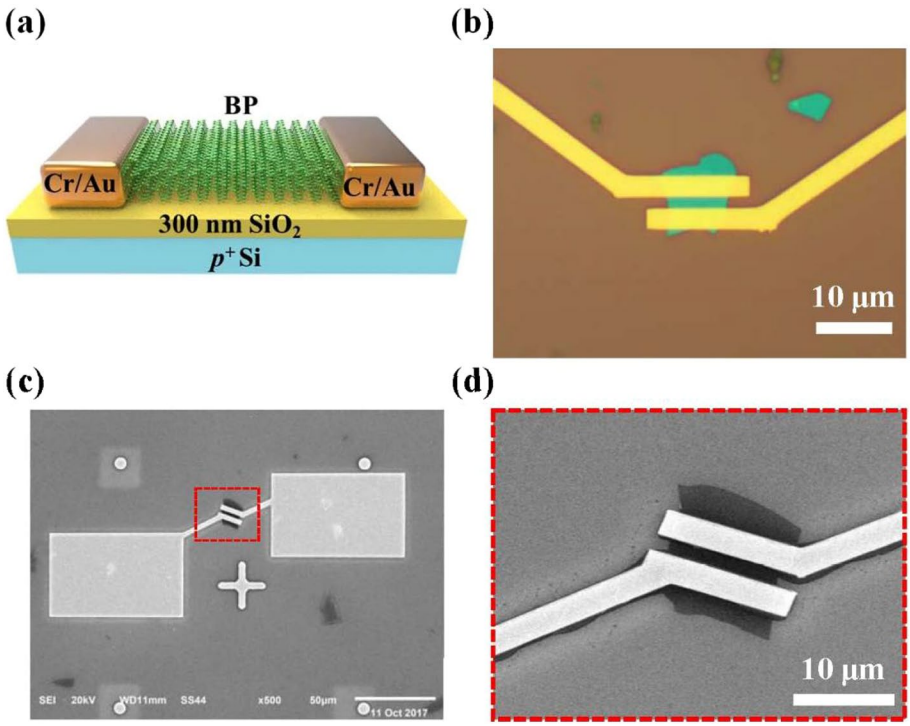

Fig. 1 **a** The schematic diagram of the device structure. **b** The optical microscope image of the BP FET. **c** SEM images of the BP FET. **d** The SEM image magnification

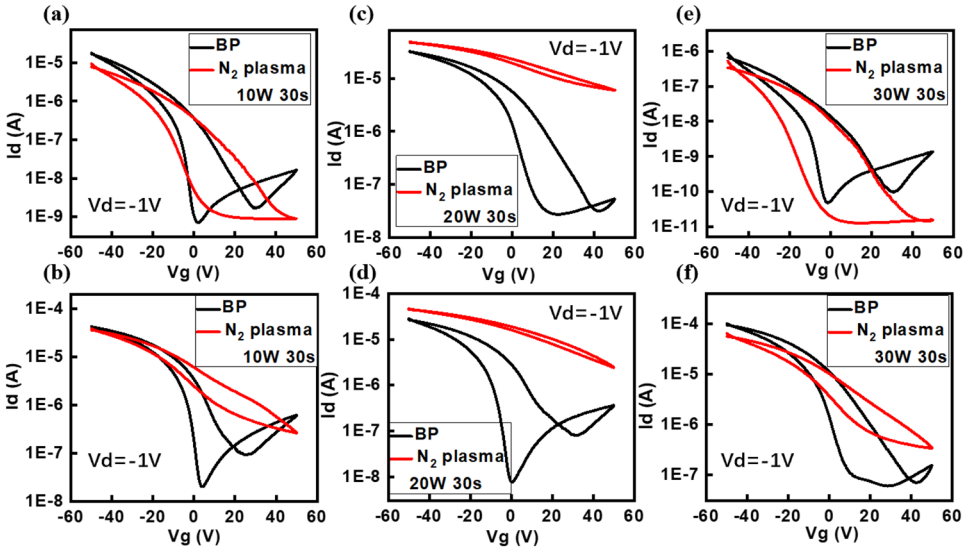

Fig. 2 **a**-**b** The transfer curves of the BP FET without and with 10W N_2 plasma treatment for 30s. **c**-**d** The transfer curves of the BP FET without and with 20W N_2 plasma treatment for 30s. **e**–**f** The transfer curves of the BP FET without and with 30W N_2 plasma treatment for 30s

current is the on-state current Ion, which will affect the running speed of the device. When the device is in the off state, the leakage current is the off state current Ioff, and the off-state current will affect the power consumption of the device. The transistor can be regarded as a faucet, then the switch ratio is equivalent to the water flow ratio of the water and the water off, the greater the water flow, the higher the efficiency of the faucet, the smaller the water flow, the less waste, the faucet has played a role in turning off. If the faucet is turned off, there is still water dripping continuously, then the quality of the faucet is not good at this time and needs to be replaced. The larger the switch ratio in logic device, the better the device performance.

For the convenience of comparison, the device performance change rates of 15 devices are given in Fig. 3.

In Fig. 3a, the ratio of the on-state current of the black phosphorus transistor after treatment and before treatment is taken as the vertical axis for ease of comparison. It can be clearly seen that the influence of 10W processing on the conduction current of the device is uncertain, while the open-state current of the device is reduced by 30W processing. Only the Ion of the 20W treated device is increased, and the increase factor is > 1.2.

Figure 3b shows the change of the ratio of the off-state current of the black phosphorus transistor with the processing power after treatment and before treatment. It is noted that 20W N_2 plasma processing has the greatest influence on the off-state current of the device, which can reach up to 300 times of the original current. N_2 plasma mainly affect the channel surface of black phosphorus devices, increasing surface defects and impurities. From our experimental results, the threshold of the device moves forward and the p terminal current increases, indicating that the device is indeed p-doped. Thus, N ions are also inserted into the BP lattice to form p-type doping of the channel [39, 40]. However, the conductive channel of the BP FET is mainly at the lower interface. When the power is small, the change of the channel surface has a little effect on the conduction channel at the lower interface, which results in erratic performance changes. As the power increases to 20W, the interface defects increase, and the doping of N ions also increases. Thus, the p-type doping effect of current increases obviously and consistently. When the power is further increased to 30W, the plasma damages the channel lattice of the device, and the damage of the channel material leads to the performance attenuation of the device.

In Fig. 3c, the switching ratio of the device after 30W treatment is significantly smaller than that of the other two, indicating that the performance of the device is indeed attenuated due to material damage.

Figure 3d shows the change of the field effect mobility of the device after treatment, in which the mobility of the 10W treatment has the largest fluctuation range, indicating that the treatment effect is unstable. With the increase of power, the variation range of mobility decreases and the treatment effect becomes more consistent. The field-effect mobility (μ) of the device can be calculated by the following formula:

$$\mu = \frac{1}{C_i} g_m \frac{L}{W} \frac{1}{V_d} \tag{1}$$

where g_m is transconductance, which defined as $g_m = d(Id)/d(Vg)$, L is the channel length, W is the channel width, C_i is the capacitance of the back gate, and V_d is the source and drain bias. Mobility is used to characterize the average drift velocity

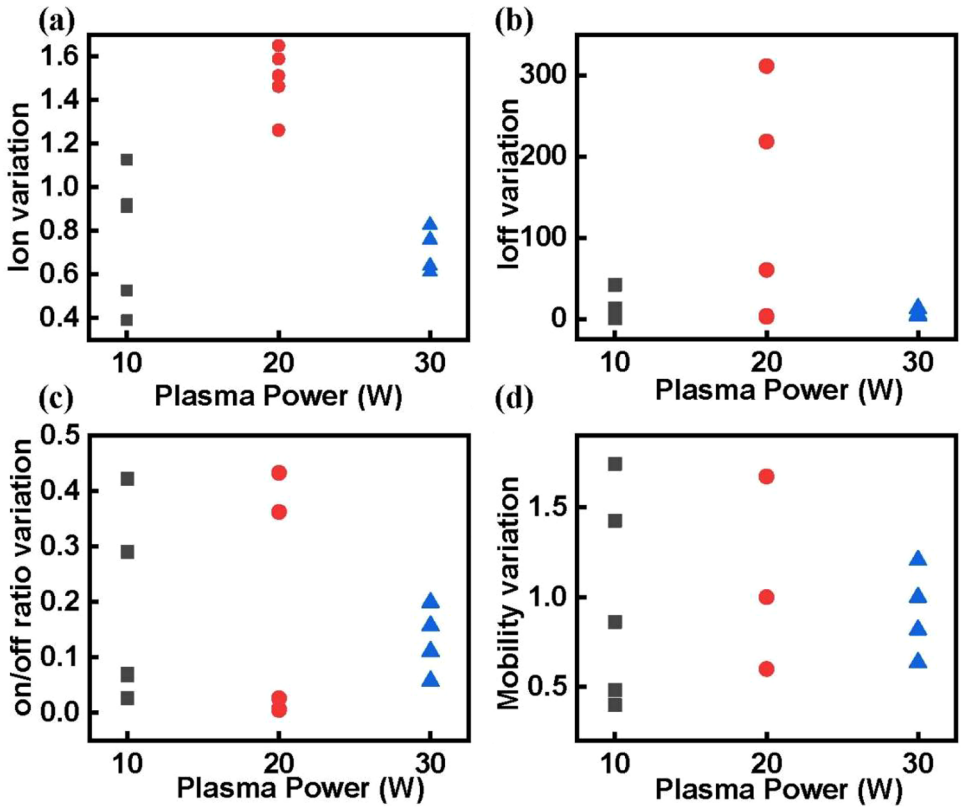

Fig. 3 **a** The change of on-state current ratio with power before and after N_2 plasma treatment. **b** The change of off-state current ratio with power before and after N_2 plasma treatment. **c** The change of on/off current ratio with power before and after N_2 plasma treatment. **d** The change of mobility ratio with power before and after N_2 plasma treatment

of carriers in a semiconductor under the action of a unit electric field. For a practical device, mobility is an important performance consideration. Similar to the water discharge speed of a faucet, under the same water pressure per unit area per unit time, the more and faster the water is discharged, the more efficient and useful it will be in line with our definition. Then, for a high-performance electronic device, the faster the carrier drift speed, the faster the device runs, the better the performance. FET as the basic unit operation speed increase, the entire integrated circuit to the chip to the electronic products of the computing and processing information ability will be accelerated, the higher the efficiency of electronic products, the better the product performance, the more to meet the needs of the market. Among them, the ratio of the 30W N_2 plasma treatment approaches 1, which indicating that the improvement is not undesirability. Overall consideration, 20W N_2 plasma treatment is the best one.

In order to further investigate the effect of processing time on device performance, we chose to use 20W N_2 plasma to process the same device multiple times. The cumulative duration is used as the total duration.

In Fig. 4a, the transfer characteristic curves of BP FET treated with different time periods were compared. It can be obviously seen that the on-state current and off-state current of the device increase with the increase of the time, but the device characteristics after treatment are significantly reduced when the time exceeds 50 s, indicating that the processing time of 70 s has damage to the device. When the N_2 plasma duration is suitable, the treatment will improve the performance of the devices. When the treatment duration exceeds a certain limit, the material will be damaged and the performance will be reduced.

Figure 4b–f shows the corresponding output characteristic curves of the devices processed for different duration. The value of V_g in the output characteristics is from 0 V, − 10 V, − 20 V, − 30 V, − 40 V and − 50 V, respectively. It is obvious that the off-state current of the devices after processing is relatively large. The maximum current first increases with the increase of the processing time, and then decreases with the increase of the processing time after more than 50 s.

Table 1 is the summary of the characteristics of recent BP transistors. BP has excellent physical properties. Since the intrinsic properties of black phosphorus depend on black phosphorus materials, the basic properties of different produced materials are inconsistent. Thus, we mainly discuss a change comparison of our devices before and after processing to highlight the role of N_2 plasma. As shown in the Table 1, the performance of our work is in the normal range in recent studies. Our devices range in mobility from 31 to 304 $cm^2/V{\cdot}s$.

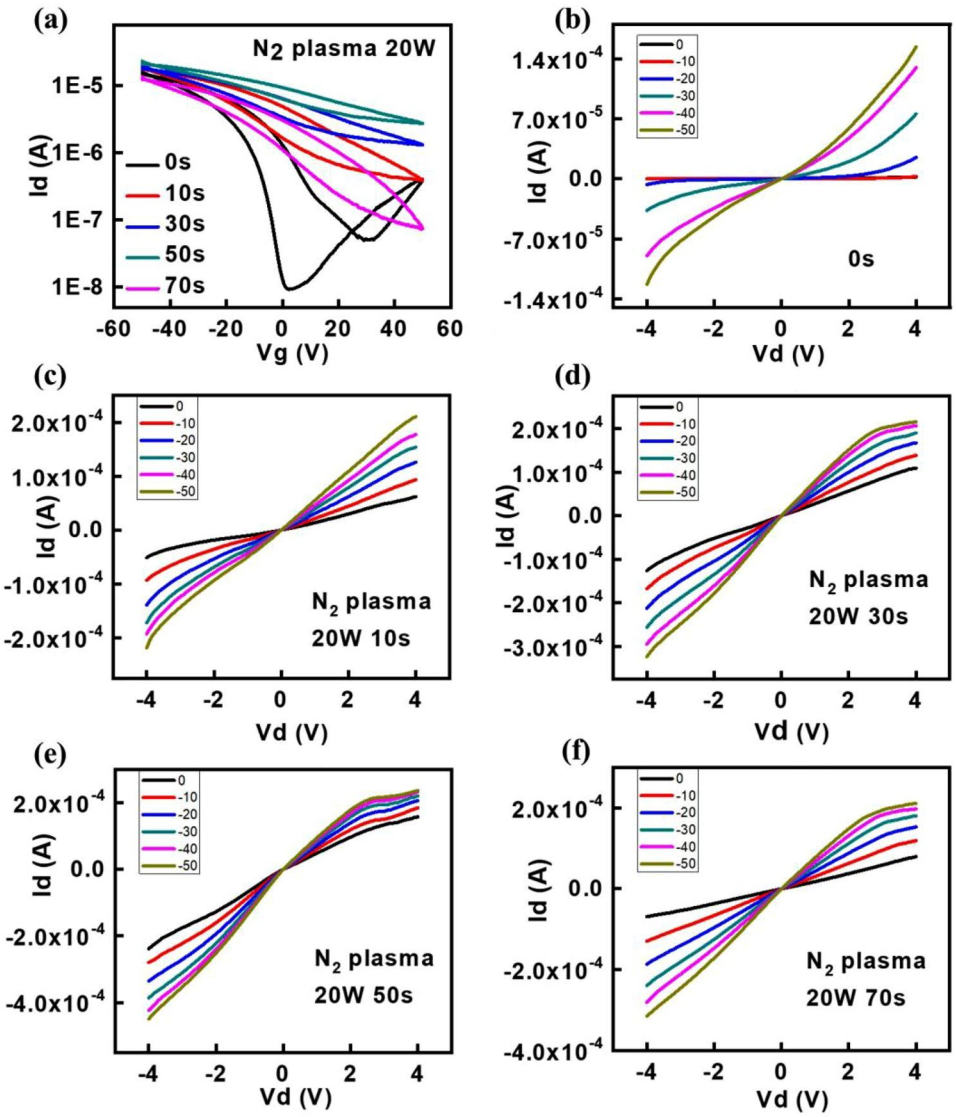

Fig. 4 **a** The transfer curves of the BP FET with 20W N_2 plasma treatment for 0s, 10s, 30s, 50s, and 70s, respectively. The output characteristic curves of the BP FET with 20W N_2 plasma treatment for 0s (**b**), 10s (**c**), 30s (**d**), 50s (**e**), and 70s (**f**), respectively

4 Conclusion

In summary, in order to meet the high-performance requirements of electronic devices for the implementation of new space systems, we explored N_2 plasma treatment to regulate the performance of BP FET devices. N_2 plasma can effectively

Table 1 Summary of characteristics of recent BP transistors

Film thickness (nm)	Gate insulator	On/off ratio	Mobility ($cm^2V^{-1}s^{-1}$)	Refs.
5	SiO_2	10^4	286	[41]
5	SiO_2	10^4	155	[42]
1.6	SiO_2	600	35	[43]
–	SiO_2	10^5	116	[44]
–	SiO_2	10^3	100	[45]
–	SiO_2	1.6×10^4	25.9	[46]
10.7 ± 0.8	HfO_2	1.2 × 103	44	[47]
–	SiO_2	2×10^3–7×10^4	31–304	Our work

improve the on-state current and mobility of the device. Better doping techniques are essential to further improve the transport performance of materials, including BP. It lays the hardware foundation for the application of subsequent devices in aerospace technology and space informatics.

Acknowledgements Acknowledgement is also given to the Hong Kong Polytechnic University, project code: WZ0W.

Author contributions Conceptualization, S.W., Z.W., X.W. and H.X.; methodology, S.W. and H.H.; software, S.W. and Q.W.; validation, Z.W., P.D. and F.L.; formal analysis, H.H. and W.-H.I.; investigation, S.W., Z.W., J.T. and K.-L.Y.; resources, X.W. and W.-H.I.; data curation, S.W. and H.H.; writing—original draft preparation, S.W., H.H. and W.-H.I.; writing—review and editing, Z.W., P.D., J.T. and K.-L.Y.; visualization, S.W., Q.W. and P.D.; supervision, K.-L.Y.; project administration, H.H. and W.-H.I.; funding acquisition, S.W., H.H. and W.-H.I.. All authors have read and agreed to the published version of the manuscript.

Funding This work is supported by Hubei Provincial Science and Technology Plan Project (2023BBB060) and the Educational Commission of Hubei Province (Q20221006). The work was supported in part by the Research Center for Deep Space Explorations of the Hong Kong Polytechnic University.

Data availability All data generated or analyzed during this study are included in this published article. Information on the datasets generated during and/or analyzed during the current study is available from the corresponding author on reasonable request.

Declarations

Competing interests Authors S.W., Z.W., X.W., H.X., Q.W., P.D., F.L. and J.T. were employed by the companies State Grid Hubei Extra High Voltage Company and Hubei Super-energic Electric Power Co., Ltd.. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

References

1. Erickson AS, Walsh KA. National security challenges and competition: Defense and space R&D in the Chinese strategic context. Technol Soc. 2008;30(3–4):349–61.
2. Board, Space Studies, and National Research Council.Earth science and applications from space: national imperatives for the next decade and beyond. National Academies Press, 2007.
3. Fortescue P, Swinerd G, Stark J. Spacecraft systems engineering. Hoboken: John Wiley & Sons; 2011.
4. Allen V, James A. Space science, space technology and the space station. Sci Am. 1986;254(1):32–9.
5. Ley W, Wittmann K, Hallmann W. Handbook of space technology. Hoboken: John Wiley & Sons; 2009.
6. Wilkinson NJ, Smith MAA, Kay RW, et al. A review of aerosol jet printing—a non-traditional hybrid process for micro-manufacturing. Int J Adv Manuf Technol. 2019;105:4599–619. https://doi.org/10.1007/s00170-019-03438-2.
7. Jiang L, Kunieda M. Realization of high discharge frequency in LC pulse generator for EDM by ignition using transistor circuit. Int J Adv Manuf Technol. 2023;126:2607–16. https://doi.org/10.1007/s00170-023-11286-4.
8. Yang T, Kuo Y, Hsieh CH, et al. An exploratory study of virtual cell design for thin-film transistor–liquid crystal display (TFT-LCD) array manufacturing. Int J Adv Manuf Technol. 2016;83:633–44. https://doi.org/10.1007/s00170-015-7588-y.
9. Oliveira De, Brandão F, et al. Size effect and minimum chip thickness in micromilling. Int J Mach Tools Manuf. 2015;89:39–54.
10. Zhou D, Liu XY. Minimization of chip size and power consumption of high-speed VLSI buffers. Proceedings of the 1997 international symposium on Physical design. 1997.
11. Chaudhry A, Jagadesh Kumar M. Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review. IEEE Trans Dev Mater Reliab. 2004;4(1):99–109.
12. Požela J. Technological and physical limitations on transistor miniaturization. In: Požela J, editor. Physics of high-speed transistors. Boston: Springer; 1993. p. 35–47.
13. Keyes RW. Physical limits of silicon transistors and circuits. Rep Prog Phys. 2005;68(12):2701.
14. Li L, Yu Y, Ye GJ, Ge Q, Ou X, Wu H, Feng D, Chen XH, Zhang Y. Black phosphorus field-effect transistors. Nat Nanotech. 2014;9:372–7. https://doi.org/10.1038/nnano.2014.35.
15. Xia F, Wang H, Jia Y. Rediscovering black phosphorus as an anisotropic layered material for optoelectronics and electronics. Nat Commun. 2014;21(5):4458. https://doi.org/10.1038/ncomms5458.
16. Liu H, Neal AT, Zhu Z, Luo Z, Xu X, Tomanek D, Ye PD. Phosphorene: an unexplored 2D semiconductor with a high hole mobility. ACS Nano. 2014;8(4):4033–41. https://doi.org/10.1021/nn501226z.
17. Liu Y, Low T, Paul Ruden P. Mobility anisotropy in monolayer black phosphorus due to scattering by charged impurities. Phys Rev B. 2016;93:165402. https://doi.org/10.1103/PhysRevB.93.165402.

18. Qiao J, Kong X, Hu Z-X, Yang F, Ji W. High-mobility transport anisotropy and linear dichroism in few-layer black phosphorus. Nat Commun. 2014;21(5):4475. https://doi.org/10.1038/ncomms5475.
19. Tran V, Soklaski R, Liang Y, Yang L. Layer-controlled band gap and anisotropic excitons in few-layer black phosphorus. Phys Rev B. 2014;89:235319. https://doi.org/10.1103/PhysRevB.89.235319.
20. Akahama Y, Endo S, Narita S-I. Electrical properties of black phosphorus single crystals. J Phys Soc Jpn. 1983;52:2148–55. https://doi.org/10.1143/JPSJ.52.2148.
21. Liu H, Du Y, Deng Y, Ye PD. Semiconducting black phosphorus: synthesis, transport properties and electronic applications. Chem Soc Rev. 2015;44(9):2732–43. https://doi.org/10.1039/C4CS00257A.
22. Churchill HOH, Jarillo-Herrero P. Two-dimensional crystals: phosphorus joins the family. Nat Nanotechnol. 2014;9(5):330–1. https://doi.org/10.1038/nnano.2014.85.
23. Xia F, Wang H, Xiao D, Dubey M, Ramasubramaniam A. Two-dimensional material nanophotonics. Nat Photon. 2014;8:899–907. https://doi.org/10.1038/nphoton.2014.271.
24. Buscema M, Groenendijk DJ, Blanter SI, Steele GA, van der Zant HSJ, Castellanos-Gomez A. Fast and broadband photoresponse of few-layer black phosphorus field-effect transistors. Nano Lett. 2014;14(6):3347–52. https://doi.org/10.1021/nl5008085.
25. Youngblood N, Chen C, Koester SJ, Li M. Waveguide-integrated black phosphorus photodetector with high responsivity and low dark current. Nat Photon. 2015;9:247–52. https://doi.org/10.1038/nphoton.2015.23.
26. Huang M, Wang M, Chen C, Ma Z, Li X, Han J, Wu Y. Broadband black-phosphorus photodetectors with high responsivity. Adv Mater. 2016;28(18):3481–5. https://doi.org/10.1002/adma.201506352.
27. Liu X, Ang KW, Yu W, He J, Feng X, Liu Q, Jiang H, Tang D, Wen J, Lu Y, Liu W, Cao P, Han S, Wu J, Liu W, Wang X, Zhu D, He Z. Black phosphorus based field effect transistors with simultaneously achieved near ideal subthreshold swing and high hole mobility at room temperature. Sci Rep. 2016;6:24920.
28. Yang B, Wan B, Zhou Q, Wang Y, Hu W, Lv W, Chen Q, Zeng Z, Wen F, Xiang J, Yuan S, Wang J, Zhang B, Wang W, Zhang J, Xu B, Zhao Z, Tian Y, Liu Z. Te-doped black phosphorus field-effect transistors. Adv Mater. 2016;28:9408–15.
29. Illarionov YY, Waltl M, Rzepa G, Kim JS, Kim S, Dodabalapur A, Akinwande D, Grasser T. Long-term stability and reliability of black phosphorus field-effect transistors. ACS Nano. 2016;10:9543–9.
30. Li L, Yang F, Ye G, Zhang Z, Zhu Z, Lou W-K, Li L, Watanabe K, Taniguchi T, Chang K, Wang Y, Chen X, Zhang Y. Quantum Hall effect in black phosphorus two-dimensional electron gas. Nature Nanotechnol. 2015;11(7):592–6.
31. Xiang ZJ, Ye GJ, Shang C, Lei B, Wang NZ, Yang KS, Liu DY, Meng FB, Luo XG, Zou LJ, Sun Z, Zhang YB, Chen XH. Pressure-induced Lifshitz transition in black phosphorus. Phys Rev Lett. 2015;115:186403.
32. Li L, Ye G, Tran V, Fei R, Chen G, Wang H, Wang J, Watanabe K, Taniguchi T, Yang L, Chen X, Zhang Y. Quantum oscillations in a two-dimensional electron gas in black phosphorus thin film. Nature Nanotechnol. 2015;10(7):608–13. https://doi.org/10.1038/nnano.2015.91.
33. Gillgren N, Wickramaratne D, Shi Y, Espiritu T, Yang J, Hu J, Wei J, Liu X, Mao Z, Watanabe K, Taniguchi T, Bockrath M, Barlas Y, Lake RK, Lau CN. Gate tunable quantum oscillations in air-stable and high mobility few-layer phosphorene heterostructures. 2D Mater. 2014;2(1):011001. https://doi.org/10.1088/2053-1583/2/1/011001.
34. Chen X, Wu Y, Wu Z, Han Y, Xu S, Wang L, Ye W, Han T, He Y, Cai Y, Wang N. High quality sandwiched black phosphorus heterostructure and its quantum oscillations. Nat Commun. 2015. https://doi.org/10.1038/ncomms8315.
35. Cao Y, Mishchenko A, Yu G, Khestanova K, Rooney AP, Prestat E, Kretinin AV, Blake P, Shalom M, Woods C, Chapman J, Balakrishnan G, Grigorieva IV, Novoselov KS, Piot BA, Potemski M, Watanabe K, Taniguchi T, Haigh SJ, Geim AK, Gorbachev RV. Quality heterostructures from two-dimensional crystals unstable in air by their assembly in inert atmosphere. Nano Lett. 2015;15(8):4914–21. https://doi.org/10.1021/acs.nanolett.5b00648.
36. Galloway KF, Witulski AF, Schrimpf RD, Sternberg AL, Ball DR, Javanainen A, Reed RA, Sierawski BD, Lauenstein J-M. Failure estimates for SiC power MOSFETs in space electronics. Aerospace. 2018;5:67. https://doi.org/10.3390/aerospace5030067.
37. Aguiar YQ, Wrobel F, Autran J-L, Leroux P, Saigné F, Pouget V, Touboul AD. Mitigation and predictive assessment of SET immunity of digital logic circuits for space missions. Aerospace. 2020;7:12. https://doi.org/10.3390/aerospace7020012.
38. O'Reilly D, Herdrich G, Schäfer F, Montag C, Worden SP, Meaney P, Kavanagh DF. A coaxial pulsed plasma thruster model with efficient flyback converter approaches for small satellites. Aerospace. 2023;10:540. https://doi.org/10.3390/aerospace10060540.
39. Azcatl A, Qin X, Prakash A, Zhang C, Cheng L, Wang Q, Wallace RM. Covalent nitrogen doping and compressive strain in MoS2 by remote N2 plasma exposure. Nano Lett. 2016;16(9):5437–43.
40. Zeng Y, Zeng X, Wang S, Hu Y, Wang W, Yin S, Ren T, Zeng Y, Lu J, Guo W. Low-damaged p-type doping of MoS2 using direct nitrogen plasma modulated by toroidal-magnetic-field. Nanotechnology. 2019;31(1): 015702.
41. Liu H, Neal AT, Zhu Z, Luo Z, Xu X, Tománek D, Ye PD. Phosphorene: an unexplored 2D semiconductor with a high hole mobility. ACS Nano. 2014;8(4):4033–41.
42. Kamalakar MV, Madhushankar BN, Dankert A, Dash SP. Low Schottky barrier black phosphorus field-effect devices with ferromagnetic tunnel contacts. Small. 2015;11(18):2209–16.
43. Castellanos-Gomez A, Vicarelli L, Prada E, Island JO, Narasimha-Acharya KL, Blanter SI, Van Der Zant HS. Isolation and characterization of few-layer black phosphorus. 2D Materials. 2014;1(2):025001.
44. Das S, Zhang W, Demarteau M, Hoffmann A, Dubey M, Roelofs A. Tunable transport gap in phosphorene. Nano Lett. 2014;14(10):5733–9.
45. Buscema M, Groenendijk DJ, Blanter SI, Steele GA, Van Der Zant HS, Castellanos-Gomez A. Fast and broadband photoresponse of few-layer black phosphorus field-effect transistors. Nano Lett. 2014;14(6):3347–52.
46. Kang J, Wood JD, Wells SA, Lee JH, Liu X, Chen KS, Hersam MC. Solvent exfoliation of electronic-grade, two-dimensional black phosphorus. ACS Nano. 2015;9(4):3596–604.
47. Haratipour N, Robbins MC, Koester SJ. Black phosphorus p-MOSFETs with 7-nm HfO 2 gate dielectric and low contact resistance. IEEE Electron Dev Lett. 2015;36(4):411–3.