Black phosphorus/ferroelectric P(VDF-TrFE) field-effect transistors with high mobility for energy-efficient artificial synapse in high-accuracy neuromorphic computing

Zhaoying Dang [a b], Feng Guo [a c], Huan Duan [d], Qiyue Zhao [e], Yuxiang Fu [e], Wenjing Jie [d*], Kui Jin [b], and Jianhua Hao [a* c]

[a] Department of Applied Physics, The Hong Kong Polytechnic University, Hung Hom, Hong Kong 999077, China

[b] Songshan Lake Materials Laboratory, Dongguan, Guangdong 523808, China

[c] The Hong Kong Polytechnic University Shenzhen Research Institute, Shenzhen 518057, China

[d] College of Chemistry and Materials Science, Sichuan Normal University, Chengdu, Sichuan 610066, China

[e] School of Integrated Circuits, Nanjing University, Nanjing, Jiangsu 210093, China

[*]Email: wenjing.jie@sicnu.edu.cn, jh.hao@polyu.edu.hk

Abstract:

The neuromorphic system becomes an attractive platform for next-generation computing with low power and fast speed to emulate knowledge-based learning. Here, we design ferroelectric-tuned synaptic transistors by integrating 2D black phosphorus (BP) with flexible ferroelectric copolymer poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)). Through nonvolatile ferroelectric polarization, the P(VDF-TrFE)/BP synaptic transistors show a high mobility value of 900 $cm^2 V^{-1} s^{-1}$ with 10^3 on/off current ratio and can operate with low energy consumption down to femtojoule level (~40 fJ). Reliable and programmable synaptic behaviors have been demonstrated, including paired-pulse facilitation, long-term depression, and potentiation. The biological memory consolidation process is emulated through ferroelectric gate-sensitive neuromorphic behaviors. Inspiringly, the artificial neural network is simulated for handwritten digits recognition, achieving high recognition accuracy of 93.6%. These findings highlight the prospects of 2D ferroelectric field-effect transistors as ideal building blocks for high-performance neuromorphic networks.

KEYWORDS: *ferroelectric polymer, 2D semiconductors, synaptic transistors, neuromorphic computing, nonvolatile memory devices*

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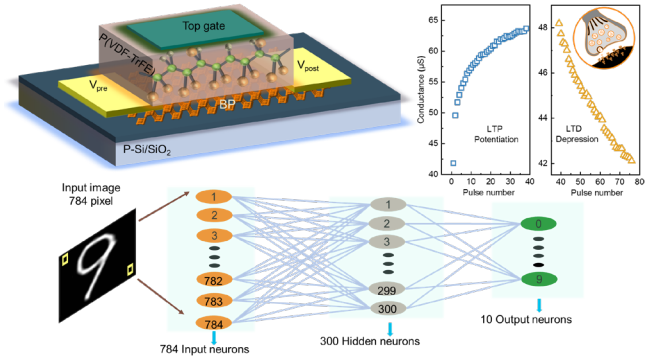

As fundamental links among 10^{11} neurons, biological synapses enable storing and processing information simultaneously through tuning the synaptic plasticity.[1-3] Such functionalities enlighten researchers to break von Neumann architecture and blur the boundary between memory and logic units,

leading to in-memory computing. The neuromorphic system has been proposed to perform computing and memory simultaneously like human brain.[4-5] As basic units of neuromorphic system, artificial synaptic transistors can simulate typical plasticity characteristics.[6-7] Among of various neuron concept devices,[8-10] 2D ferroelectric field-effect transistors (FeFETs) have been widely used because the ferroelectric gates can provide high doping-density, reversible and nonvolatile modulation of channel carriers, and fast memory operations.[11]

Compared with ferroelectric oxide-based synapse transistors,[12] organic ferroelectrics represented by copolymer P(VDF-TrFE) hold significant advantages, such as low crystallization temperature, accessible fabrication method, and high flexibility.[13-14] Extensive efforts have been devoted to investigating polymer-based FeFETs onto 2D semiconductors with van der Waals (vdWs) interface contact for developing neural network. However, the related works usually involved low mobility 2D nanosheets such as ambipolar $MoTe_2$ or n-type MoS_2 and small conductance variations, which circumvent applications for energy-efficient and high-accuracy neuromorphic computing.[15-16]

Herein, by combining p-type and high mobility BP with ferroelectric copolymer P(VDF-TrFE), we demonstrate three-terminal ferroelectric synaptic transistors. Notably, the developed FeFETs have exhibited high mobility of 900 $cm^2 V^{-1} s^{-1}$ and large on/off ratio of 10^3. Besides, femtojoule-level energy consumption for per pulse event is realized for state-of-the-art artificial synapses. The synaptic behaviors, including long-term potentiation (LTP), long-term depression (LTD), paired-pulse facilitation (PPF), and memory consolidation process under ferroelectric gate adjustment, have also been studied. Remarkably, the hardware neural network is simulated for pattern recognitions with high accuracy of 93.6%. With high carrier mobility and large conductance variation, the presented ferroelectric synaptic transistors show promise toward energy-efficient applications for in-memory computing cells.

Fig. 1(a) displays the three-terminal architecture of FeFETs based on P(VDF-TrFE)/BP devices and the third terminal imposes signals. Detailed device fabrication process is demonstrated in Supplementary Note. 1 and Fig. S1. Ferroelectric layer P(VDF-TrFE) is a copolymer combining two homopolymers (Fig. 1(a)). The ferroelectric polarization in P(VDF-TrFE) films origins from opposite direction of dipole moments. Solution-based spin-coating fabrication method for P(VDF-TrFE) films followed by a low-temperature annealing process contributes to increasing crystallinity and developing clean interface.[17] Biological synapses operations are based on the ferroelectric effect of P(VDF-TrFE) and the tunable polarity of the BP channels.

Here, we first clarify the working mechanism of ferroelectric effect on the active channel. Figure 1(b) illustrates the mechanism of controlling BP channel based on ferroelectric polarization. If the P(VDF-TrFE) layer is polarized upward under negative voltage, the majority carriers (holes) in the p-type BP channel are fully accumulated (Fig. S2), and the barrier narrows to δ_1 (Top panel of Fig. 1(c)). Meanwhile, holes in the BP channel will readily cross from the source to the drain, resulting in high drain current. On the contrary, carriers in the BP channel are exhausted if the P(VDF-TrFE) is polarized downward under positive gate voltage. The barrier height is enlarged to δ_2, hindering the carriers from crossing the barrier (Bottom panel of Fig. 1(c)). Therefore, drain current becomes much smaller, corresponding to the high resistance state. Fig. 1(d) shows the transfer characteristics of P(VDF-TrFE)/BP transistors at room temperature, including two states read by the low bias voltage. Due to the

ferroelectric insulator layer encapsulation of source−drain electrodes, the gate current is negligible compared with the drain current.

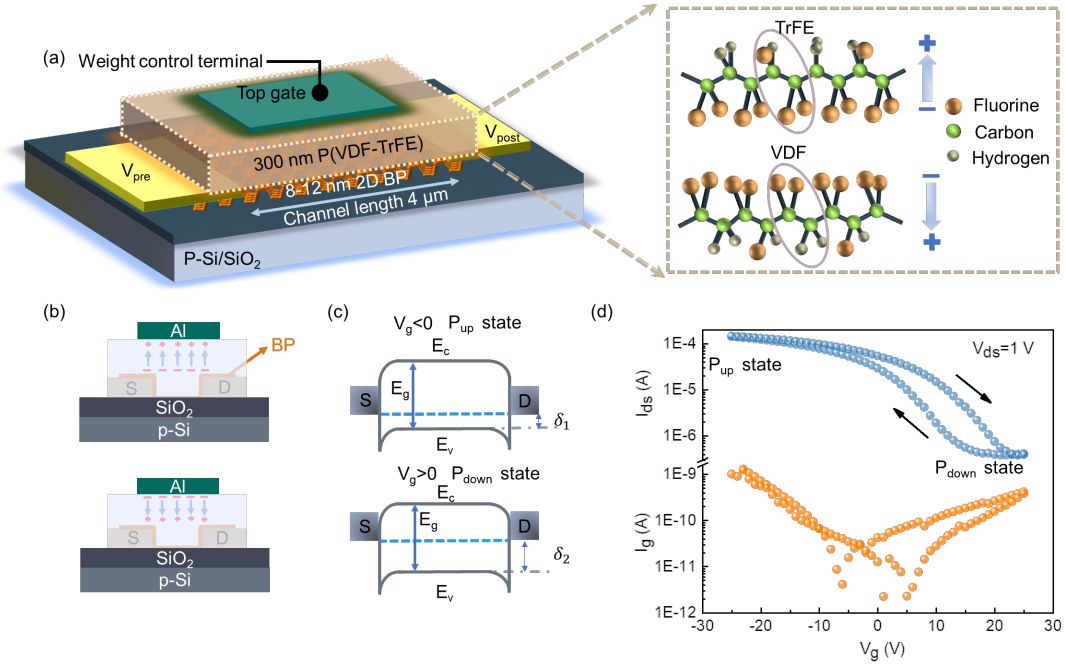

Figure 1. Device structure design and the working mechanism of P(VDF-TrFE)/BP-based organic FeFETs. (a) Schematic configuration of top-gate 2D FeFETs with P(VDF-TrFE) gate dielectric and BP channel. The right panel displays the chemical structure of P(VDF-TrFE) copolymer under opposite directions of dipole moments. (b) The cross-section structures of the device with dynamically modulating BP channel based on ferroelectric domain control. (c) Lateral energy band diagrams after experiencing the positive (top) and negative (bottom) voltage pulses. The E_c, E_V and E_g represent the minimum conduction band energy, maximum valence band energy, and bandgap of BP respectively. δ is the height from the bottom of the valence band to the Fermi level. δ_1 and δ_2 are related to the different polarization states. (d) The drain and gate currents tuned by P(VDF-TrFE) ferroelectric gate at room temperature.

The Raman spectroscopy confirms the structural quality of the transferred few-layered BP. Fig. 2a shows three typical characteristic peaks of A_{1g}, B_{2g}, and A_{2g}.[18] Atomic force microscopy (AFM) reveals a step-shaped texture (Fig. 2b). The thicknesses of BP used in FeFETs are approximately 8 nm (~13 layers) and 12 nm (~20 layers). X-ray diffraction (XRD) spectra with the prominent peak at 19.7º confirm the formation of β-phase with (200) plane in P(VDF-TrFE) films (Fig. 2(c)).[19] The spin-coating P(VDF-TrFE) films contain a high content of crystalline structure after low-temperature annealing. Furthermore, we note that the XRD peak intensity increases with the weight ratio of the solution, indicating that P(VDF-TrFE) films obtained from larger weight ratio solution possess a higher crystallinity. Taking the surface roughness and crystallization into account for synaptic device integration (Fig. S3), we fabricate P(VDF-TrFE) films with 6 wt% solution concentration and the thickness of the films is about 300 nm. Figure 2d presents the ferroelectric hysteresis loop of Al/P(VDF-TrFE)/Au capacitors, implying that the remnant polarization is about 4 μC/cm^2 and corresponding coercive voltage is ≈10 V. The piezoresponse force microscopy (PFM) measurement illustrates the

ferroelectric amplitude and phase, revealing the switching process of ferroelectric domain reversal.[20] Fig. 2(e) shows the contrast change in parallelogram-like piezoelectric response from the Phase 1 channel and butterfly-like amplitude loops indicate that the polarity of P(VDF-TrFE) films are forced up or down under writing voltage. Measurement setup of PFM and phase hysteresis loop from the Phase 2 channel are exhibited in Fig. S4. By applying a set of opposite voltage pulses, the P(VDF-TrFE) films demonstrate clear contrast between downward and upward polarized domains after biased-tip scanning (Fig. 2(f)).[21]

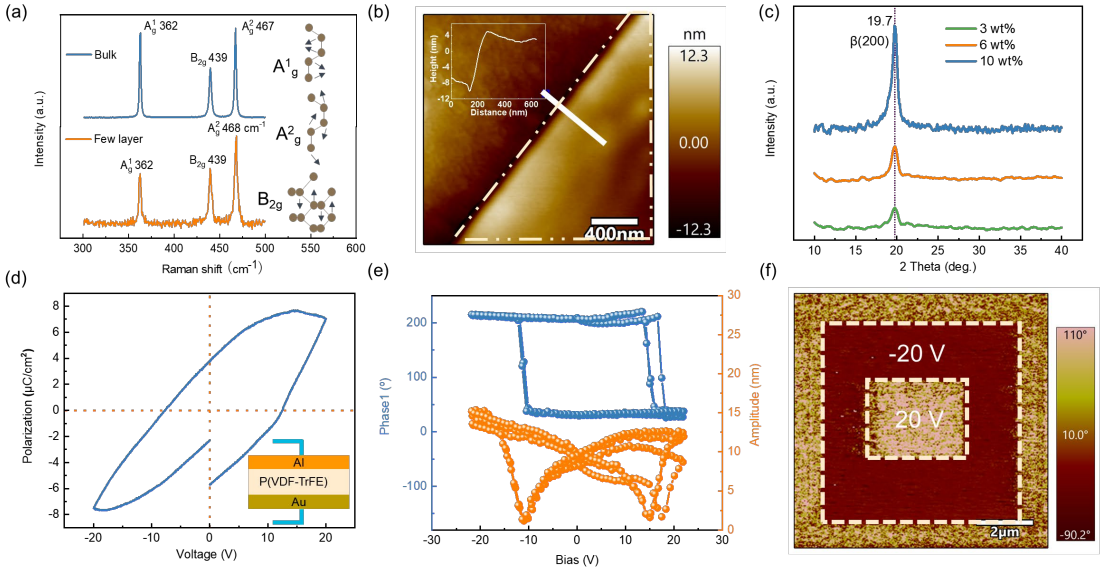

Figure 2. Characterization of the BP flakes and ferroelectric copolymer P(VDF-TrFE) films. (a) Raman spectra of the bulk and few layered BP. (b) Surface topographic images of BP. Inset: AFM step-height profiles. (c) XRD analysis results of P(VDF-TrFE) copolymer films fabricated under different solution concentration of 3 wt% ratio, 6 wt% ratio, and 10 wt% ratio. (d) Polarization-electric field hysteresis loop of the Al/P(VDF-TrFE)/Au capacitors at the test frequency of 100 Hz. (e) The amplitude and phase hysteresis loops of P(VDF-TrFE) films. (f) PFM images of P(VDF-TrFE)/Pt (Pt bottom electrode). The "box-in-box" ferroelectric domain pattern is written with +20V and -20 V tip bias.

Prior to synaptic functions investigation, we characterize the transport properties of FeFETs. Fig. 3(a) shows the cross-sectional view of three-terminal FeFETs with electrical probe settings for measurements. The output characteristics are exhibited in Fig. 3(b), where the drain current increases considerably when the gate voltage changes from positive to negative. Linear output characteristics indicate that good ohmic contacts are formed at the contact region between electrodes and BP. Fig. S5 illustrates the dual-sweep output curves and presents negligible hysteresis. Fig. 3(c) shows the collective results of the drain current when the gate voltage is swept from ±10 V to ±30 V in 5 V steps. The transport characteristics can be sorted into two parts: BP channel is turned on as the gate voltage sweeps from zero to the negative direction when P(VDF-TrFE) copolymer is polarized up. If the voltage is swept back to the positive direction, BP channel is fully depleted and P(VDF-TrFE) copolymer is polarized down. Therefore, the overall transfer curves show clockwise hysteresis direction and typical p-type transport behavior and ferroelectric polarization reversal plays a dominant role in regulating electrical transportation behaviors.

The ferroelectric hysteresis in transfer curves at forward and reverse bias voltages are both related to the ferroelectric polarization switching process. Therefore, Fig. 3(c) and 3(d) exhibit similar memory hysteresis loops. As the gate voltage is more than 10 V, memory windows are clearly observed because the larger gate voltage will result in a stronger polarization electric field in P(VDF-TrFE) films.[22] The minimum drain voltage for transfer curves can be set as 1 mV (Fig. 3(e)), which is meaningful for low-power nonvolatile memory operation and will be discussed later. It should be pointed out that BP-based FeFETs display high linear mobility value of 500 $cm^2 V^{-1} s^{-1}$ for 12 nm BP and 900 $cm^2 V^{-1} s^{-1}$ for 8 nm BP at room temperature (Fig. 2(f)) and carrier mobility values exhibit negligible differences for various gate voltage ranges (Fig. S6). Detailed transfer characteristics in linear scale for the two thicknesses can be found in Fig. S7. Overall, the demonstrated P(VDF-TrFE)/BP transistors have shown advantages in terms of reducing structure complexity, high carrier mobility, satisfactory memory properties, and stable electrical performance.

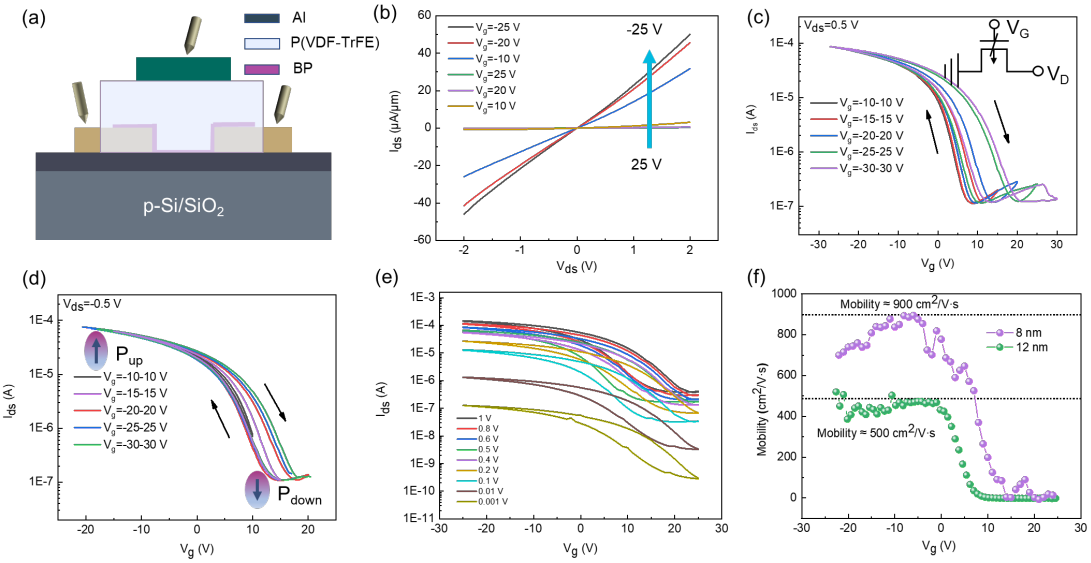

Figure 3. Transport properties for P(VDF-TrFE)/BP FeFETs. (a) Cross-section view of the P(VDF-TrFE)/BP FeFETs with probe position. (b) The output characteristics of the P(VDF-TrFE)/BP FeFETs, where top gate voltage varies from -25 V to 25 V. Drain current vs. top gate memory hysteresis loops of typical P(VDF-TrFE)/BP FeFETs under positive bias voltage of 0.5 V (c) and a negative bias voltage of -0.5 V (d) where top gate voltage varies from -30 V to 30 V with a step of 5 V. Inset: circuit diagram of P(VDF-TrFE)/BP transistors. The clockwise hysteresis windows expand with increasing top gate voltage, showing cumulative channel polarization. (e) Drain current vs. top gate memory hysteresis loops and displacement characteristics of P(VDF-TrFE)/BP FeFETs under various positive bias voltage. (f) Linear mobility plots of top gate P(VDF-TrFE)/BP FeFETs. All measurements are carried out at room temperature.

Given that P(VDF-TrFE) copolymer films enjoy successive and observable modulation of BP electrical transportation, which is the physical foundation for versatile synaptic plasticity. Next, the overall synaptic behavior of P(VDF-TrFE)/BP transistors will be discussed. A biological synapse transmits various electrical or chemical signal from the presynaptic terminal to the postsynaptic terminal by tuning neurotransmitter content (Fig. 4(a)).[23] In a three-terminal ferroelectric device, the gate

terminal acts as the presynaptic function for signal transmission, whereas the channel layer is the postsynaptic terminal, and stimuli from the gate terminal can modulate its behaviors. Therefore, the signal transmission and learning process can be carried out simultaneously.

As shown in Fig. 4(b), if one synaptic device is triggered by two electrical pulses, the postsynaptic current (PSC) induced by the second pulse is much higher (A2>A1) owing to the ferroelectric nonvolatility. Under the minimum time interval, the intensity difference between two PSC signals reaches the maximum and decreases gradually when time interval increases (Fig. 4(c)). PPF index is defined as the ratio of the amplitude difference of the PSC induced by the two consecutive electrical pulses (A2−A1) to the PSC of the first spike (A1), and it decreases to zero.[24-25] The whole process emulates the phenomenon of neurotransmitter release enhancement in synapses.

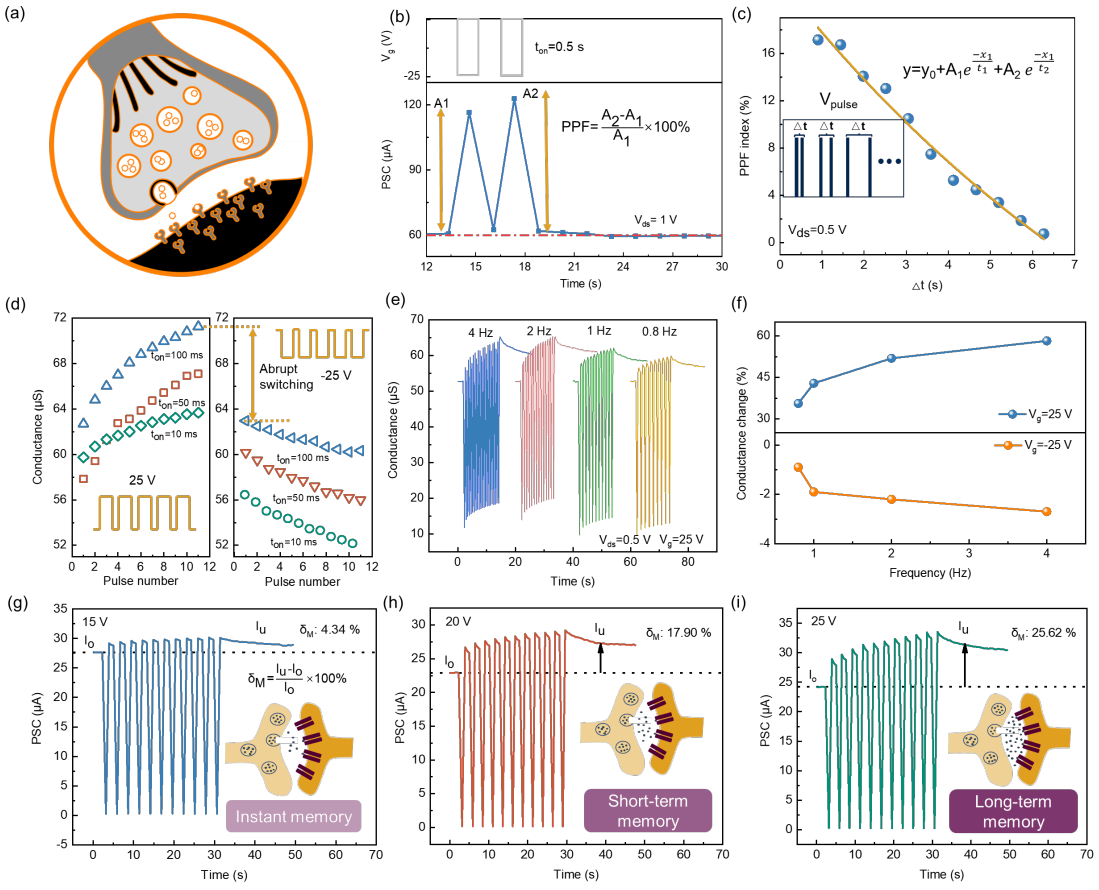

Figure 4. Synaptic behaviors mimicked in P(VDF-TrFE)/BP based artificial synapses and memory consolidation process. (a) Sketch of biologic synapse with signal transmission process. (b) PSC triggered by several consecutive electrical pulses and A is defined as the amplitude of PSC. (c) PPF index as a function of electrical pulse interval time Δt, the fitting curve exhibits that PPF decreases exponentially with the increase of Δt. Inset: Pulse voltage setting with increasing time interval. (d) The conductance weight modulation when P(VDF-TrFE)/BP synapses are subjected to a train of ±25 V voltage pulse under various pulse widths. (e) Spike frequency-dependent responses of channel conductance under 25 V. (f) Conductance gain and reduction under positive and negative pulse voltage plotted as a function of spike frequency. Electrical PSC response of P(VDF-TrFE)/BP synaptic transistors modulated by the different ferroelectric gate

voltages of 15 V (g), 20 V (h), and 25 V (i), respectively. Inset: Schematic diagram of neurotransmitter release amount representing synaptic connection strength under different gate voltages.

Additionally, different programming schemes, including pulse widths, heights, and frequencies are found to have an influence on the synaptic weight update behaviors. Fig. 4(d) displays that the conductance increase when the pulse width is increased from 10 ms to 100 ms. Such phenomenon can also be observed in other gate voltage ranges (Fig. S8). Meanwhile, gate voltage value will effectively modulate the conductance magnitude that increasing pulse height will bring with higher conductance, which is consistent with the synaptic behavior (Fig. S9). It should be mentioned that larger pulse heights can further increase the conductance ratio at the expense of the number of intermedium conductance states.[26] In the NeuroSim online learning, a dummy column can be added to compensate for the limited on/off ratio.[27-28]

Energy consumption for a single pulse event is related with pulse width and height[29] and is estimated to be 41.02 fJ under 1 mV source-drain voltage (Fig. S10). Such ultra-low energy consumption is comparable to human brain synapse (10 fJ). The low energy consumption results from high carrier mobility of BP and effective ferroelectric gate modulation, which could promote signal transmission within synapse.[30-31] In addition, thanks to the small source-drain voltage under ohmic contact, consuming power in the nonvolatile FeFETs can be minimized for each synaptic event. The detailed power consumption with other reported synaptic transistors have been listed in Table S1, which suggests P(VDF-TrFE)/BP advantages for energy-efficient neuromorphic system. Besides, we discuss the programming mode energy consumption, total potential energy from architecture computation, and further energy reduction methods in Supplementary Note 2.

In neurological system, synaptic weight update behaviors can be modulated under different temporal patterns.[32] Figure 4(e) shows the plot of the conductance in response to successive spikes under positive gate voltage with frequency ranging from 0.8 to 4 Hz. Under positive gate pulses, higher stimulus frequency leads to a more prominent potentiation effect whereas the peak values of the resulting conductance decrease with the stimulus frequency increasing under negative voltage (Fig. S11). Above phenomenon strongly illustrate that our P(VDF-TrFE)/BP neuromorphic device can serve as a frequency filter. To further describe the filtering property, the frequency-dependent conductance change percentage is exhibited in Fig. 4(g), the conductance can increase from 35.6 % to 58.2 % and reduce from -0.9 % to -2.7% when the pulse frequency is increased. To realize more practical frequency-dependent behaviors, we have extended the frequency to 16 Hz (Fig. S11). The real-time conductance is sensitive to the external gate voltage pulses. After the gate voltage was turned off, the final conductance value remained stable. The retention time after gate voltage pulse is longer than 3500 s (Fig. S12).

In addition, we simulate the memory strengthening process based on ferroelectric gate voltage tuneability. P(VDF-TrFE)/BP transistors can realize three memorizing modes by PSC change magnitude under different gate biases. Artificial visual system and the three memorizing phases are exhibited in Fig. S13. In order to reflect the change of PSC and the degree of information storage, we define and calculate the memory parameter δ_M. From Fig. 4(g-i), δ_M can be effectively adjusted by the ferroelectric gate voltage. δ_M is 4.34% (instant memory), 17.90 % (short-term memory), and 25.62% (long-term memory) under the gate voltages of 15 V, 20 V, and 25 V, respectively. The increased gate voltages will

contribute to the switching of ferroelectric polarization and generate enhanced PSC change magnitude. Such results are similar to the biological memory consolidation process, represented by the amount of neurotransmitter release.[33] Memory consolidation process under negative ferroelectric gate voltage is shown in Fig. S14 and Table S3.

In order to demonstrate detailed LTP and LTD synaptic behaviors, 40 successive ±25 V gate pulses are applied to the gate electrode (Fig. 5(a)). The real-time conductance change of potentiation and depression under different gate voltage is displayed in Fig. S15. Fig. 5(b) demonstrates the cycle-to-cycle variation by applying 400 consecutive pulses and shows little difference between each cycle. The nonlinearity parameter, asymmetric factor, and cycle variation are essential metrics for synaptic devices, which directly impact the accuracy for neuromorphic computing. Table S4 lists the obtained quantities based on analog weight update and detailed fitting equations and normalize results (Fig. S16) are provided in Supplementary Note 3. Those nonideal factors results of demonstrated P(VDF-TrFE)/BP are at the same levels with previous reported ferroelectric synapses based on graphene or WSe_2.[34]

Such device system has successfully simulated different synaptic behaviors based on multilevel conductance states and laid foundation for further neuromorphic computation. Therefore, to perform pattern recognition application, a multilayer perceptron artificial neural network (ANN) is integrated. For the simulation section on the CrossSim platform, we used an 8×8 pixel image version of handwritten digits, 28×28 pixel version of Modified National Institute of Standards and Technology (MNIST) handwritten digits dataset, and Sandia file classification dataset.[35] The number of dataset used in the backpropagation training simulations are summarized in Table S5. Schematic diagram used for the input pattern recognition process consists of a three-layer network (Fig.5(c)). In the system, the 784 neurons in the input layer correspond to the 28×28 (pixels) of the MNIST image, and the 10 output neurons correspond to 10 classes of digits (from 0 to 9).[36] The multilayer perception system is an interconnected network. A detailed circuit diagram of a synapse layer like a crossbar structure consisting of M×N P(VDF-TrFE)/BP transistors is shown in Fig. S17.

The classification accuracy during 40 epochs of ideal synapse for the three classification datasets are shown in Fig. 5(d-f). In the first few epochs, the recognition accuracy enhances dramatically and reaches saturation value of more than 90%, which approaches the neuromorphic algorithm limit. Note that the training outcomes of high accuracies between 90% and 94% are comparable to other state-of-the-art nonvolatile memories[37-38], and they can be further improved by various voltage pulse schemes. Therefore, ANN simulation at the system level indicates outstanding performance in pattern recognition.

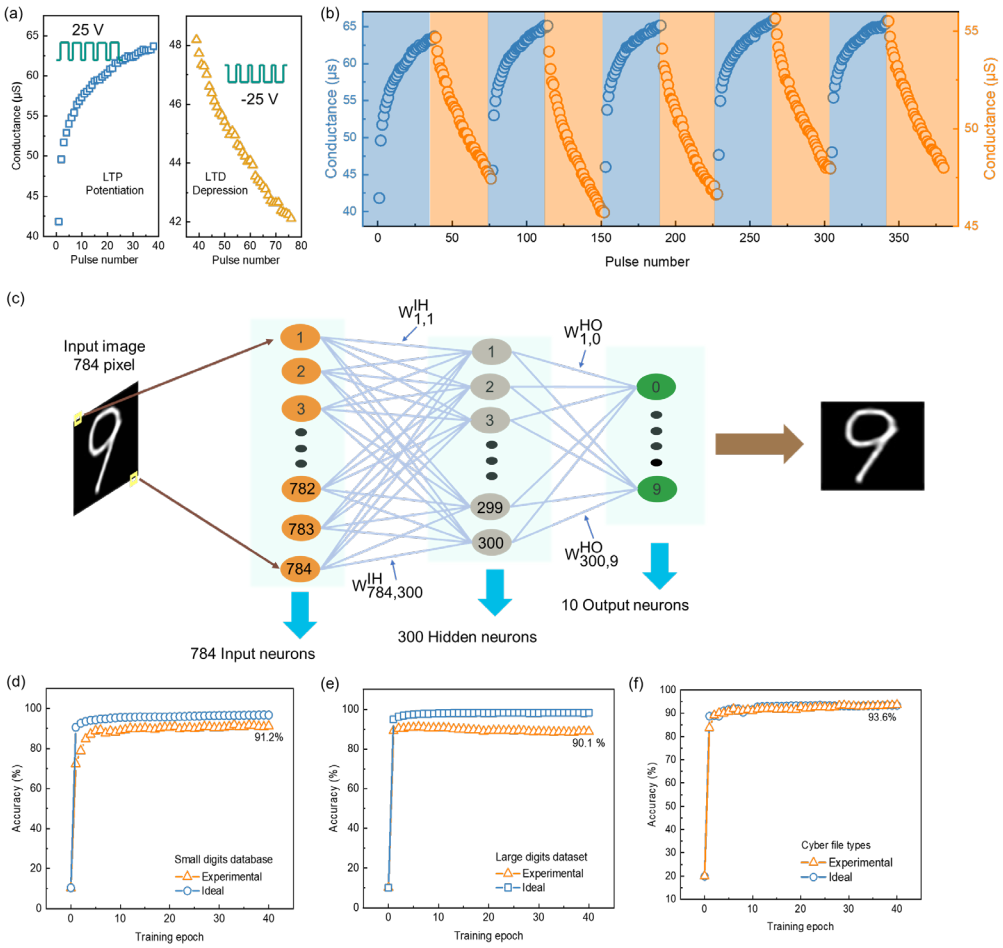

Figure 5. Long-term synaptic characteristics of P(VDF-TrFE)/BP synaptic transistors and pattern recognition with multilayer perception neural network. (a) LTP and LTD operations under 25 V and −25 V (100 ms on time) with 40 pulses, respectively. (b) Cycle-to-cycle variation of P(VDF-TrFE)/BP based artificial synapses under 400 pulses stimulations. (c) Schematic illustration of a three-layer (one hidden layer) neural network for recognition tasks. The simulated pattern recognition accuracy of small digits database (d), large digits database (e), and file types (f) of P(VDF-TrFE)/BP synaptic transistors compared with the ideal cases.

Through the combination of BP and P(VDF-TrFE), P(VDF-TrFE) offers a non-volatile electric field on the BP layer, leading to the fixation of partial carriers under two polarization directions and achieving the modulation of channel conductance.[37, 39] After analyzing and comparing performance and simulation results of P(VDF-TrFE)/BP synapses with other previous reports (Table 1), we can conclude that the high mobility of the 2D BP channel can contribute to signal transmission within synapse and accordingly reducing power consumption, whereas the large conductance variation is favorable for weight update and high accuracy for in-memory computing.

Table 1. Comparison of the features between P(VDF-TrFE)-based 2D FeFETs and the device of this work

Channel Materials	Device structure	Mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	On/off ratio	Synaptic behaviors	Simulation accuracy	Ref.
MoS_2	Top gate	86.5	~10^6	-	-	[40]
$MoSe_2$/PS brush	Top gate	20.2	10^4	-	-	[41]
InGaAs nanowires	Top gate	-	-	STP LTPPPT	>80%	[30]
MoS_2 and $MoTe_2$	Dual gate	-	10^3-10^4	LTP LTD	88%	[42]
BP/MoS_2	Top gate	1159	10^3	-	-	[43]
$MoTe_2$	Back gate	40-80	-	-	-	[44]
BP	Top gate	~500 (12 nm BP) ~900 (8 nm BP)	10^3	LTP LTD PPF	93.6%	**This work**

In conclusion, taking advantages of the emerging concept of 2D FeFETs, we have developed P(VDF-TrFE)/BP ferroelectric synapse based on ferroelectric gate tunability and a high degree of functionality for synaptic behavior operations. The presented FeFETs can perform a large on/off ratio and high mobility under small bias voltage, with very low femtojoule level (~40 fJ) of energy consumption. Based on synaptic weight updates, a series of synaptic plasticity and biological memory consolidation process can be emulated. The neural network simulation shows a high recognition accuracy of ~93.6% for handwritten digits. The proof-of-concept device opens up a way for implementing energy-saving and highly integrated artificial neural system.

Supporting Information

Device fabrication methods, PFM and AFM characterization for ferroelectric films, electrical properties and synaptic behaviors of transistors, conductance change under external gate voltage modulation, consumed energy of the synaptic device, estimation of nonideal factors, and the real-time potentiation and depression processes.

Acknowledgments:

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