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The effect of pre-existing voids on solder reliability at different thermomechanical stress Levels: Experimental assessment

Abbas Waseem [a,*], Mesfin Seid Ibrahim [a,c], Chang Lu [a], Muhammed Waseem [a,b], Hiu Hung Lee [a,*], K.H. Loo [a,b,*]

[a] Centre for Advances in Reliability and Safety, New Territories, Hong Kong
[b] The Hong Kong Polytechnic University, Hung Hom, Hong Kong
[c] Kombolcha Institute of Technology, Wollo University, Kombolcha 208, Ethiopia

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ABSTRACT

After lead-free technology, pre-existing voids in Power-MOSFET device solder connections have been a hot topic. Previous studies have examined the mechanical performance of solders with manufacturing-induced voids typically by generating excessive voids intentionally using simulation analysis without/insufficient experimental results. Electronic assembly standards such as IEC 61191-2, J-STD-001G, and IPC-A-610G do not cover voiding due to conflicting opinions and insufficient experimental evidence. In this context, comprehensive experimental results are needed to verify simulation results and assist in setting the standard. Silicon-based Power MOSFET packages with different locations, sizes, and patterns of pre-existing voids with nearly the same percentage of voids (30–33%) have been chosen to address this critical issue. The Power MOSFET test samples underwent power cycling-based accelerated degradation testing at various stress levels and monitored the location and rate of solder degradation at specific time intervals. It is found that small dispersive voids in solder life are useful, but clusters can accelerate damage propagation. Contrary, large dispersive voids at the edges initiate solder damage, reducing solder life. Our experimental investigation findings indicate that pre-existing voids' positions, sizes, and patterns should be considered when establishing solder void inspection standards. This would improve power devices' reliability for end-user power supply and control.

1. Introduction

Metal oxide semiconductor field effect transistors (MOSFETs) are power electronic semiconductor switches that are widely utilized in industrial applications such as power inverters, electrical control, and power supply systems. The single MOSFET has a convoluted design that contains many components, such as a copper baseplate, gate, solder/die-attach, die, and wire bonds [1]. The method of soldering is used to assemble these separate components into one complete package [2]. The thermomechanical stresses caused by nonconformity between the coefficients of thermal expansion (CTE) in the components result in multiple modes of failure in this assembly [3]. Power cycling in electronic systems is the primary cause of power semiconductor ageing and can affect wire bonds, Cu-baseplate, die, or solder interconnections. Literature suggests that mechanical deterioration of power electronic devices occurs more frequently at solder junctions [4,5]. It is well known that thermal expansion creates a shear strain between the die, solder, and substrate during power cycling, which is expressed as;

$$\Delta\varepsilon = \frac{(\tau_{Up}.\Delta T - \tau_{Lo}.\Delta T)L}{2t} \quad (1)$$

where $\Delta\varepsilon$, L, t, τ_{up}, τ_{Lo} and ΔT are strain magnitude, largest dimension's length, solder thickness, CTE of upper and lower material, and temperature undergone by the bond, respectively. Accordingly, the damage would propagate from the boundaries of the solder (regions of high-strain) into the waist. However, this is only true when the solder has no voids. Typically, there are always manufacturing process-induced voids in the solder-joint fabricated with solder-paste [6–8]. Several factors impact the formation of these voids in solder; however, the reflow process is the primary cause of this formation [9]. Briefly, soldering involves heating a paste of solder to its melting point, at which point all the volatile chemicals in the paste will have evaporated. Evaporation occurs throughout the paste's volume, not simply on its top

* Corresponding authors at: Centre for Advances in Reliability and Safety, The Hong Kong Polytechnic University, Hong Kong.
E-mail addresses: waseem.abbas@cairs.hk (A. Waseem), rainbow.lee@cairs.hk (H.H. Lee), kh.loo@polyu.edu.hk (K.H. Loo).

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surface. There is a tendency for gaseous components to escape the molten solder alloy, but some of them are unable to escape and become stuck within, creating voids.

Voids are categorized into numerous types [10] pinhole, shrinkage, kirkendall, and microvia voids exist alongside macrovoids and microvoids. However, the most generally reported types of processing-induced (pre-existing) voids are small/micro and large/macrovoids [9]. These voids have received much attention since they are the only ones readily visible using common X-ray imaging techniques [11]. The diameter of a typical large/macrovoid is between 100 μm and 300 μm [9]. According to Subbarayan [12] and D. Busek [9], voids with diameters<50 μm are classified as small/microvoids. Since voids with diameters between 50 μm and 100 μm are sometimes called small/microvoids and sometimes large/macrovoids, there is no unambiguous size distinction between large/macro and small/microvoids. In this study, we set the size limits for microvoids and macrovoids < 50 μm and < 150 μm respectively, referred to as small and large voids throughout the article. Notably, if we consider the voids are nearly circular and embedded in the middle of the solder layer, the average diameter would be less than or equal to 40 μm because the solder layer has a thickness of 40 μm. However, process-induced voids could be of different sizes and shapes, as shown in Fig. 4S (supplementary info). They have maximum heights of $\sim$ 40 μm and widths more or less than $\sim$ 40 μm. Since we proposed voids, inspection using non-destructive 2D X-ray imaging, images could be captured from the top–bottom or bottom-top of a MOSFET, with the width of the voids being the average diameter.

The influence of process-induced pre-existing voids on the thermo-mechanical performance of solder has been the subject of a number of studies. Until recently, many prior pieces of research have focused on the voids effects on the durability of solder layers within an electronic package, utilizing finite element method (FEM) modeling with no/insufficient experimental results to prove their arguments [13–15]. Since the simulation helps to comprehend the stresses based on geometry and materials and to calculate a typical damage value [16]. However, the solder voids arrangement is oversimplified in design and not reflective of reality; real comprehensive experimental examples of degradation are rare. Expensive equipment and time-consuming experiments also drive the researchers to work on simulation using software such as COMSOL, ANSYS, and ABAQUS. However, this behaviour led to confusion when setting standards for solder void inspection. For instance, Shibutani et al. [17] demonstrated that when the size of the void is small, it imposes minimal impacts on the failure life; however, the influence of multiple small voids arrayed on a fracture is stronger than that of a large void. Otiaba et al. [13] demonstrated that $\geq$ 30% of small voids stop the spread of the fracture and prevent degradation while larger voids at the high-stress sites are detrimental to the life of a solder. In contrast, Surendar et al. [14] demonstrated that small voids arrest strain and produce a zone of high-strain density, whereas larger voids are less damaging. Following Surendar's research, Jiang et al. [15] established that the more distributed the small voids, the poorer the mechanical characteristics of the solder. Yunus et al. [18] conclude that large voids, regardless of their location, severely reduce joint life, while small voids on the component side aid fracture growth. According to the opinions of soldering companies [19,20], small and uniformly dispersed large voids are a necessary and essential component of the joint. Unresolved is the question of whether and how voids affect the reliability of solder junctions. Voids may serve as stress relievers and crack arrestors, but they can also be stress raisers. As a result of these polarizing points of view and the lack of definitive proof, voiding has not been covered by current standards for the demands and acceptance of electronic-assemblies, including IEC 61191-2 [21], J-STD-001G [22], and IPC-A-610G [23].

To address this critical problem, this study's primary objectives are to experimentally assess degradation and failure analysis for Silicon power MOSFET packages with various locations, sizes, and patterns of pre-existing voids in their solders with almost the same levels of voids percentage. Before power cycling, the voids inspection is carried out with Scanning Electron Microscopy (SEM) and X-ray diagnostic equipment. A power cycling-based accelerated ageing test is conducted to capture scanning accosting microscopy (SAM) images after fixed intervals of cycles to examine the position, types, location, and degradation rate. In addition, structure–function analysis is performed to detect and precisely validate failure locations based on the internal structure or physical features of power MOSFET layers. The power cycling approach is selected because it mimics real operating conditions better than thermal cycling to detect device failure modes and mechanisms. The results suggest that solder voids inspection standards should consider pre-existing voids positions, sizes, and patterns. From a production standpoint, solder joints should have small, fairly dispersive voids.

2. Methodology

This section discusses the experimental design and setup to collect data for the investigation of the impact of sizes, locations, and patterns of pre-existing voids in the solders of power MOSFETs on the life of test samples.

2.1. Description of test samples

This study used a commercial Silicon MSOFET with a 600 V power rating and 49A maximum current capacity at $T_c = 100$ °C. The packaging is TO-247, intended for high-voltage applications with a super junction with a rapid switching frequency and low switching and conduction losses. Fig. 1 depicts the pictorial and schematic of the internal layers of the Si-MOSFET power device. Primarily it is made of four layers, including Lead-frame (Copper), Solder/Die-attach (Compounds of Antimony, Silver, and Tin), Die (Silicon), and Encapsulations (mixture of Epoxy-resin, Carbon-black and Silicon-dioxide). Typically, manufacturing process-induced voids with varying positions, sizes, and patterns exist in the solder layer (Fig. 1) and will be the focus of this article.

2.2. Description of experimental setup

A power cycling-based accelerated degradation test on Si-based power MOSFETs was performed in this study to assess the lifetime of Si-based power devices at the component level by investigating the impact of long-term thermal and electrical stresses on solder degradation, which had pre-existing voids of varying locations, sizes, and patterns. The voids percentage was calculated before power cycling utilizing Yvlon Cougar X-ray diagnostic equipment. T3ster Master Software with a resolution of 20 points/decade and 1000 Bayes iteration number was used to determine the structure–function (STF) of the test samples before power cycling and after completing 72,000 cycles. The scanning acoustic microscopy (SAM) system (Model; KSI WINSAM Vario III) with a 15 MHz transducer is employed to examine the defects and their locations and types in the samples under test. Subsequently, SAM measurements were performed regularly once 7200 cycles had been completed. Destructive methods, such as decapsulation, microsection polishing, and SEM/optical analysis, are also used to understand the internal structure of the MOSFETs.

Nine Si-based MOSFET samples from the same batch were chosen for this experiment, and three groups with various junction temperature swing (ΔT_j) scenarios were created. Each scenario of degradation testing consisted of three samples, with the first group (samples 1–3) set at ΔT_j of 45 °C, the second group (samples 4–6) at 100 °C, and the third group (samples 7–9) at 110 °C. Minimum junction temperatures ($T_{j\text{-}min}$) and maximum junction temperatures ($T_{j\text{-}max}$) for each case range from 40 °C to 85 °C, 25 °C to 125 °C, and 25 °C to 135 °C, respectively, and the operating principle is schematically described in Fig. 2. Notably, the distribution of small voids in scenario 1 ($\Delta T_j = 45$ °C, sample 1–3), scenario 2 ($\Delta T_j = 100$ °C, sample 6), and scenario 3 ($\Delta T_j = 110$ °C,

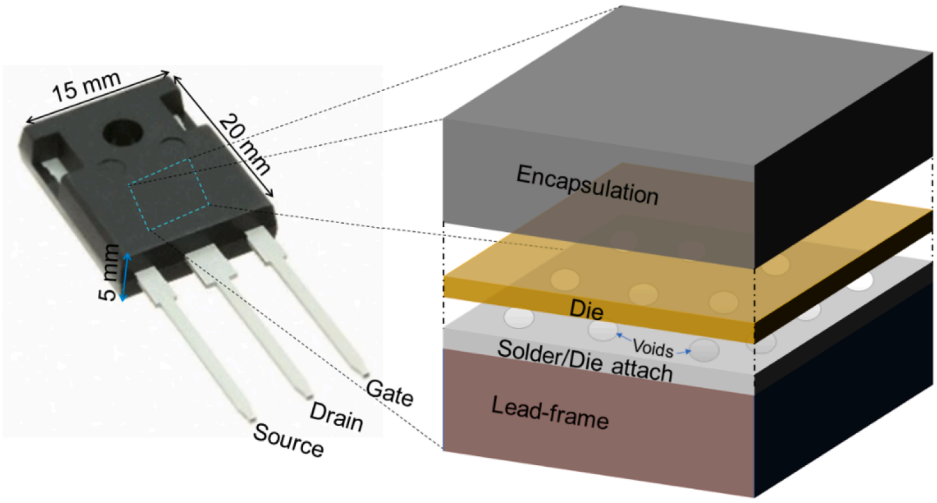

Fig. 1. The test sample, pictorial, and schematic of internal layers.

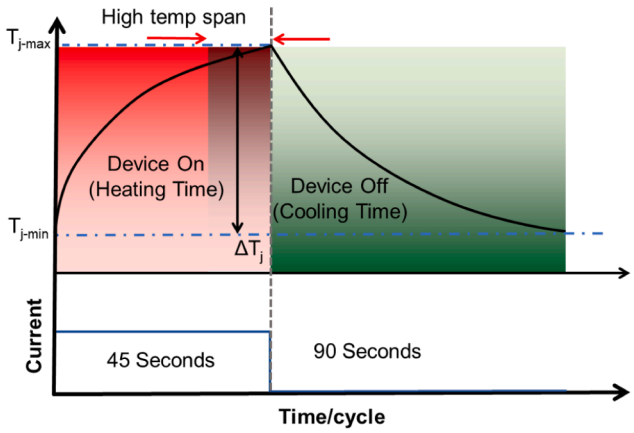

Fig. 2. Operating Principle for the Power Cycling Test.

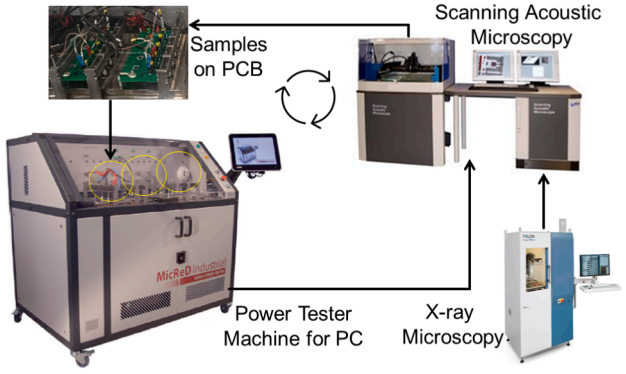

Fig. 3. Experiment design and data collection.

sample 7–9) is kept similar to check the impact of dispersive small voids on the degradation initiation and propagation of solder at different stress levels. Samples 4 and 5 (with clusters of voids) are kept in scenario 2 ($\Delta T_j = 100$ °C) to determine the lifetime of solder with specific patterns of pre-existing voids at moderate junction temperature. This allows us to estimate the lifetime of that particular case at temperatures above and below the set die temperature. Since the lifespan of a device is an exponential function of die temperature, it decreases by two to three times for each 10 °C increase in temperature [24,25].

The experimental design for the various ΔT_j scenarios is based on the diverse operating environments of power MOSFETs. All test samples in each group were aged at a standard ambient temperature of 24 ± 2 °C for about 72,000 cycles. In this work, temperature-sensitive electrical parameters based on the forward-biased voltage parameter of a diode are utilized to monitor a continuous online junction temperature swing throughout a power cycle test. The calibration process is carried out routinely after a specified time interval.

During a single power cycle, the unit was ON for 45 s (during the heating phase) and OFF for 90 s (during the cooling phase), for a total cycle time of 135 s **(**Fig. 2**).** Primarily, the experiment was divided into accelerated ageing utilizing power cycling and SAM analysis (Fig. 3), which lasted until adequate degradation data were collected.

3. Results and discussions

3.1. Internal structure and Process-Induced voids

To understand a MOSFET's internal structure and layers, we decapsulate and cross-section two silicon-based MOSFETs. Accordingly, Fig. 4**(a)** shows the decapsulation of the MOSFET until the Si-die and bonding wires have been exposed. Fig. 4**(b)** shows the cross-sectional image of a Si-MOSFET. It has been revealed that there are five layers named, Encapsulation, Bonding-pad, Si-die, Solder/die-attach, and Lead-frame in a MOSFET with thicknesses of around 1500, 5, 200, 40, and 1000 μm, respectively. Several pre-existing videos have been detected in the solder/die-attach layer with ~ 7–30 μm diameters. Previous studies have shown that forming these voids is unavoidable and the reflow method is the most influential factor in creating these voids [9]. Notably, the destructive method used in this study involves microsection polishing and SEM/optical analysis (Fig. 4**a, b**); with a downside, the observation is limited to one plane. In this regard, an X-ray inspection system is a quick and simple method to inspect the overall voids in a test sample. This technique's most popular diagnostic approach analyses voids from a 2D perspective. However, in this situation, a large macrovoid could conceal smaller voids that may be located beneath or above it. X-ray imaging, despite the fact that it makes it difficult to accurately determine the percentage of voids at minor differences, still offers information about the relative change in the total percentage of voids .

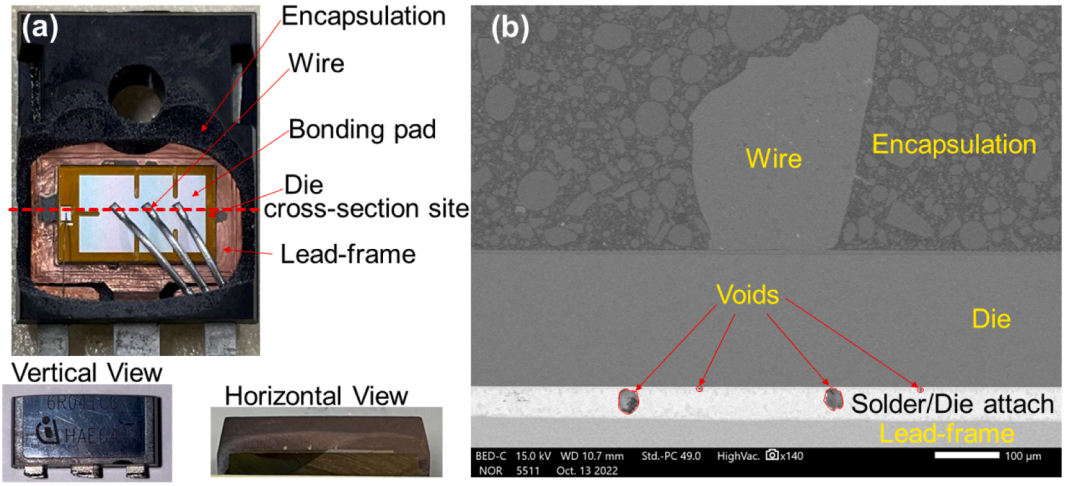

Fig. 4. **(a)** Decapsulation of a new Si-MOSFET (b) SEM cross-sectional image of a new Si-MOSFET.

For this study, nine Si-MOSFET packages with various locations, sizes, and patterns of pre-existing voids with almost the same levels of voids percentage (~30–33%) have been selected by using X-ray inspection (Fig. 5). Notably, even though contrast variation caused by the copper structure beneath the solder joint results in pronounced contrast variation at the samples' bottom edges and upper center [11], we can still easily distinguish the small and large voids at those sites in the images. Due to the potential impact of these contrast changes on automated techniques, we manually calculated the voiding % using ImageJ software. Since the percentage of voids primarily impacts the packages' thermal resistance (Rth) [25]. To confirm our estimation of voids percentage, we also checked the R_{th} of the corresponding samples via STF (**Fig 2S**, supplementary info). We found similar R_{th} values of all the test samples, a crossover to a similar percentage of pre-existing voids.

Fig. 5 shows X-ray images of the packages with die-attach voids. It is depicted that all the samples have multiple small voids with a diameter of ~ 30–35 μm. Notably, the diameters (d) of voids are consistent with those measured from the SEM cross-sectional image of the new MOSFET (Fig. 4**b**) and are called micro/small voids in the literature [9,12]. It is shown that multiple small voids with similar sizes are distributed in the die-attach layers of all samples. However, the void's locations, sizes and patterns make some samples distinct from the rest. For instance, sample 4 has highly concentrated voids (i.e., cluster area of ~ 3370 μm^2 with ~ 55% voids) distributed at the bottom right corner and edges of that sample, while at the center (indicated inside the yellow line), the distribution is most likely uniform.

Similarly, sample 5 has clusters of voids (area ~ 1150 μm^2) at the bottom right corner and the edges but is relatively less condensed (~50 % voids) and smaller than sample 4. A very small number of larger voids (d = ~130 μm) have also been noticed at the center and bottom edges of samples 9 and 6. Based on these observations, the samples can be divided into three groups: those with a large and dense cluster of small voids (sample 4) and those with relatively small clusters with less

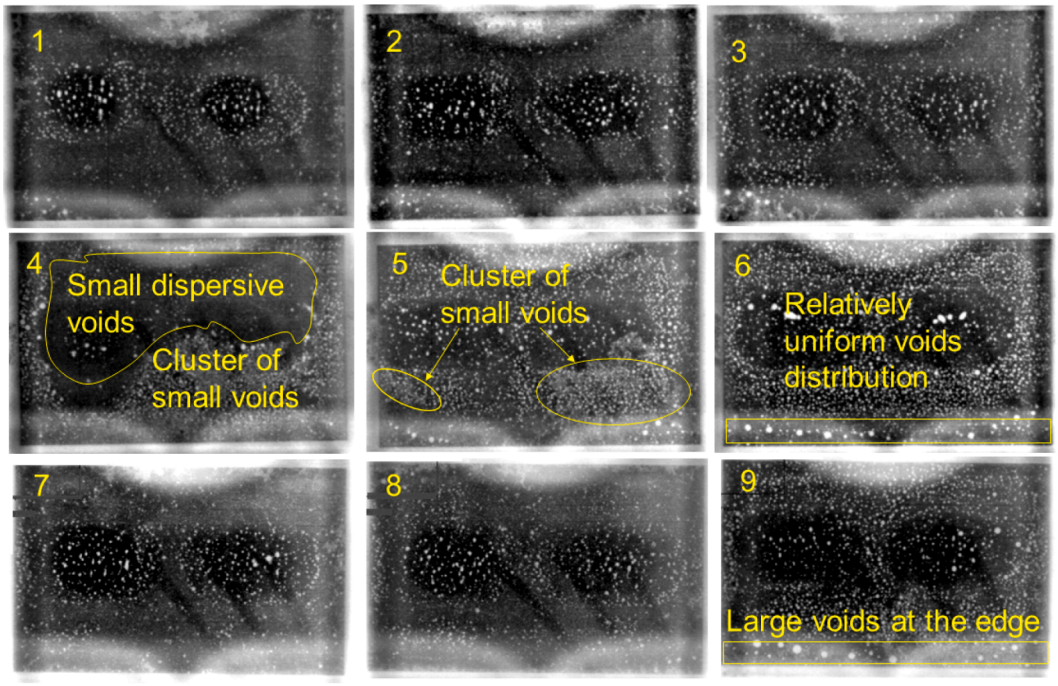

Fig. 5. X-ray images of samples 1–9 chosen as test samples.

density of voids (sample 5). Samples 9 and 6 have a small number of larger dispersive voids at the bottom edges and the centers. In contrast, the remaining samples have a relatively uniform distribution of multiple small voids.

These nine samples are divided into three scenarios based on the thermomechanical stress level applied during power cycling. Scenario 1: samples 1–3, with the least temperature swing (ΔT_j) 45 °C. Scenario 2: samples 4–6 with a moderate ΔT_j of 100 °C. Scenario 3: samples 7–9 with a high ΔT_j of 110 °C. Detecting cracks and their locations through X-ray imaging is problematic and sometimes impossible. In this regard, for the evolution of the degradation process after repeated and fixed numbers of power cycles (7200 cycles in our case), the nondestructive analysis technique, scanning acoustic microscopy (SAM), is used.

Notably, SAM is an acknowledged method for nondestructive assessment and verification of microelectronic components and materials. It has two detection modes: transmission mode (T-SAM) and reflection mode (C-SAM). T-SAM detects defects and their positions, while C-SAM estimates the types of defects in a specific layer. To confirm the ability of SAM, we compared the C-SAM image with the decapsulated sample. It is depicted in Fig. 3S **(**supplementary info) that the SAM has the appropriate capability to see the footprints of degradation on the die during power cycling without decapsulation.

3.2. Impact of different stress levels on voided solders

The SAM evaluation of test samples 1–3 for the first power cycling scenario with the least temperature swing of 45 °C is shown in Fig. 6**.** As the ageing stress is minimal, the change in degradation is very slow, or it is the least compared with the subsequent two cases. Due to this, test samples stayed as intact as they were at their pristine stage even after 72,000 cycles.

The T-SAM outcomes of scenario 2 ($\Delta T_j = 100$ °C, samples 4–6) are presented in Fig. 7**(a).** The images are captured routinely at an interval of 7200 cycles. Nevertheless, test samples remain undamaged for longer and do not undergo changes; hence, images are presented after 14,400 cycles. The SAM of test samples 4–6 in their pristine states (0-cycle) is shown on the top and is used as a standard for ageing test samples. It is found that the edges of the test samples 4–6 and the corner of sample 4 convert into semi-black after 14,400 cycles, indicating the growth of defects from the edges of all samples and the corner of sample 4. The semi-black portion of sample 4 converts into fully black after 28,800 cycles and keeps increasing with the increasing cycle numbers until 57,600 cycles, then stops and keeps stopping up to 72,000 cycles. Similar behavior in sample 5 is observed, but after 21,600 cycles, the bottom right corner converts into semi-black and entirely black after 57,600 cycles. To estimate the location of defects in the corresponding samples, STF (integral and differential) of the test samples 4–6 is taken prior to power cycling and after every 72,000 cycles, as shown in Fig. 7 **(b, c).** Notably, the STF is a sophisticated thermal analysis tool that may be used to easily and precisely detect failure locations based on the internal structure or physical properties of power MOSFET layers [26,27]. These functions have been generated for samples 4–6 using T3ster Master Software with a resolution of 20 points/decade, 1000 Bayes iteration numbers, and without parallel R_{th} correction. Individual package layers are easily recognizable; the first area in $C_{th}(R_{th})$ denotes the silicon chip/die, followed by the die-attach/solder, lead-frame, thermal-pad, fixture, and sink. Please note that the differential STF is equal to the square of the heat conducting path's cross-sectional area, as follows: [26,27]

$$K = \frac{dC_{th}}{dR_{th}} = \lambda c A^2 \tag{2}$$

where λ is the thermal conductivity and c is the volumetric heat capacitance and can be used to easily detect defects' location (i.e., which layer). It is worth noting that the curves first overlap (i.e., at 0 cycles), which manifests an intact structure of the test samples with similar R_{th} values (Fig. 7**b**). The measured values reveal considerable variations in the corresponding curves after 72,000 cycles (Fig. 7**c**). The place where curve separation began indicates the region of deterioration [26,27]. In the plots depicted in Fig. 7**(c),** degradation is observed mainly at the die-attach layer of the power MOSFETs. Similarly, thermal capacitance, C_{th} (Y-axis, Fig. 7**b, c**) is a material property that is described as follows:

$$C_{th} = c_p M = V \rho c_p \tag{3}$$

where V, ρ, M, and c_p are the volume, density, mass, and specific heat of the materials. It is depicted in Fig. 7**(b,** 0-cycles**)** that C_{th} is the same for samples 4–5 and reflects a similar percentage of pre-existing voids for the corresponding test samples. After 72,000 cycles (Fig. 7**C**), the intensities of the peaks (C_{th} values) related to die-attach decrease with the sequence of $C_{th\text{-}Sample\ 4} < C_{th\text{-}Sample\ 5} < C_{th\text{-}Sample\ 6}$. This demonstrates that sample 4 has the most significant solder deterioration, while sample 6 has the least, which is further verified with the C-SAM in the following Figure.

Fig. 8**(a)** shows the C-SAM of test samples 4–6 (scenario 2). Clues of popcorn fractures (outside of the die area) are noticeable in all samples and are likely due to the release of trapped moisture at a significantly high junction temperature (i.e., 100 °C) [28]. Delamination close to edges and bottom-right corners initiates in Sample 4 and gradually increases until 32,400 cycles, then increases rapidly, slows down again and finally stops (Fig. 8**b**). Evidence of delamination close to the edges is also observable in sample 5. Sample 5 shows the same trend as Sample 4 but with a significantly late initiation interval and a slower degradation rate. Using ImageJ software, we measured the delaminated area with the number of cycles to estimate the quantity of the degradation. Fig. 8**(b)** shows that delamination from the edges and bottom-right corner in Sample 4 is gradually increasing with the ratio of ~ 0.05 cm^2/7200-cycles until 28,800 cycles, then increasing rapidly (0.08 cm^2/7200 cycles) and slowing down again, indicating void growth that continues but at a less aggressive rate and finally stopping after 57,600 cycles.

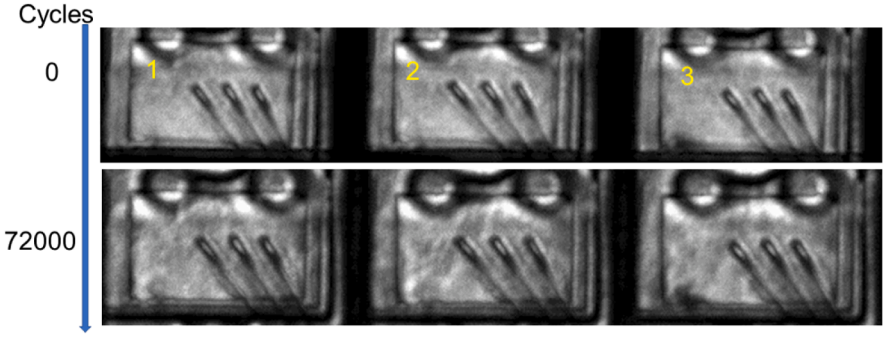

Fig. 6. T-SAM of scenario 1 (samples 1–3), degrading at $\Delta T_j = 45$ °C.

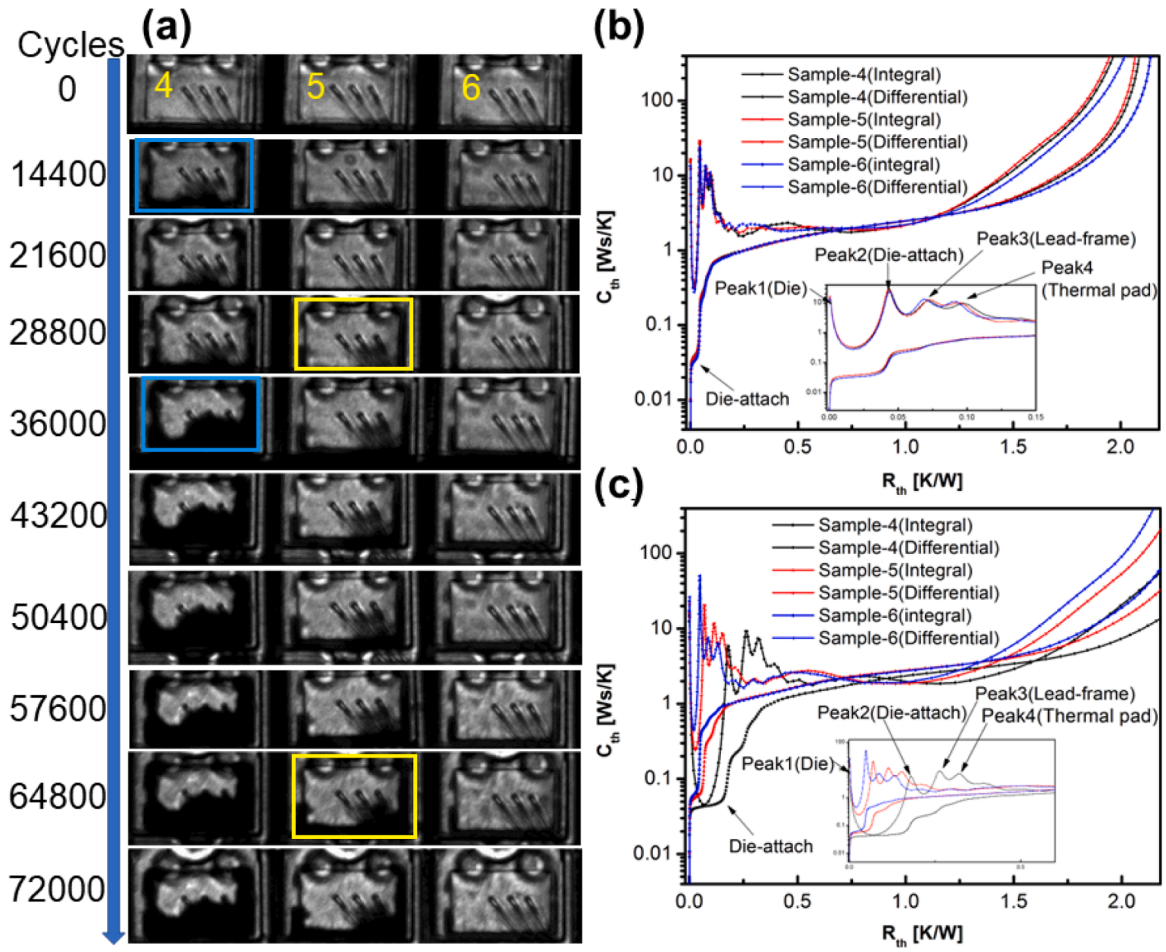

Fig. 7. Scenario 2 ($\Delta T_j = 100$ °C, samples 4–6) **(a)** T-SAM, 0–72000 cycles (b) structure–function, before starting power cycling (c) structure–function after 72,000 cycles. Insets depict the zoomed part of the structure–function curves.

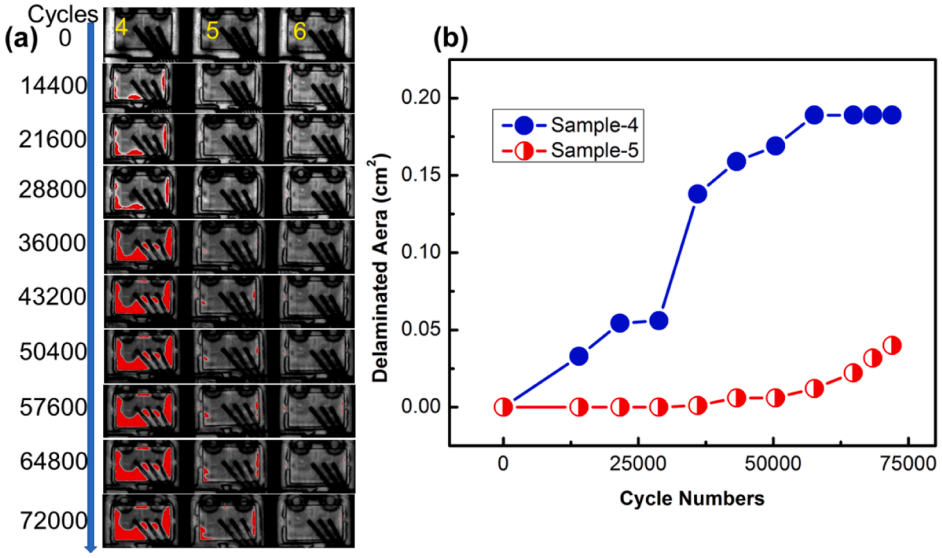

Fig. 8. Scenario 2 ($\Delta T_j = 100$ °C, samples 4–6) **(a)** C-SAM, 0–72000 cycles (b) delaminated areas with the passing of 72,000 cycles.

Interestingly, sample 5 also has dominant die-attach degradation but with a relatively late initiation interval and a slower degradation rate (Fig. 8**b).** Please note that the die-attach degradation of samples 4 and 5 from the bottom right corner is not very clear in C-SAM (top–bottom) but is evident in T-SAM. Most probably, the reflected sound waves were distracted by the bonding wires at those corners and the information about that signal's loss. In this regard, by capturing the C-SAM from the bottom top, the delimitation at the corners of both samples becomes

obvious, as shown in Fig. 3SS (supplementary info). In summary, the images captured through T-SAM show the position of the defect's growth in test samples 4–6. The STF of samples indicates that these defects are formed at the die-attach layer of the MOSFETs. The images from C-SAM (Fig. 8**a**) confirmed that the die-attached degradation appeared in the form of delimitation. The solder with large clusters (area ~ 3370 μm^2) of concentrated small voids (~55%) initiates the damage sooner and degrades it faster (i.e., sample 4). Contrary to this, smaller clusters (area ~ 1150 μm^2) with less concentrated small voids (~50%) have a later initiation interval and a slower degradation rate (i.e., sample 5). Interestingly, there are no signs of damage initiation in the solder of the sample with relatively dispersed small voids (i.e., sample 6) (detailed in the next section).

Similarly, the SAM inspection for scenario 3, where the junction temperature swing is 110 °C and shown in Fig. 9**(a, b).** These results are shown at intervals of 0 cycles and completing 72,000 cycles. The T-SAM and C-SAM indicate only popcorn fractures outside the die area in all samples and a small delimitation at the edges of samples 7 and 9. Noteworthy, T-SAM indicated that after 72,000 cycles the connections of the bond wires converted to black in the samples of the corresponding scenario, which are clues of bond wire degradation.

To see the impact of the locations, sizes, and patterns of the pre-existing voids on the solder life, we mask the x-ray images from Fig. 5 (captured in the pristine state) with the T-SAM images captured after the 72,000 cycles (processed with software to remove the degraded area) and show them in Fig. 10. Scenario 1 (ΔT_j = 45 °C, samples 1–3): there are no clues about the detrimental effect of small voids on the life performance of solder when they are fairly dispersive. Scenario 2 (ΔT_j = 100 °C, samples 4–6); clusters of small voids along the high-strain and path of fracture propagation (samples 4 and 5) impact the solder life negatively. They initiate and accelerate the damage propagation, and the time of initiation and rate of propagation depends upon the area of clusters and the frequency of the voids in the clusters. The damage initiation is faster, and the degradation rate is high for large clusters with a high frequency of voids (i.e., sample 4) and vice versa (i.e., sample 5). The mechanism can be understood as follow; Multiple variables, including strain, stress, and cumulative plastic work, contribute to the initiation and propagation of damage. Strain energy is a form of potential energy stored inside a body due to the work done on the body by external stresses. With each successive power cycle, strain energy builds up in the solder/die-attach layer. Solder damage will likely initiate when the accumulated total strain energy hits a certain threshold. It is well known that the amount of strain energy increases as the void percentage increases. This behavior can be described in physical characteristics such as the load-carrying area and the stress concentration factor. Such as, a decrease in the load-bearing area as the proportion of void increases. This adds to the deleterious effect of overall compliance and stress concentration effects. In our particular instance, the percentage of voids has reached as high as 55% in the clustering zones, which indicates that the collected strain energy has the potential to reach a critical threshold more quickly, making it easier for damage to start and spread. These results and interpretations are consistent with the simulation analysis results done by Otiaba et al. [13], which demonstrates that the maximal strain energy increases abruptly when the percentage of clustered small voids increases from 30%.

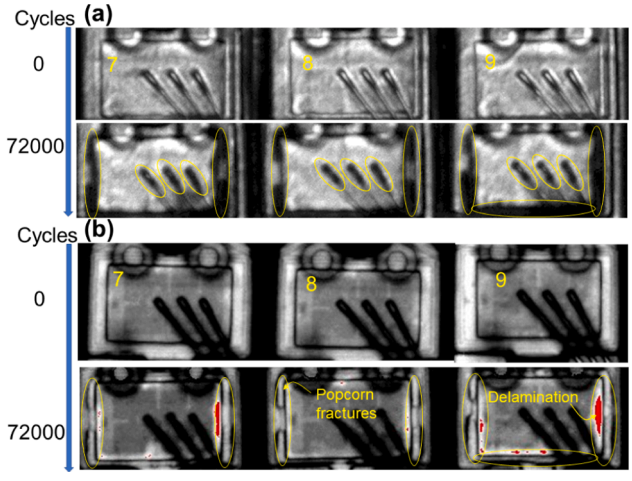

Fig. 9. Scenario 3 (ΔT_j = 110 °C, samples 7–9) **(a)** T-SAM (b) C-SAM.

When small voids are fairly dispersed, they have no apparent negative impact on the lifespan of solder (i.e., sample 6). If the voids are large (d < 150 μm) along the edges, which is considered high-strain and a damage propagation path [13,15] could cause the initiation of the die-attach degradation (i.e., samples 6 and 9). This could be understood as large voids are likely through voids (Fig. 4S a, b, supplementary info). Through voids are 40 μm deep in a solder layer of 40 μm thickness and located at the edges (high strain and crack propagation path) of samples 9 and 6 solder joints. It is well known that when the void grew so enormous that it became truncated to the lead frame, it caused an increase in the stress concentration and stiffness of the joint. Since there is a rise in the stress concentration at the interfaces whenever the void interacts with the silicon die or the copper heat spreader, and verified [13] to be most detrimental when found at the edges of a solder joint; hence, the solder with large voids cannot withstand high stress and crack propagation path at the site and initiate the damage. However, the presence of such voids at the center of die-attach (i.e., sample 6) has no negative impact on the life of the solder due to the lowest stress at that site per equation (1). Scenario 3 (ΔT_j = 110 °C, samples 7–9); no detrimental effect is seen by the fairly dispersed small voids on the degradation of solder life, even if the stress level is high.

Notably, it is found that when the damage propagation reaches the site of fairly dispersive small voids (sample 4), even at the edges (samples 9 and 6), where strain is supposed to be high, the damage propagation stops (Fig. 8**a, b**). This seems to show that small voids stop the damage from spreading. One possible explanation for this damage arrest mechanism is that the small void acts as a blunting agent, reducing the sharpness of the damaged region's tip [13,29,30]. For instance, if we consider the solder as an elastic material. In Linear Elastic-Fracture Mechanics, it is well known that the J-integral/fracture-driving force is a path-independent line integral that quantifies the singular stresses and strains close to a fracture tip. The following expression [29] demonstrates the two-dimensional form of J. The fracture is assumed to reside in the global Cartesian X-Y plane, with X parallel to the fracture.

$$J = \int_{\gamma} W d_y - \int_{\gamma} \left(t_x \frac{\partial u_x}{d_x} + t_y \frac{\partial u_y}{d_y} \right) ds \tag{4}$$

In this equation, γ, W, t_x, t_y, u, and s represent any path surrounding the fracture tip, strain energy density, traction along the x-axis, traction along the y-axis, stress component, displacement, and distance along the path, respectively. Accordingly, if the fracture-driving force (J-integral) value decreases, there will be less chance of initiation or propagation of fracture. In our case, the small voids are nearly circular and embedded in the solder layer (Fig. 4b). The stress concentration factor, which represents the ratio of the highest stress to the nominal far-field stress, is typically 3 or lower for small circular voids [31]. Consequently, in the majority of instances, the stresses exerted on the opposite side (180°away) from the fracture are insufficient to initiate a new fracture.

Interestingly, our experimental results and interpretations align closely with the FE simulation study by Lau et al. [29] It has been observed that the J-integral, which represents the driving force around the crack tip, is considerably reduced in the presence of small voids with diameters of approximately 25 μm and 35 μm, compared to situations where voids are absent or larger in sizes. This implies that the solder joint containing smaller voids in front of the fracture exhibits a reduced likelihood of fracturing compared to joints lacking voids or containing

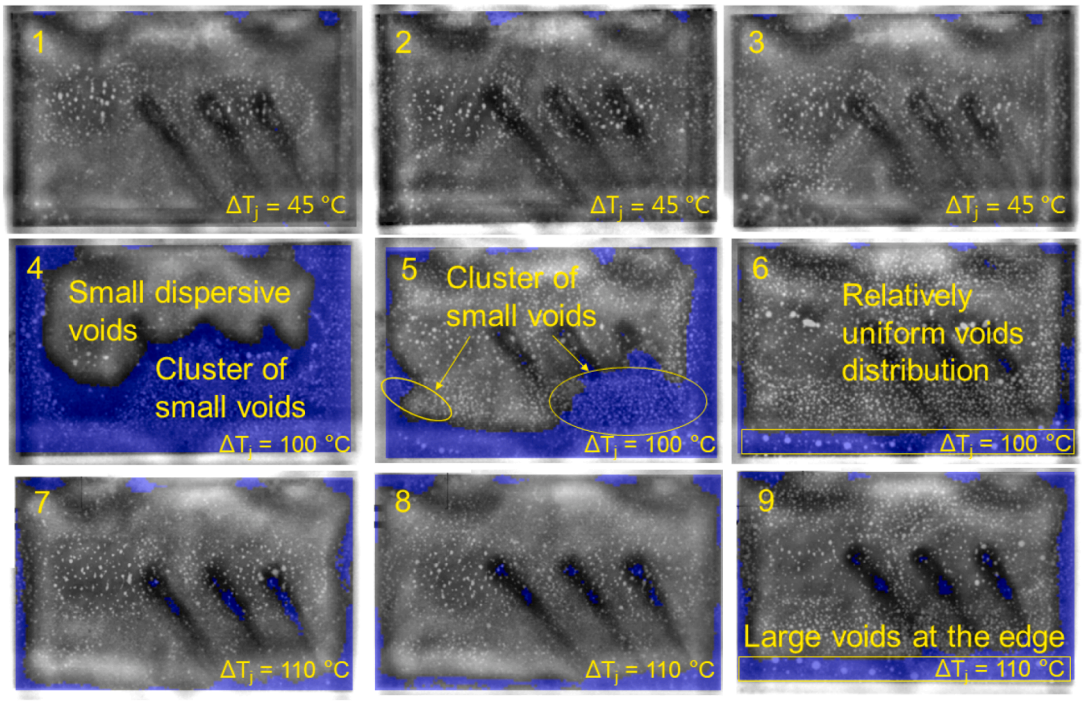

Fig. 10. X-ray images of all samples 1–9, masked with semitransparent T-SAM images (processed with software) of corresponding samples. Degraded areas are indicated by sky blue colour.

larger voids. This removes the notion that small dispersive voids are the fundamental source of the solder's poor mechanical characteristics, as proposed in refs [14,15,18]. These results are consistent with the simulation results shown in refs [13,29,30], particularly with Otiaba et al. [13] work, which demonstrated that ≥ 30% of small voids arrest the spread of cracks to prevent degeneration.

It is noteworthy that in this study, the distribution of small voids in scenario 1 ($\Delta T_j = 45$ °C, sample 1–3), scenario 2 ($\Delta T_j = 100$ °C, sample 6), and scenario 3 ($\Delta T_j = 110$ °C, sample 7–9) exhibits similarities, indicating the examination of the influence of dispersive small voids at varying stress levels. It is observed that small distributed voids remain resilient against solder degradation across different stress levels. The current inquiry pertains to the potential outcome of introducing samples 4 and 5, which possess clusters of voids, from scenario 2 with a temperature swing of $\Delta T_j = 100$ °C, into scenario 1 with a temperature swing of $\Delta T_j = 45$ °C. The degradation of these devices would follow a similar pattern, albeit with more prolonged damage initiation and a slower degradation rate. This is because the lifespan of a device is an exponential function of the die temperature, decreasing by a factor of two to three for every 10 °C increase in temperature [24,25].

4. Conclusions

In this research, the effect of pre-existing voids locations, sizes, and patterns on the mechanical performance of a solder joint in a MOSFET package degrading under varying thermomechanical stress levels has been studied and compared with existing FEM simulation results. The following are the key findings:

Small dispersive voids are useful for the life of solder until they are not in the form of clusters. Since we found that the small dispersive voids are likely to arrest the damage propagation even when initiated at the edges (high-strain and crack propagation path) due to the large dispersive voids. However, clusters of small voids aid in initiating and accelerating damage propagation. The damage initiation interval and solder degradation rate depend upon the clusters' area and the frequencies of small voids in the clusters. Large clusters with frequent voids initiate damage sooner and degrade the solder faster. Small dispersive voids disrupt damage propagation and aid solders in reducing damage initiation and degradation.

On the contrary, large dispersive voids are detrimental to the life of solder until they are away from the high-strain and crack path. It is found that the samples with large dispersive voids at the center, away from high-strain and crack path, have no obvious clues of degradation even after 72,000 cycles at the high-stress level. On the other hand, large dispersive voids at the edges (high-strain and crack paths) have noticeable clues of damage propagation. The experimental results also confirmed that the FEM simulation done by Otiaba et al. [13] is mostly consistent with our actual experimental results and inconsistent with the studies in refs [14,15,18].

The current findings indicate that the positions, sizes, and patterns of pre-existing voids should be taken into account when setting standards for solder void inspection. From a manufacturing perspective, voids should be small and fairly dispersed in a solder joint. The experiment enables the examination of reliability information in silicon power MOSFETs, such as failure modes, mechanisms, and failure locations, which can potentially be utilized as input for reliability enhancement in the power electronics components.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.matdes.2023.112275.

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