Segmented-Vector Pulse Frequency Modulated Three-Level Converter for Wireless Power Transfer

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***Abstract*—Multilevel converters have attracted more and more attention for their advantages over the two-level converters in breaking voltage limitation and multichannel wireless power transfer (WPT), but their switching loss is unbearable due to the lack of an effective soft-switching modulation method. To fill this gap, this article proposes and implements a segmented-vector pulse frequency modulation (SVPFM) of a half-bridge three-level inverter for WPT systems. Moreover, the sigma-delta (Σ-Δ) modulator for the SVPFM-WPT system is proposed, and the modulation range is expanded to [0, 1]. It can achieve wide-range zero voltage switching (ZVS) without auxiliary circuits and inverter modification, and it suppresses the power losses, further improving the system efficiency of a three-level inverter-based WPT system. In the meantime, a switching state-based capacitor voltage balancing method is proposed to control the half-bridge three-level inverter for the WPT system. It can balance the capacitor voltage of the flying capacitor at the reference value with a small voltage ripple. Software simulation and hardware experimentation are both given to verify the feasibility of the proposed Σ-Δ SVPFM of the three-level inverter for WPT systems. The system efficiency can reach 95.2% with the wide-range ZVS operation.**

***Index Terms*—Wireless power transfer, segmented-vector pulse frequency modulation, three-level converter, zero voltage switching.**

I. Introduction

Wireless power transfer (WPT) technology can be traced back over one century to the work of Nikola Tesla. The WPT using magnetic resonant coupling has been extensively investigated and generally applied to various fields [1],[2], such as electric vehicle charging, smartphone charging [3], electric toothbrush charging, and motor driving, due to its safety, convenience, electrical isolation, and better user experience [4]. A growing number of academic researchers and industries hold the belief that the WPT technology will be widely used in the next five to ten years.

Recently, multilevel inverters have attracted more and more attention for their advantage over two-level inverters in breaking voltage limitation and multichannel WPT systems. On the one hand, for some special applications such as 11-kW electric vehicle charging, the gallium-nitride-based two-level inverters cannot be applicable due to voltage limitations, but the WPT system using multilevel inverters allows a higher voltage handling capability. On the other hand, multilevel inverters can be applied for decoupled multichannel WPT systems to eliminate the transformers and simplify the system configuration [6],[7]. Besides, multilevel inverters contain the advantages of reduction in low-order harmonics, low voltage stress, and high reliability [8]. However, switching loss is a serious issue for multilevel inverter-based WPT systems. Thus, to break through the limitation of switching loss, the soft-switching modulation method of multilevel inverters for WPT systems is urgent to be further investigated.

There are several modulation schemes for the two-level inverter-based WPT systems, including pulse-width modulation (PWM), pulse density modulation (PDM), ON-OFF keying modulation, pulse frequency modulation (PFM), and hybrid modulation. Phase-shift control (PSC) [9],[10] regarded as a kind of PWM with a controllable phase angle is generally used in controlling the converters of the WPT system, but it usually suffers from hard switching except for using soft-switching control. ON-OFF modulation uses the low-frequency ON-OFF duty ratios to control the converters [11], but it suffers from low average efficiency and large output ripples. Hybrid modulation combines the PFM and ON-OFF modulation, but it also suffers from large output ripples [12]. By comparison, PDM and PFM are promising ways for the WPT systems due to breakthrough the above limitations.

The PDM for dual-side half-bridge converter-based WPT systems was first proposed in [13] to realize zero-voltage switching (ZVS) and maximum power tracking, and it regulates the density of pulses to change the output power. However, coupling and load conditions influence the soft switching of the PDM-WPT system [11]. To ensure soft switching under various operating conditions, the PDM full-bridge converter for the WPT system with a ZVS branch between switch nodes was proposed in [14], but it suffers from the limitation of the inverter modification, low-frequency subharmonics, narrowed modulation range, and a modulation delay. To solve those issues, a low-subharmonic, full-range, and rapid PDM strategy is proposed in [15]. Furthermore, the improved PDM is gradually proposed in [16] and [17] to decrease the output power fluctuation by switching the inverter from full-bridge mode to half-bridge mode. Given that the output voltage of the half-bridge mode is half of the full-bridge mode, the output ripple is reduced twice. However, the PDM-WPT system needs to add an auxiliary circuit to change the current frequency for maintaining the soft switching.

Needlessly adding the auxiliary circuit, the PFM for WPT systems was proposed in [18]-[21], and it regulates the output power by utilizing the high-order harmonics of the square wave at a specific frequency. The Σ-Δ modulator is presented in [19],

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where the frequency is regulated by increasing or decreasing the comparator indirectly, but the response speed is slow when the frequency is changed from high to low. The half-wave PFM is first proposed in [20],[21], and the half-wave autonomous PFM for the self-excited oscillating WPT system is proposed to offer output power regulation with reliable ZVS [22]. The above studies focus on series compensation topology, studies in [23] further apply PFM to wireless charging with high-order compensation topologies. However, the number of hybrid-frequency pulse sequences needs to be calculated for any given modulated coefficient. To solve this issue and decrease the output ripple, the Σ-Δ modulator of improved PFM is proposed in [24], where the frequency is changed directly by holding different sampling periods of the control system. Recently, from a different perspective, step density modulation that uses the density of steps to regulate the output power is proposed in [25], which has the same waveform as the PFM.

The studies above focus on the modulation methods of two-level inverters for the WPT system. However, the soft-switching modulation method of multilevel inverters needs to be further explored for the WPT systems. Wherein, capacitor voltage balancing is a crucial issue of multilevel inverters [26]-[28]. Thus, considering the special characteristics of the WPT system, a simple and effective capacitor voltage balancing method for the multilevel inverters needs to be investigated.

Motivated by realizing the soft-switching modulation of multilevel inverters for WPT systems, this paper proposes a Σ-Δ segmented-vector pulse frequency modulation (SVPFM) method, the main contributions of this article are listed as:

1) A Σ-Δ SVPFM is proposed to realize the wide-range ZVS of a half-bridge fly-capacitor three-level inverter for the WPT systems.

2) A switching state-based capacitor voltage balancing method is proposed for the fly-capacitor three-level half-bridge inverter, and it can balance the capacitor voltage of the flying capacitor at the reference value with a small voltage ripple.

3) A zero vector is used in the proposed SVPFM method, and it ensures that the duty ratio can range within [0, 1].

The rest of the paper is organized as follows: Section II presents the fundamental principles of the proposed Σ-Δ SVPFM for WPT systems. Section III presents the proposed capacitor voltage balancing method of a multilevel inverter without using current sensors. Section IV presents the experimental verification of the Σ-Δ SVPFM method. Section V draws the conclusions of this work.

II. SVPFM Multilevel Inverter for WPT System

A. WPT System

Fig. 1 shows an equivalent circuit of a series-series compensated WPT system. L_t and L_r are the self-inductances of the coupler, respectively. C_t and C_r are compensated capacitors on the transmitter and receiver sides. The power is transferred from the transmitter side to the receiver side via the mutual inductance M. R_t and R_r are the parasitic resistances of the coils. The three-level half-bridge inverter operates at the resonant frequency of the LC resonators, and the relationship between the LC resonators of the transmitter and receiver sides can be expressed as:

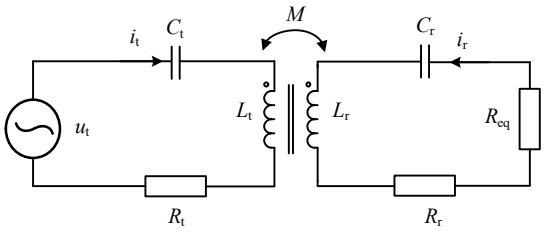

Fig. 1. Equivalent circuit of a WPT system.

$$f_r = \frac{1}{2\pi\sqrt{L_t C_t}} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

where f_r is the resonant frequency.

The circuit equations of the series-series compensated WPT system can be given as follows:

$$\left(j\omega L_t + \frac{1}{j\omega C_t} + R_t\right) i_t + j\omega M i_r = u_t \tag{2}$$

$$j\omega M i_t + \left(j\omega L_r + \frac{1}{j\omega C_r} + R_r + R_{eq}\right) i_r = 0 \tag{3}$$

According to (2) and (3), the input impedance on the transmitter side can be obtained as follows:

$$Z_{in} = \left(j\omega L_t + \frac{1}{j\omega C_t} + R_t\right) + \frac{\omega^2 M^2}{j\omega L_r + \frac{1}{j\omega C_r} + R_r + R_{eq}} \tag{4}$$

Considering that the diode rectifier load is utilized in this paper, R_{eq} is defined as:

$$R_{eq} = \frac{8R_{dc}}{\pi^2} \tag{5}$$

where R_{dc} is the dc-link load.

There exists an optimum load resistance for the WPT system to maximize the efficiency of the system, and it can be expressed as [11]:

$$R_{eq\_opl} = R_r\left(\sqrt{1+\frac{\omega^2 M^2}{R_t R_r}}\right) \tag{6}$$

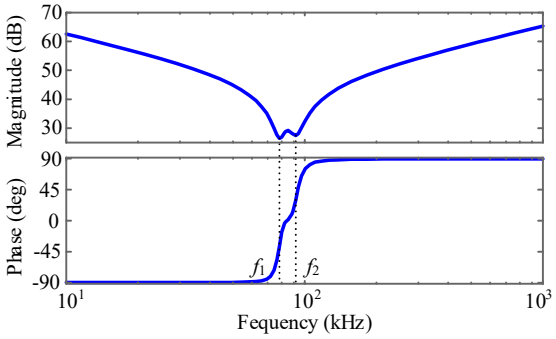

Fig. 2. Bode plot of input impedance Z_{in}.

Fig. 2 shows the bode plot of the input impedance of the WPT system. When the frequency is bigger than f_2 or smaller than f_1, the impedance amplitude of Z_{in} is dramatically increased. It implies that the series-series compensated WPT system characterizes the bandpass filter. Besides, Z_{in} behaves with inductive characteristics while the switching frequency is

slightly bigger than f_r and capacitive characteristics while the switching frequency is slightly smaller than f_r.

B. SVPFM of Multilevel-Inverter-Based WPT System

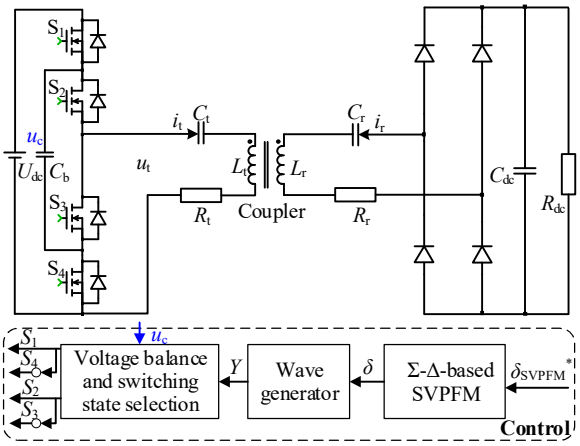

Fig. 3. The SVPFM three-level half-bridge inverter-based WPT system.

Fig. 3 shows the three-level half-bridge flying-capacitor inverter-based series-series compensated WPT system including a transmitter, a receiver, a DC voltage source (U_{dc}), a three-level half-bridge flying-capacitor inverter, a diode rectifier load, and a DC-side capacitor and resistor. C_b is the flying capacitor of the three-level half-bridge inverter. u_c is the DC-side voltage of the flying capacitor. Different from the two-level inverter, the three-level inverters can output voltage pulses with variable amplitude and frequency. It is noticed that only the output waves with periods equaling T_s and $3T_s$ are analyzed. T_s is the WPT resonant period and T_s=1/f_r. As shown in Fig. 3, the control of a three-level flying-capacitor half-bridge inverter-based WPT system consists of Σ-Δ SVPFM, wave generator and capacitor voltage balancing and switching state selection method, which will be discussed in detail in Section II.C. Besides, the flying capacitor voltage needs to be sampled for the proposed voltage balancing method. The switching states of S_1 and S_4 are complementary, and the switching states of S_2 and S_3 are complementary.

Due to the bandpass characteristic of the WPT system as shown in Fig. 2, only the harmonic components at f_r can transfer power from the transmitter side to the receiver side. The two-level inverter can only output voltage wave as shown in Fig. 4(a) and (c), and the fundamental amplitude of output voltage with the frequency f_s can be derived as:

$$U_t = \frac{2f_r U_{dc}}{f_s \pi} = \frac{2U_{dc}}{(2m+1)\pi} = \frac{1}{(2m+1)} V_m \tag{7}$$

where $m \in \mathbb{Z}^+$.

TABLE I
BASIC VOLTAGE VECTORS OF MULTILEVEL INVERTER

F \ M	0	1/k	2/k	3/k	...	1
f_r	0	1/k	2/k	3/k	...	1
f_r/3	0	1/(3k)	2/(3k)	3/(3k)	...	1/3
f_r/5	0	1/(5k)	2/(5k)	3/(5k)	...	1/5
f_r/7	0	1/(7k)	2/(7k)	3/(7k)	...	1/7
...	...	...	...	...	...	...
f_r/(2m+1)	0	1/(2m+1)/k	2/(2m+1)/k	3/(2m+1)/k	...	1/(2m+1)

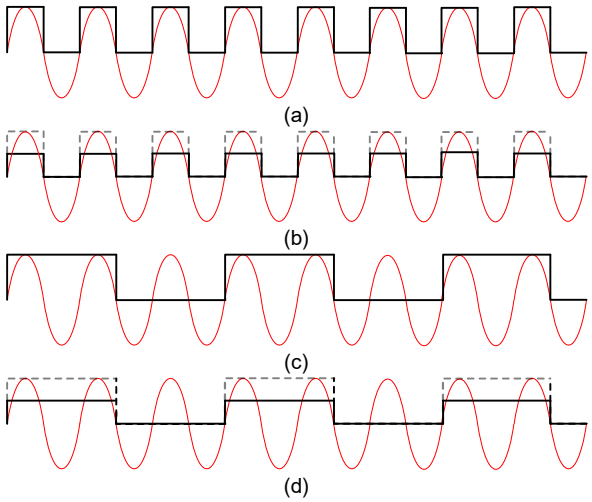

Fig. 4. Transmitter current and basic voltage vectors of three-level inverters for the WPT system (T=1/f_r and 3/f_r). (a) δ=1. (b) δ=1/2. (c) δ=1/3. (d) δ=1/6.

Variable δ denotes the ratio of the fundamental amplitude of output voltage of the multilevel inverter and V_m. The two-level inverter only outputs an amplitude at a frequency point, but the multilevel inverter can output the voltage pulse with different amplitudes and frequencies at the same time. Table I shows the basic voltage vectors of the multilevel inverter by changing the frequency and voltage level, where F and M represent the frequency and magnitude of the voltage level, respectively, and $k \in \mathbb{Z}^+$.

First of all, all the voltage vectors (δ) in Table I are sorted from largest to smallest. If the same values appear, the value with the bigger frequency is removed. All the basic voltage vectors can be used as one part of the quantizer. Supposing three adjacent δ are selected as δ_a, δ_b, and δ_c, thus δ_a>δ_b>δ_c. The quantization is a segmentation function essentially. Then, any segment of the quantization can be obtained as:

$$\begin{cases} y = 1, u \geq \dfrac{1+\delta_b}{2}, \delta_a = 1 \\ y = \delta_b, \dfrac{\delta_b + \delta_c}{2} \leq u < \dfrac{\delta_a + \delta_b}{2} \\ y = 0, u \leq \dfrac{\delta_b}{2}, \delta_c = 0 \end{cases} \tag{8}$$

where u and y are the input and output of the quantizer.

Importantly, define y_1 as the ratio between the period of y and T_s/2, which is used for Σ-Δ SVPFM in section II.C. As shown in Table I, y_1 can be given as:

$$y_1 = \begin{cases} 2, \ y = 0, \dfrac{1}{k}, \dfrac{2}{k}, \dfrac{3}{k}, \cdots, 1 \\ 6, \ y = \dfrac{1}{3k}, \dfrac{2}{3k}, \dfrac{3}{3k}, \cdots, \dfrac{1}{3} \\ \cdots \\ 4m+2, \ y = \dfrac{1}{k(2m+1)}, \dfrac{2}{k(2m+1)}, \cdots, \dfrac{1}{(2m+1)} \end{cases} \tag{9}$$

For example, Fig. 4 shows the basic voltage vectors of the three-level half-bridge inverter with the period equaling T_s and $3T_s$. The basic voltage vectors of the square waves as shown in Fig. 4 are V_m, 1/2V_m, 1/3V_m, and 1/6V_m, respectively. According

to (8), the quantizer of the three-level half-bridge inverter after adding zero voltage vector can be derived as:

$$y=\begin{cases}1, & u\ge\dfrac{3}{4}\\ \dfrac{1}{2}, & \dfrac{5}{12}\le u<\dfrac{3}{4}\\ \dfrac{1}{3}, & \dfrac{1}{4}\le u<\dfrac{5}{12}\\ \dfrac{1}{6}, & \dfrac{1}{12}\le u<\dfrac{1}{4}\\ 0, & u<\dfrac{1}{12}\end{cases} \tag{10}$$

Furthermore, y_1 of the three-level flying-capacitor half-bridge inverter can be expressed as follows:

$$y_1=\begin{cases}6, & y=\dfrac{1}{3},\dfrac{1}{6}\\ 2, & y=0,\dfrac{1}{2},1\end{cases} \tag{11}$$

The SVPFM of a half-bridge inverter-based WPT system utilizes the whole cycles or half cycles of two adjacent voltage vectors to construct the desired $\delta_{\mathrm{SVPFM}}^{*}$ for minimizing the pulse sequence and output ripple. The smallest modulation period is a key parameter that influences the output voltage ripple. The smallest modulation period can be derived as follows:

$$T_{\mathrm{SVPFM}}=\left(m_1N_{\mathrm{m1}}+m_2N_{\mathrm{m2}}\right)T_{\mathrm{s}} \tag{12}$$

where m_1T_{s} and m_2T_{s} represent the periods of the voltage vectors with adjacent amplitudes, respectively; N_{m1} and N_{m2} represent the number of the whole-cycle voltage vectors with adjacent amplitudes, respectively.

By adjusting the number of adjacent amplitude voltage vectors, the equivalent fundamental sinusoidal voltage at the inverter output can be adjusted. For example, in Fig. 5(a), m_1=m_2=1, N_{m1}=3, N_{m2}=2. In Fig. 5(b), m_1=1, m_2=3, N_{m1}=2, N_{m2}=1. The Fourier series expansion of the output voltage waves (u_{t}) of the multilevel inverter can be expressed as:

$$u_{\mathrm{t}}(t)=a_0+\sum_{n=1}^{\infty}\left(a_n\cos 2\pi nft+b_n\sin 2\pi nft\right) \tag{13}$$

where

$$a_0=\frac{1}{\left(m_1N_{\mathrm{m1}}+m_2N_{\mathrm{m2}}\right)T_{\mathrm{s}}}\int_0^{T_{\mathrm{SVPFM}}}u_{\mathrm{t}}(t)dt \tag{14}$$

$$a_n=\frac{2}{\left(m_1N_{\mathrm{m1}}+m_2N_{\mathrm{m2}}\right)T_{\mathrm{s}}}\int_0^{T_{\mathrm{SVPFM}}}u_{\mathrm{t}}(t)\cos 2\pi nftdt=0 \tag{15}$$

$$b_n=\frac{2}{\left(m_1N_{\mathrm{m1}}+m_2N_{\mathrm{m2}}\right)T_{\mathrm{s}}}\int_0^{T_{SVPFM}}u_{\mathrm{t}}(t)\sin 2\pi nftdt \tag{16}$$

Considering the bandpass characteristic of the WPT system, the harmonic components of the voltage wave can be ignored. Thus, the amplitude of the fundamental component of voltage can be derived as:

$$U_{\mathrm{tf}}=b_1=\frac{\lambda_{\mathrm{m1}}N_{\mathrm{m1}}+\lambda_{\mathrm{m2}}N_{\mathrm{m2}}}{\left(m_1N_{\mathrm{m1}}+m_2N_{\mathrm{m2}}\right)}\frac{2U_{\mathrm{dc}}}{\pi} \tag{17}$$

where λ_{m1} and λ_{m2} are the ratios of voltage pulse amplitude to DC-side voltage for two adjacent-amplitude voltage vectors, and λ_{m1} and λ_{m2} can be 0, 1/n, 2/n, 3/n, ⋯, 1, as shown in Table I, where m_1 is the odd number; and m_2=m_1 or m_1+2 or m_1−2.

Without losing the generality, δ_{SVPFM} of the multilevel inverter can be given as:

$$\delta_{\mathrm{SVPFM}}=\frac{\lambda_{\mathrm{m1}}N_{\mathrm{m1}}+\lambda_{\mathrm{m2}}N_{\mathrm{m2}}}{\left(m_1N_{\mathrm{m1}}+m_2N_{\mathrm{m2}}\right)} \tag{18}$$

Table II further shows the voltage vector selection method and the simplified (18) for the three-level half-bridge inverter in detail. As shown in Table II, while $1\ge\delta_{\mathrm{SVPFM}}^{*}>1/2$, voltage vectors of δ_1=1 and δ_2=1/2 are combined to construct the desired $\delta_{\mathrm{SVPFM}}^{*}$; while $1/2\ge\delta_{\mathrm{SVPFM}}^{*}>1/3$, voltage vectors of δ_1=1/2 and δ_2=1/3 are combined to construct the desired $\delta_{\mathrm{SVPFM}}^{*}$; while $1/3\ge\delta_{\mathrm{SVPFM}}^{*}>1/6$, voltage vectors of δ_1=1/3 and δ_2=1/6 are combined to construct the desired $\delta_{\mathrm{SVPFM}}^{*}$; while $1/6\ge\delta_{\mathrm{SVPFM}}^{*}\ge0$, voltage vectors of δ_1=1/6 and δ_2=0 are combined to construct the desired $\delta_{\mathrm{SVPFM}}^{*}$. The output voltage of the half-bridge converter behaves as the half-cycle symmetrical characteristic. If the frequencies of two voltage vectors with adjacent magnitudes are the same, the minimum unit of the output voltage of the three-level half-bridge invert will be the whole cycle of the voltage pulse, as shown in Fig. 5(a); otherwise, the minimum unit of the output voltage will be the half cycle of the voltage pulse, as shown in Fig. 5(b).

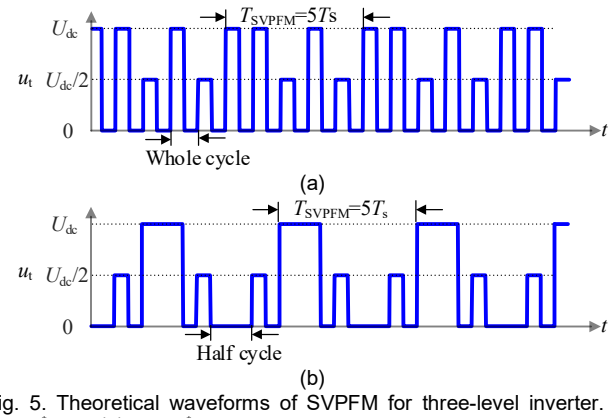

Fig. 5. Theoretical waveforms of SVPFM for three-level inverter. (a) $\delta_{\mathrm{SVPFM}}^{*}$=0.8. (b) $\delta_{\mathrm{SVPFM}}^{*}$=0.4.

TABLE II

COMBINATION FOR DIFFERENT $\delta_{\mathrm{SVPFM}}^{*}$

δ_1=1	δ_1=1/2	δ_1=1/3	δ_1=1/6
δ_2=1/2	δ_2=1/3	δ_2=1/6	δ_2=0
$\dfrac{N_{m1}+0.5N_{m2}}{N_{m1}+N_{m2}}$	$\dfrac{0.5N_{m1}+N_{m2}}{N_{m1}+3N_{m2}}$	$\dfrac{N_{m1}+0.5N_{m2}}{3N_{m1}+3N_{m2}}$	$\dfrac{N_{m1}}{3N_{m1}+N_{m2}}$
$1\ge\delta_{\mathrm{SVPFM}}^{*}\ge1/2$	$1/2\ge\delta_{\mathrm{SVPFM}}^{*}\ge1/3$	$1/3\ge\delta_{\mathrm{SVPFM}}^{*}\ge1/6$	$1/6\ge\delta_{\mathrm{SVPFM}}^{*}\ge0$

C. Delta-Sigma Modulator of SVPFM

It is important to realize the SVPFM at any given $\delta_{\mathrm{SVPFM}}^{*}$, and a general way to obtain the higher resolution is Σ-Δ modulator. As depicted in Fig. 6(a), this paper proposes a Σ-Δ modulator structure for SVPFM. The modulator has two input signals. One is continuous input pulses and the other is the given $\delta_{\mathrm{SVPFM}}^{*}$. The rising edges of the input pulses trigger the integrator (sigma), and the input of the integrator is the difference (delta) between the given $\delta_{\mathrm{SVPFM}}^{*}$ and the output of Latch. The quantizer of the SVPFM for the three-level half-bridge inverter is shown in (10) and (11). According to the

output (u) of the integrator, the quantizer will output the magnitude denoted as y and the period ratio denoted as y_1. The gain K of the integrator can regulate the filter characteristic and response speed of the Σ-Δ modulator. Besides, a latch is utilized to change the frequency of output voltage of the three-level half-bridge converter. The latch unit samples and holds the magnitude y for $y_1T_s/2$. The waveform generator units of SVPFM need to produce voltage waves with variable frequency and amplitude. As for the three-phase half-bridge inverter, y_1 in (11) should be divided by 2 to produce the half cycle of voltage pulse when δ_{SVPFM}^* ranges within (1/3, 1/2) and y=1/2 or 1/3.

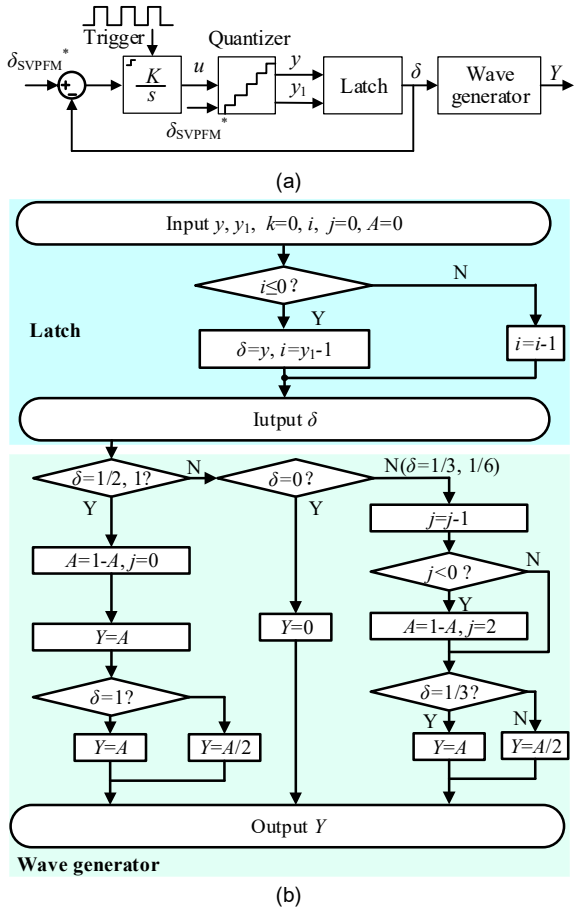

Fig. 6. Σ-Δ SVPFM for the three-level inverter. (a) Modulator. (b) Latch and wave generation.

Fig. 6(b) shows the realizations of the Latch and wave generator in detail. As shown in Fig. 6(b), in every control period, if i is positive, i is equal to i-1 and δ remains unchanged; otherwise, δ is equal to y and i is equal to y_1-1. In this way, δ can output y by holding y_1 control periods. Furthermore, together with the Latch, the wave generator of SVPFM produces the key waves as shown in Fig. 5. In Fig. 6(b), "A" is a variable that constantly flips between zero and one. While δ is equal to 1/2 or 1, "A" flips between 0 and 1 in one control period; moreover, if δ is equal to 1/2, the output of the wave generator is A/2; if δ is equal to 1, the output of the wave generator is A. While δ is equal to 1/3 or 1/6, "A" flips between 0 and 1 in three control periods; moreover, if δ is equal to 1/6, the output of the wave generator is A/2; if δ is equal to 1/3, the output of the wave generator is A. While δ is equal to 0, "A" remains unchanged, and the output of the wave generator is 0. Thus, the output of the wave generator consists of "1", "0.5" and "0".

Fig. 7 shows the waveforms of the proposed Σ-Δ SVPFM for the case of δ_{SVPFM}^*=0.4. In this scenario, the modulation period consists of ten switching cycles which is the minimum solution. Furthermore, every modulation period contains two half-cycle voltage vectors with δ equaling 1/3 and two voltage vectors with δ equaling 1/2.

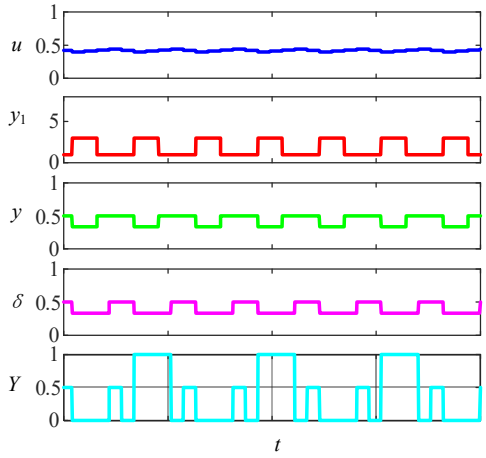

Fig. 7. Waveforms of proposed Σ-Δ SVPFM for δ_{SVPFM}^*=0.4.

III. Capacitor Voltage Balancing of Three-Level Inverter for WPT System

A. Capacitor Voltage Balancing of SVPFM WPT System

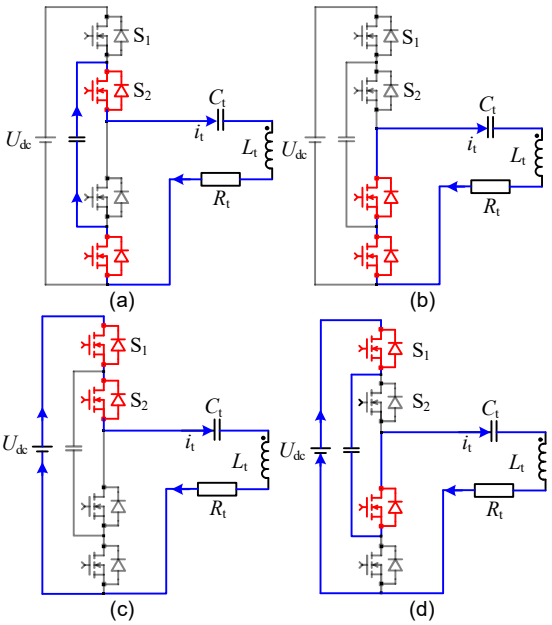

Fig. 8. Switching modes of three-level half-bridge inverter. (a) State "01", U_{dc}/2, and capacitor discharging. (b) State "00", and zero voltage. (c) State "11", and U_{dc}. (d) State "10", U_{dc}/2, and capacitor charging.

The capacitor voltage balance of the three-level flying-capacitor inverter for the WPT system is very important. Fig. 8 shows the valid switching modes of the three-level half-bridge inverter. Fig. 8(b) shows mode "00" operations of the flying capacitor three-level inverter, where S_1 and S_2 turn

off, while S_3 and S_4 turn on. It produces zero voltage while keeping the voltage of the flying capacitor. Fig. 8(c) shows mode "11" operations of the flying capacitor three-level inverter, where S_3 and S_4 turn off, while S_1 and S_2 turn on. It produces an output voltage of U_{dc} while keeping the voltage of the flying capacitor. Fig. 8(a) shows mode "01" operations of the flying capacitor three-level inverter, where S_1 and S_3 turn off, while S_2 and S_4 turn on. Fig. 8(d) shows mode "10" operations of the flying capacitor three-level inverter, where S_2 and S_4 turn off, while S_1 and S_3 turn on. Both mode "10" and "01" produce the output voltage of $U_{dc}/2$. However, when the transmitter current is positive, mode "01" charges the flying capacitor while mode "10" discharges the flying capacitor. When the transmitter current is negative, mode "01" discharges the flying capacitor while mode "10" charges the flying capacitor. Thus, the switching modes of "10" and "01" can be used to balance the capacitor voltage.

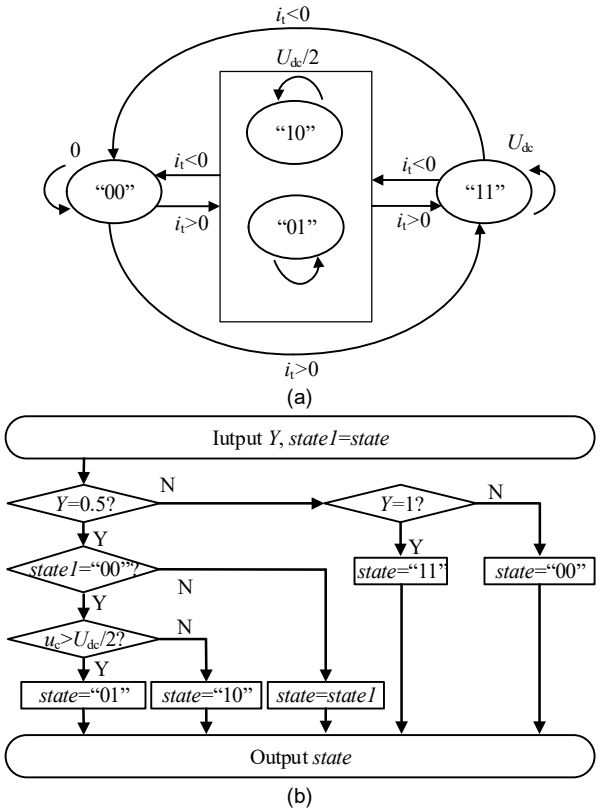

Fig. 9. The proposed voltage balancing and switching state selection method. (a) Switching transitions. (b) The flow chart.

As discussed above, voltage levels like U_{dc} and 0 only have one switching state, which is created by closing all upper or bottom switches. As no flying capacitors are connected, the two switching states for voltage levels U_{dc} and 0 do not influence the capacitor voltage balance. Considering that the voltage level of $0.5U_{dc}$ has redundant switching states, two switching states leading to opposite capacitor charging directions need to be selected.

Fig. 9(a) shows all the switching state transitions of the three-level half-bridge inverter. The three-level half-bridge inverter can output three kinds of voltage levels. It can be observed that the transmitter current i_t is negative while the output voltage of the three-level inverter changes from U_{dc} to $U_{dc}/2$ or 0. The transmitter current i_t is positive while the output voltage of the three-level inverter changes from 0 to $U_{dc}/2$ or U_{dc}. Thus, the transmitter current i_t can be judged by the switching state instead of measuring.

Fig. 9(b) shows the proposed switch state selection and voltage balance method. The flying-capacitor voltage (u_c) as shown in Fig. 3 needs to be measured. The last switching state is recorded in every control period, denoted as *state1=state* in Fig. 9(b). Then, if the output of the Σ-Δ SVPFM is 1, the switching state is selected as "11". If the output of the Σ-Δ SVPFM is 0, the switching state is selected as "00".

When the output of the Σ-Δ SVPFM is 0.5, state "10" or "01" needs to be judged for balancing capacitor voltage. Considering the last voltage level might be U_{dc}, $U_{dc}/2$, or 0, thus, there are three cases to be discussed. If the last switching state is "10" or "01", the switching state is kept. In every control period, i_t will change its direction. Thus, in the switching state from "10" to "10" or "01" to "01", the capacitor voltage fluctuation will be eliminated. If the last voltage level is 0, i_t will be positive in this switching period. In this case, if u_c is bigger than the reference value, switching state "01" should be selected to discharge the capacitor; otherwise, switching state "01" should be selected to charge the capacitor. If the last voltage level is U_{dc}, i_t will be positive in this switching period. In this case, if u_c is bigger than the reference value, switching state "01" should be selected to discharge the capacitor; otherwise, switching state "10" should be selected to charge the capacitor. It is noticed that the output voltage of the SVPFM three-level inverter contains no voltage step from U_{dc} to $U_{dc}/2$, thus, the third case can be neglected.

To further explain the charging/discharging process of the proposed method, Fig. 10 shows an example of the flying capacitor charging/discharging when δ_{SVPFM}^*=0.6. As shown in Fig. 10, only a half-wave transmitter current is used for charge/discharging. The charging and discharging of the flying capacitor of the three-level half-bridge inverter is proportional to the integral of the transmitter current of the WPT system. The balancing algorithm execution frequency is twice the switching frequency to ensure the lowest possible voltage variation in the flying capacitor voltage. Therefore, during a control period, the flying-capacitor voltage variation will be

$$\Delta u_c = \frac{1}{C_b}\int_0^{T_s/2} i_t(t)dt = \frac{I_t T_s}{\pi C_b} \tag{19}$$

where I_t is the peak value of the transmitter current.

When δ_{SVPFM}=1, the fundamental component of i_t for the WPT system is maximum. In this case, the average transmitter current is twice the DC-side current.

$$\frac{2I_{tr}}{\pi} = \frac{2P_r}{U_{dc}} \tag{20}$$

where I_{tr} is the rating value of the I_t; P_r is the rating input power of the WPT system.

Considering the influence of harmonic current, the maximum peak value of the transmitter current can be given as

$$I_{tmax} = kI_{tr} \tag{21}$$

where k is a correction factor ranging in (1, 1.2).

According to (19)-(21), the voltage ripple of the flying capacitor can be derived as follows:

$$\Delta u_c \le \frac{I_{tmax} T_s}{\pi C_b} = \frac{k P_r T_s}{C_b U_{dc}} \tag{22}$$

As shown in Fig. 10, the voltage ripple is ±1.1 V, which is completely consistent with (22). Based on (22), the capacitor should be selected as follows:

$$C_b \ge \frac{2 k P_r T_s}{\varepsilon U_{dc}^{\ 2}} \tag{23}$$

where ε is the voltage ripple rate of the flying capacitor, and $\varepsilon = 2\Delta u_c / U_{dc}$.

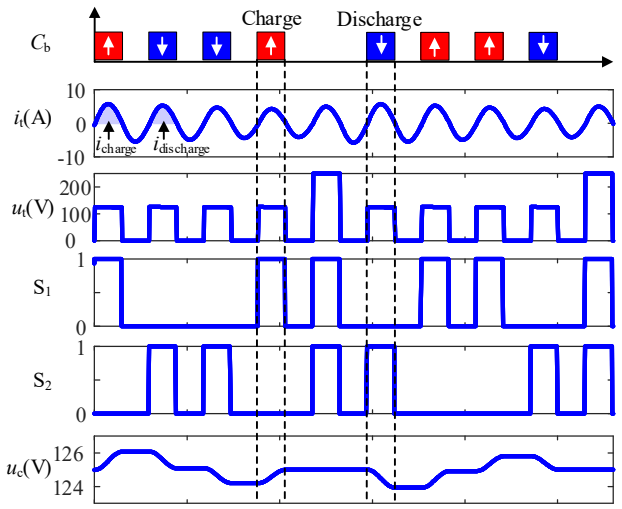

Fig. 10. Simulation results of the flying capacitor charging/discharging when δ_{SVPFM}^{*}=0.6 and C_b=22 uF.

B. Zero-Voltage Switching Analysis

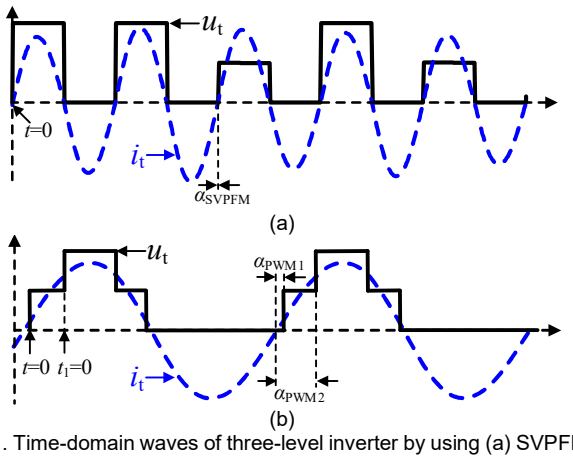

Fig. 11. Time-domain waves of three-level inverter by using (a) SVPFM, δ_{SVPFM}=0.6. (b) PWM, d_{pwm}=0.6.

According to (13) and (18), the Fourier series expansion of the output voltage waves (u_t) of the multilevel inverter using SVPFM can be further derived as

$$u_t = \frac{\delta_{SVPFM} U_{dc}}{2} + \delta_{SVPFM} \sum_{n=1}^{\infty} \frac{U_{dc}}{n\pi} \left(1 - \cos(n\pi)\right) \sin n\omega t \tag{24}$$

According to (24), the switching angles of SVPFM α_{SVPFM} as shown in Fig. 11(a) is always equal to zero. While the switching frequency is equal to the resonant frequency, the phases of u_t and i_t are consistent. By comparison, selecting t=0 as the timeline, u_t of the multilevel inverter using the conventional PWM in the Appendix can be derived as

$$u_t = \frac{(D_1 + D_2) U_{dc}}{2} + \sum_{n=1}^{\infty} \frac{U_{dc}}{n\pi} \begin{pmatrix} (\sin n\pi D_1 + \sin n\pi D_2) \\ \cos[n\pi D_1 - n\omega t] \end{pmatrix} \tag{25}$$

Based on (25), the switching angle of PWM (α_{pwm1}) as shown in Fig. 11(b) is derived as

$$\alpha_{pwm1,\,n} = (0.5 - D_1) n\pi \tag{26}$$

Similarly, selecting t_1=0 as the timeline, α_{pwm2} is derived as

$$\alpha_{pwm2,\,n} = (0.5 - D_2) n\pi \tag{27}$$

Thus, under the PWM, zero switching angles can be realized only when D_1=D_2=0.5. The smaller duty ratios (D_1 and D_2) lead to bigger switching angles, which means that ZVS will not be maintained when changing the duty ratio of the PWM. By comparison, under the SVPFM, the switching angle is always zero when changing the voltage ratio δ_{SVPFM}, thus, the ZVS of the SVPFM is easier to realize compared with PWM.

The input impedance of the series-series compensated WPT system is inductive while the switching frequency is slightly higher than the resonant frequency or the transmitter capacitor is increased. When the transmitter capacitor is increased, according to (4), the input impedance of the WPT system will be expressed as

$$Z_{in}(\omega_r) = |Z_{in}| e^{j\alpha} = j \frac{\Delta C}{\omega_r C_r (C_r - \Delta C)} + R_t + \frac{\omega_r^{\ 2} M^2}{R_r + R_{eq}} \tag{28}$$

where ΔC is the increased capacitance; $\omega_r = 2\pi f_r$.

According to (28), the magnitude and phase of Z_{in} at the resonant frequency can be approximately regarded as

$$|Z_{in}| \approx R_t + \frac{\omega_r^{\ 2} M^2}{R_r + R_{eq}} \tag{29}$$

$$\tan\alpha = \frac{(R_{eq} + R_r)\Delta C}{(\omega_r^{\ 2} M^2 + R_t R_r + R_t R_{eq}) \omega_r C_r^{\ 2}} = m \frac{\Delta C}{C_r} \tag{30}$$

While the switch state is changed from "00" to "11" as shown in Fig. 12(a), i_t lags u_t slightly during the dead time, and the phase difference is α. The C_{oss} of S_1 and S_2 will be discharged and the C_{oss} of S_3 and S_4 will be charged by the transmitter current i_t, as shown in Fig. 12(b), where Q_{zvs} means the integral of i_t during the dead time. The ZVS of the three-level inverter can be realized when Q_{zvs} can charge/discharge the C_{oss}:

$$Q_{zvs} = \int_0^{T_d} i_t dt \ge \int_0^{U_{dc}/2} (C_{oss1} + C_{oss2} + C_{oss3} + C_{oss4}) dv \tag{31}$$

where C_{oss1}, C_{oss2}, C_{oss3}, and C_{oss4} represent the drain-source capacitors of S_1, S_2, S_3 and S_4, respectively.

The transmitter current i_t during the dead time is assumed to be part of the sine waves. Based on this assumption, according to (21) and Fig.10 (b), the minimum phase difference α_{min} and dead time T_{dmin} can be derived as follows:

$$\alpha_{min} = \cos^{-1}\left(1 - \frac{\omega_r C_{osst} U_{dc}}{I_t}\right) \tag{32}$$

where C_{osst}=C_{oss1}+C_{oss2}+C_{oss3}+C_{oss4}.

$$T_{dmin} = \frac{\alpha_{min}}{\omega_r} \tag{33}$$

According to (24), ignoring the influence of the harmonic current, I_t can be calculated as

$$I_t = \frac{2\delta_{SVPFM} U_{dc}}{\pi |Z_{in}|} \tag{34}$$

According to (29)-(34), the relationship between the desired increased capacitor (ΔC) and the load condition (R_{eq}) to realize the ZVS can be derived as follows:

$$\frac{\Delta C}{C_r} \geq \frac{1}{m} \sqrt{\frac{16\delta_{SVPFM}^{\ 2}}{\left(4\delta_{SVPFM} - \pi\omega_r C_{osst}\left(R_t + \frac{\omega_r^{\ 2} M^2}{R_r + R_{eq}}\right)\right)^2} - 1} \tag{35}$$

It should be noted that increasing the transmitter capacitor can decrease the transfer power of the WPT system. Thus, $\Delta C/C_r$ cannot be very big, and it is suggested to be 5% to realize wide-range ZVS during power control [21].

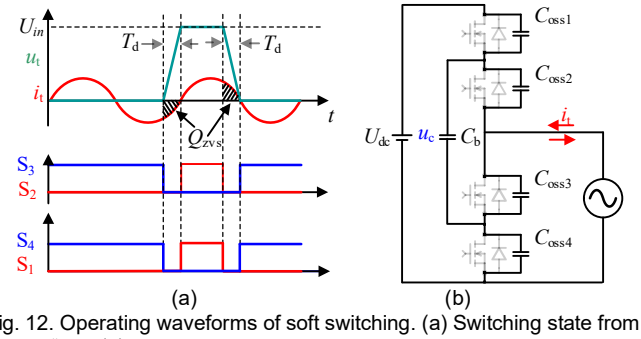

Fig. 12. Operating waveforms of soft switching. (a) Switching state from "00" to "11". (b) Equivalent circuit during dead time.

IV. Experimental Verification

A. Hardware Implementation

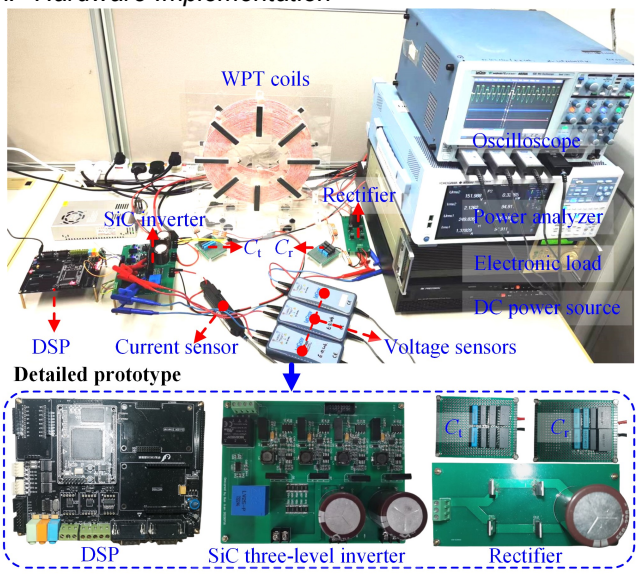

Fig. 13. Experimental system.

To verify the feasibility of the proposed Σ-Δ SVPFM-based WPT system, a practical system with a 400W prototype is constructed for experimentation. As shown in Fig. 13, the system consists of a DC power source, a power analyzer, a silicon-carbide-based three-level flying-capacitor half-bridge inverter with drivers, a WPT circuit, a bridge rectifier, an electronic load, a 24V auxiliary voltage source, and TMS320FDSP28335 board. The transmitter and receiver coils are copper Litz wire. The DC power source (MR50040) provides the DC-link input voltage, and the power analyzer (YOKOGAWA WT5000) is utilized to measure the input and output power. The system parameters are listed in Table III.

TABLE III
System Parameters of the WPT System

Items	Value
DC-link voltage (U_{dc})	250 V
Primary compensated capacitance (C_t)	13.40 nF
Primary coil inductance (L_t)	272.70 μH
Parasitic resistance of L_t in series with C_t	0.275 Ω
Secondary compensated capacitance (C_r)	13.30 nF
Secondary coil inductance (L_r)	269.79 μH
Parasitic resistance of L_r in series with C_r	0.278 Ω
Distance between two coils (d)	9 cm
Mutual inductance (M)	75.2 μH
Resonant frequency (f_r)	85 kHz
Output capacitance (C_o)	TDA 550V/220 μF
Flying capacitance (C_b)	TDA 450 V/470 μF
Load resistance (R_{dc})	59.82 Ω
Dead time (T_d)	150 ns
Integration coefficient (K)	0.2
Digital signal processer	TMS320F28335
SiC MOSFET	SCT3060
Diode	CVFD20065A
Voltage sensor	LV25-P
Measured system efficiency (η)	95.2%

B. Zero-Voltage Switching

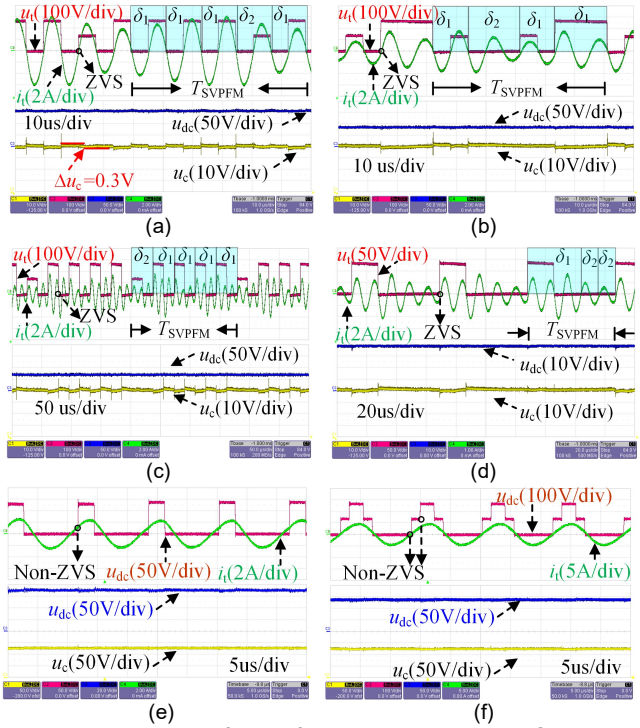

Fig. 14. Measured waveforms of the WPT system using SVPFM and PWM. (a) δ_{SVPFM}^*=0.9. (b) δ_{SVPFM}^*=0.4. (c) δ_{SVPFM}^*=0.3. (d) δ_{SVPFM}^*=0.1. (e) d_{pwm}=0.25. (f) d_{pwm}=0.75.

Fig. 14(a)-(d) shows the operating waveforms of a three-level inverter-based WPT system by using the proposed SVPFM and PWM. When δ_{SVPFM}^*=1, the capacitor voltage u_c does not have to be balanced at the reference value. When $\delta_{SVPFM}^* \neq 1$, Fig. 14(a)-(d) shows that the capacitor voltage can

be balanced at around 125V. Besides, the capacitor voltage ripples caused by the charging/discharging current are very small ($\Delta u_c \leq 0.3$ V), because the capacitor is big enough, which matches closely with (22).

While $\delta_{SVPFM}^*=0.9$, as shown in Table II, $(N_{m1}+0.5N_{m2})/(N_{m1}+N_{m2})=0.9$. The minimum solutions ($N_{m1}=4$ and $N_{m2}=1$) can be calculated. It means that u_t will consist of four whole-cycle voltage pulses with $\delta_1=1$ and one whole-cycle voltage pulses with $\delta_2=1/2$ when $\delta_{SVPFM}^*=0.9$, which has been verified by the experimental results in Fig. 14(a). While $\delta_{SVPFM}^*=0.4$, according to Table II, N_{m1} and N_{m2} can be calculated to be 2 and 1, respectively, to realize the minimum period of the output voltage. As shown in Fig. 14 (b), u_t consists of two half-cycle voltage pulses with $\delta_1=1$ and two whole-cycle voltage pulses with $\delta_2=1/2$ when $\delta_{SVPFM}^*=0.4$. Moreover, as shown in Fig. 14(c) and (d), u_t consists of four whole-cycle voltage pulses with $\delta_1=1$ and one whole-cycle voltage pulses with $\delta_2=1/2$ when $\delta_{SVPFM}^*=0.3$, and u_t consists of the voltage output with $\delta=1/6$ and zero vector when $\delta_{SVPFM}^*=0.1$.

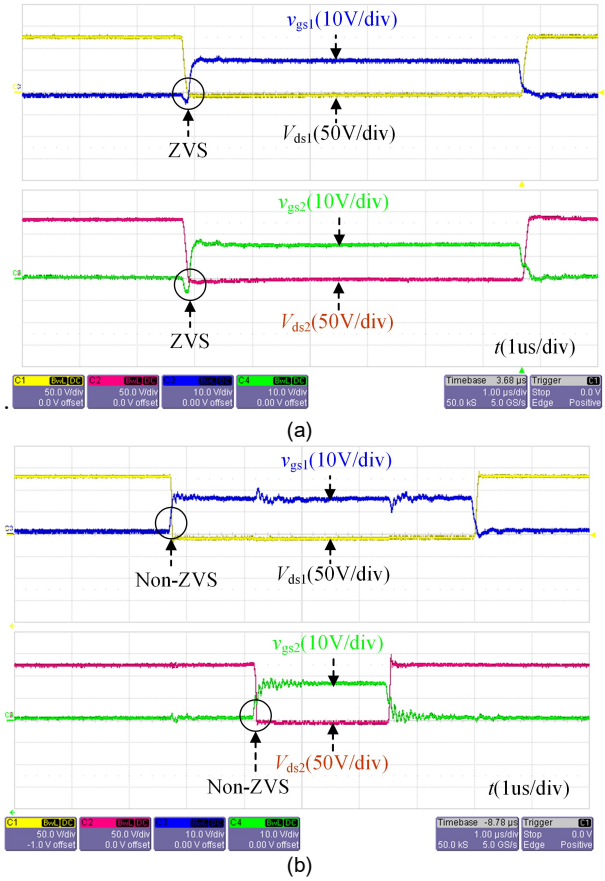

Fig. 15. Measured switching waveforms comparison of SVPFM and PWM in [7]. (a) $\delta_{SVPFM}=0.9$.(b) $d_{pwm}=0.8$.

The minimum periods of the output voltage shown in Fig. 14(a), (b), (c), and (d) are $5T_s$, $5T_s$, $15T_s$, and $5T_s$, respectively, which are consistent with the calculated results. It means that the delta-sigma SVPFM enables the three-level inverter to output voltage with the optimal solution of N_{m1} and N_{m2}.

Fig. 14(e) and (f) show experimental waves of the PWM three-level inverter-based WPT with $d_{pwm}=0.8$ and $d_{pwm}=0.3$. By comparison, all the switches in the SVPFM three-level inverter-based WPT system can realize the ZVS with different δ_{SVPFM}^*, but only in the case of $d_{pwm}=1$, all switches in the three-level inverter-based WPT system using the PWM in the Appendix can realize ZVS. Furthermore, Fig. 15 shows the comparative switching waveforms of PWM-WPT system and SVPFM-WPT system, V_{ds1}, and V_{gs1}, V_{ds2}, and V_{gs2}, when $\delta_{SVPFM}^*=0.9$ and $d_{pwm}=0.8$, where v_{ds1} and v_{gs1} are the drain-source voltage and gate-source voltage of the switch S_1, respectively; V_{ds2} and V_{gs2} are the drain-source voltage and gate-source voltage of the switch S_2, respectively. As shown in Fig. 15(a), it can be observed that V_{gs1} becomes high-level voltage after V_{ds1} becomes zero and V_{gs2} becomes high-level voltage after V_{ds2} becomes zero, indicating that both S_1 and S_2 can realize reliable ZVS for the SVPFM-WPT system. The operating characteristics of the S_3 and S_4 are the same as S_2 and S_1, respectively. Thus, all of them for the SVPFM-WPT system can realize the desired ZVS. By comparison, Fig. 15(b) shows that V_{gs1} becomes high-level voltage before V_{ds1} becomes zero and V_{gs2} becomes high-level voltage before V_{ds2} becomes zero, indicating that both S_1, S_2, S_3, and S_4 cannot realize ZVS for the PWM-WPT system while $D_1 \neq 0.5$ and $D_2 \neq 0.5$. These measured results confirm the ZVS operation of the proposed SVPFM, which well agrees with the theoretical analyses.

C. Step Response of the SVPFM-WPT system

Furthermore, Fig. 16 shows the step responses and their zoom-in waveforms by using the proposed SVPFM technique with varying δ_{SVPFM} and DC-side load. With an increasing δ_{SVPFM} from 0.2 to 0.8 in Fig. 16(a), the DC-side voltage of the flying capacitor has insignificant change, and the DC-side output voltage of the WPT system has a fast step response without overshoot, and the response time is 0.08 s. With an increasing load from 40.84 Ω to 68.94 Ω in Fig. 16(b), the DC-side voltage of the flying capacitor also remains unchanged. Considering the SS compensated WPT system behaves the current-source characteristic, thus, the DC-side output voltage of the WPT system also has a fast step response without overshooting while the load is quickly increasing, and the response time is also 0.08 s. Besides, during the step-response period of 0.08s, there exist cases where the ZVS fails. However, we only focus on the steady-state ZVS characteristic, and the ZVS is realized after the step response. Fig. 16 shows that the WPT system by using the proposed flying capacitor voltage balancing method is quite stable for the step response.

D. Efficiency and Power Loss Evaluation of the SVPFM-WPT system

Fig. 17 (a) compares the efficiency of the PWM WPT system and SVPFM WPT system with different output power by changing the δ_{SVPFM}^* or d_{pwm}. The maximum efficiency (95.2%) occurs at the point of maximum power. Over a wide output power range, the system efficiency of the SVPFM WPT system is maintained at more than 90%. The system efficiency of the PWM WPT system is gradually decreased with decreasing d_{pwm} from (0.5, 1] or [0, 0.5]. During power control, the three-level inverter-based WPT system using the SVPFM can achieve higher system efficiency by up to 1.49% while d_{pwm} or δ_{SVPFM}^* ranging in (0.5, 1] and 12.70% while d_{pwm} or δ_{SVPFM}^* ranging in [0, 0.5], than that using the PWM.

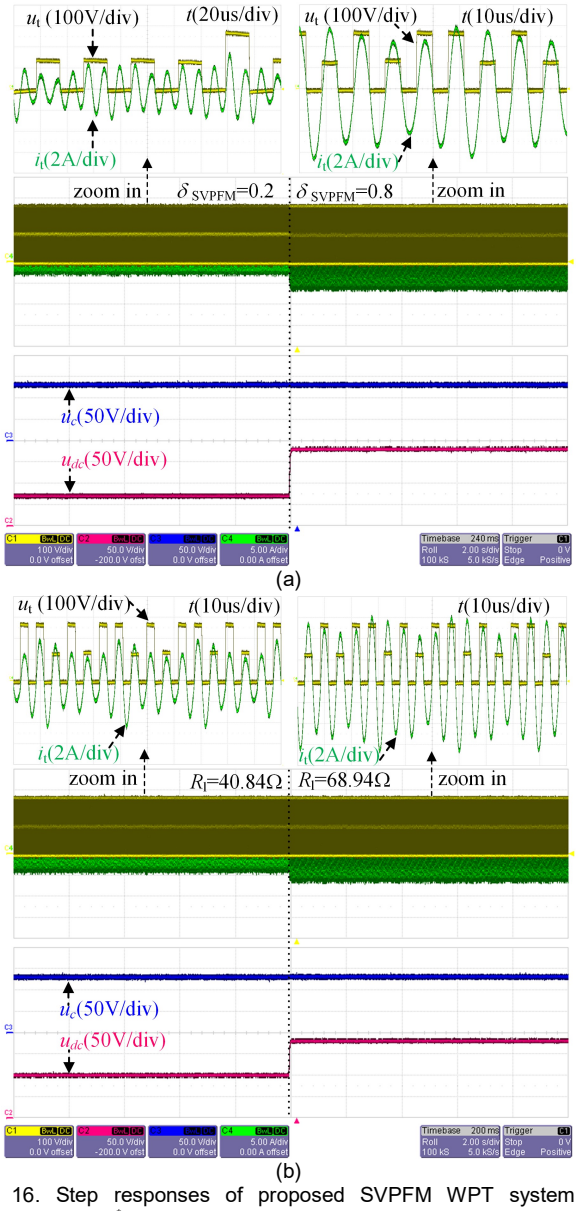

Fig. 16. Step responses of proposed SVPFM WPT system (a) increasing δ_{SVPFM}^*. (b) increasing R_l (δ_{SVPFM}=0.8).

While the other parameters are fixed, the power level is proportional to the square of the input voltage. Fig. 17(b) shows the system efficiency with different power levels by changing the input voltage. As shown in Fig. 17(b), the system efficiency is gradually increased with increasing the power level, and the system efficiency is 95.59% while the power level is twice the rated power. Fig. 17(c) shows the system efficiency with changing the air gap between the transmitter and receiver coils. As shown in Fig. 17(c), the system efficiency is gradually decreased with increasing the air gap. The system efficiency is obviously influenced by the air gap, and the system efficiency is 91.6% while the air gap is 13 cm.

Fig. 17(d) shows the system efficiency with changing the horizontal misalignment distance (Δl) of the transmitter and receiver coils. The coil diameter at the transmitting and receiving ends is 30 cm. As shown in Fig. 17(d), while Δl is changing from 0 to 10 cm, the system efficiency is gradually decreased. In case of 10 cm misalignment, the system efficiency is around 89.7%. Given that the misalignment case is not the main focus of this paper, it is not evaluated in detail.

Fig. 17(e) and (f) compare the system efficiency of WPT using PWM and SVPFM with variable loads. When d_{pwm}=0.82 and δ_{SVPFM}^*=0.8 or d_{pwm}=0.6 and δ_{SVPFM}^*=0.62, the WPT system using PWM or SVPFM has the same output power. The efficiency of the WPT system by using SVPFM is improved under the 30%-100% load compared with the WPT system by using PWM. Under the heavy load, the ZVS of SVPFM leads to the efficiency difference. There exists a boundary load that leads to the failure of the ZVS for the proposed SVPFM, but the efficiency of the proposed method is still a little higher than that of PWM. By using SVPFM, as discussed in III.B, the switching angle of SVPFM is zero. It means that the MOSFETs turn on at the moment when the transmitter current is always around 0, thus, the switching loss of SVPFM is lower than that of PWM even in the Non-ZVS state.

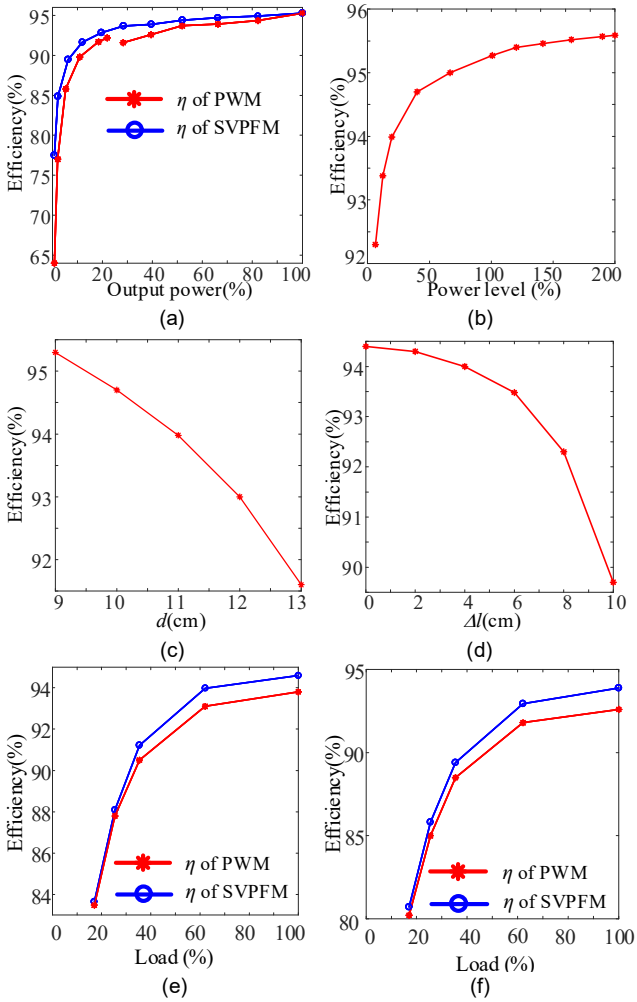

Fig. 17. Efficiency of WPT system. (a) Comparison between PWM and SVPFM by changing δ_{SVPFM} and d_{pwm} (b) With different power levels by changing the input voltage (δ_{SVPFM}^*=1) (c) With different air gap (δ_{SVPFM}^*=1). (d) With different misalignment distances (δ_{SVPFM}^*=0.7). (e) With different loads (δ_{SVPFM}^*=0.8). (f) With different loads (δ_{SVPFM}^*=0.6).

The total power loss of the SVPFM-WPT system by ignoring that of SiC drivers can be given as follows:

$$P_t = P_{tr} + P_I + P_D \tag{36}$$

where P_{tr} is the transfer network loss including the transmitter and receiver coils, and transmitter and receiver capacitors; P_I is the power loss of the three-level flying-capacitor half-bridge inverter; P_D is the power loss of the diode rectifier.

The input power (P_{in}), output power (P_{out}), inverter output power (P_1), and input power of the diode rectifier (P_2) are measured by the power analyzer (WT5000). Thus, the power loss of the diode rectifier and the power loss of the three-level flying-capacitor half-bridge inverter can be obtained as:

$$\begin{cases} P_I = P_{in} - P_1 \\ P_D = P_2 - P_{out} \\ P_{tr} = P_{in} - P_{out} - P_I - P_D \end{cases} \tag{37}$$

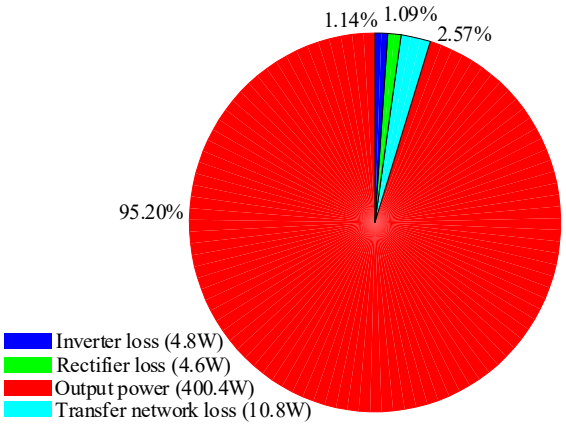

Fig. 18. Output power and various loss components.

Hence, the percentage of loss components with respect to the output power can be calculated. As shown in Fig. 18, the transfer network loss accounts for 2.57%, which is the maximal. The power loss of the three-level flying-capacitor half-bridge inverter accounts for 1.14%, which is similar to the power loss of the diode rectifier. Table III shows the comparison between the proposed technology and the conventional one. As shown in Table IV, compared with the existing method, the proposed one has a higher voltage handling capability and can realize ZVS for a three-level inverter-based WPT system.

V. Conclusions

This paper has proposed and implemented a Σ-Δ SVPFM method of the three-level converter for the WPT system. Some conclusions are summarized as follows:

1) This paper has newly proposed the Σ-Δ SVPFM method of three-level inverters for WPT systems. It can realize the wide-range ZVS of the three-level inverter-based WPT system without adding an auxiliary circuit.

2) The switching state-based capacitor voltage balancing method of the fly-capacitor three-level inverter for the WPT system has been proposed.

3) A zero vector is used in the proposed SVPFM method, which ensures that its duty ratio can range within [0, 1]. In this case, the application range of the SVPFM can be expanded.

Finally, both theoretical derivation and experimental verification are given to verify the feasibility of the proposed Σ-Δ SVPFM three-level converter for WPT.

VI. Appendix

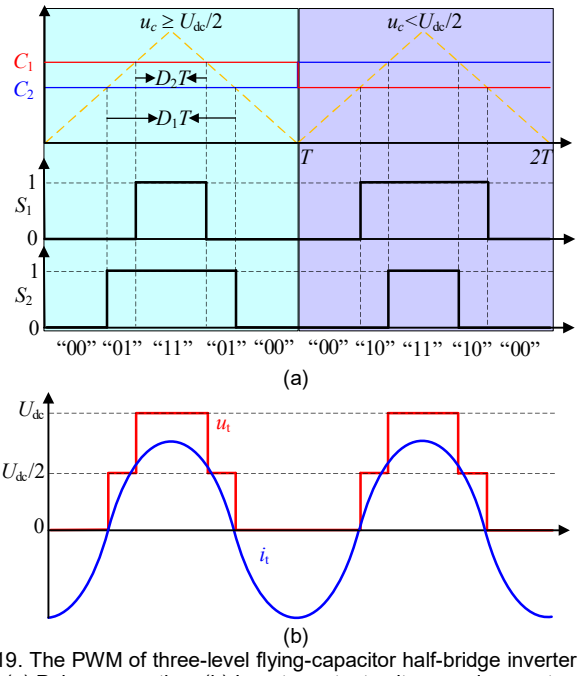

Fig. 19. The PWM of three-level flying-capacitor half-bridge inverter for WPT (a) Pulse generation. (b) Inverter output voltage and current.

Fig. 19 shows the conventional PWM method of a three-level flying-capacitor half-bridge inverter for the WPT system, and the similar PWM method for the three-phase full-bridge T-type inverter can be found in [7]. As shown in Fig.

TABLE IV
COMPARISON BETWEEN THE PROPOSED TECHNOLOGY AND THE CONVENTIONAL ONES

Technology	[24]	[23]	[22]	[17]	[7]	Proposed
Number of MOSFET/GaN	4	8	4	6	8	4
ZVS range (including load condition and duty ratio)	wide	wide	wide	wide	very narrow	wide
MOSFETs voltage stress	v_{in}	v_{in}	v_{in}	v_{in}	v_{in}	$v_{in}/2$
Input voltage	100 V	40 V	40 V	210 V	150 V	250 V
Peak efficiency	93.7 %	91 %	85.7%	93.3%	84.1%	95.2%
Power level	N/A	16 W	40 W	1.05 kW	1 kW	400 W
Switching frequency	85k Hz	1 MHz	200 kHz	85 kHz	100/200 kHz	85 kHz
Voltage levels	Two	Two	Two	Two	Three	Three

19(a), two comparison values C_1 and C_2 together with a triangular carrier are used to generate the pulses S_1 and S_2. The DC-link voltage of the flying capacitor (u_c) needs to be measured for the voltage balance strategy. With the capacitor voltage balance strategy, suitable switching sequences and control signals can be found. While $u_c>0.5U_{dc}$, the switching sequence denoted as "00"-"01"-"11"-"01"-"00" is selected to discharge the capacitor. While $u_c<0.5U_{dc}$, the switching sequence denoted as "00"-"10"-"11"-"10"-"00" is selected to charge the capacitor. The switching sequences are changed by exchanging two comparison values (C_1 and C_2).

Fig. 19(b) shows the inverter output voltage and current, where u_{in} consists of two superimposed pulse-width of D_2T and D_1T. $0.5\geq D_2\geq 0$, $0.5\geq D_1\geq 0$, and $D_1\geq D_2$. While the fundamental components of the output voltage of the three-level inverter of the WPT system using SVPFM or PWM is the same, the relationship between δ_{SVPFM} and d_{pwm} can be derived as:

$$\delta_{SVPFM} = d_{pwm} = 0.5\left(\sin\left(D_1\pi\right)+\sin\left(D_2\pi\right)\right) \tag{38}$$

According to d_{pwm}, D_1 and D_2 are given as [7]

$$\left[D_1\ D_2\right]=\begin{cases}\left[0.5-\dfrac{1}{\pi}\cos^{-1}\left(2d_{pwm}\right)\right] & 0\leq d_{pwm}\leq\dfrac{\sqrt{3}}{4}\\ \left[\dfrac{2}{3}-\dfrac{1}{\pi}\cos^{-1}\left(\dfrac{2d_{pwm}}{\sqrt{3}}\right),\dfrac{1}{3}-\dfrac{1}{\pi}\cos^{-1}\left(\dfrac{2d_{pwm}}{\sqrt{3}}\right)\right] & \dfrac{\sqrt{3}}{4}\leq d_{pwm}\leq\dfrac{3}{4}\\ \left[\dfrac{1}{3}+\dfrac{1}{\pi}\cos^{-1}\left(\dfrac{2d_{pwm}}{\sqrt{3}}\right),\dfrac{1}{3}-\dfrac{1}{\pi}\cos^{-1}\left(\dfrac{2d_{pwm}}{\sqrt{3}}\right)\right] & \dfrac{3}{4}\leq d_{pwm}\leq\dfrac{\sqrt{3}}{2}\\ \left[\dfrac{1}{2}-\dfrac{1}{\pi}\cos^{-1}\left(\dfrac{2d_{pwm}}{\sqrt{3}}\right),\dfrac{1}{2}-\dfrac{1}{\pi}\cos^{-1}\left(\dfrac{2d_{pwm}}{\sqrt{3}}\right)\right] & \dfrac{\sqrt{3}}{2}\leq d_{pwm}\leq 1\end{cases} \tag{39}$$

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