Integrating operations research into very large-scale integrated circuits placement design: A review

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Abstract: In very large-scale integrated circuits (VLSI) physical design (PD), the placement stage specifies the arrangement and order of components within an area, and the effectiveness of the placement result will directly affect the chip's performance. With the advancement of process standard and the reduction in the feature size, the complexity of placement design has increased dramatically, and the realization of placement algorithms to deal with millions of components has become one of the important issues in the automation of integrated circuit electronic design. In this paper, we firstly segment the circuits into VLSI design styles, and review them from three aspects, practical placement problems, placement design ideas and placement optimization methods. In traditional circuits, the focus is on the essence of the placement problem, placement steps, placement algorithms, classification and other basic knowledge of the generalization. In modern circuit placement, the discussion focuses on the impact of technical constraints on design. After identifying the essence of the placement problem, solutions to the packing problem are reviewed, which in turn summarizes representative placement algorithms. Finally, based on the development of VLSI placement design, the optimization bottlenecks of existing placement design are summarized, and suggestions for future research are made based on the latest research topics and methodologies.

Keywords: VLSI placement, placement design, mixed-cell-height, operational optimization

1. Introduction

Since its debut in 1965, Moore's Law has been used as a development goal followed by industry and academia (Wang *et al.*, 2023a). However, as time passes and technology advances, chip development is no longer solely dependent on transistor count; heat dissipation and power are other factors to be considered (Wang *et al.*, 2023b). Product design in the post-Moore era will be more diverse, with shrinking critical dimensions and process windows, and a model where process and design are independent of each other, all requiring the chip design process to follow process rules. The process alone to achieve feature size reduction and further enhancement of chip performance has become more and more difficult in response to the market's demand for constant improvement of chip performance,

and the traditional design process is no longer able to meet the demands of modern circuits. Innovative solutions are urgently needed for the technological problems that the physical design (PD) of very large-scale integrated circuits (VLSI) cannot be handled properly at present.

Compared with analog circuits, digital circuits are more automated (Yu *et al.*, 2010), and therefore require a lot of complex tools to develop them. Algorithms for chip design can also compile digital circuit designs, which is a very sophisticated process. Thus, this paper attempts to synthesize the prior research on placement design based on digital circuits, provides a summary of the new process and design rule constraints, and gives the future research direction. In the circuit design process of VLSI, the pre-process steps' level of abstraction is high, whereas the abstraction level of the post-process steps is gradually reduced. As shown in Figure 1, PD is located in the middle of the overall design flow, it is the key to bringing the design concept to fruition. placement, which determines the coordinates of the location of all components based on the netlist information from the preceding processes to minimize the wire length and efficacy of the circuit, is the most challenging part of physical design.

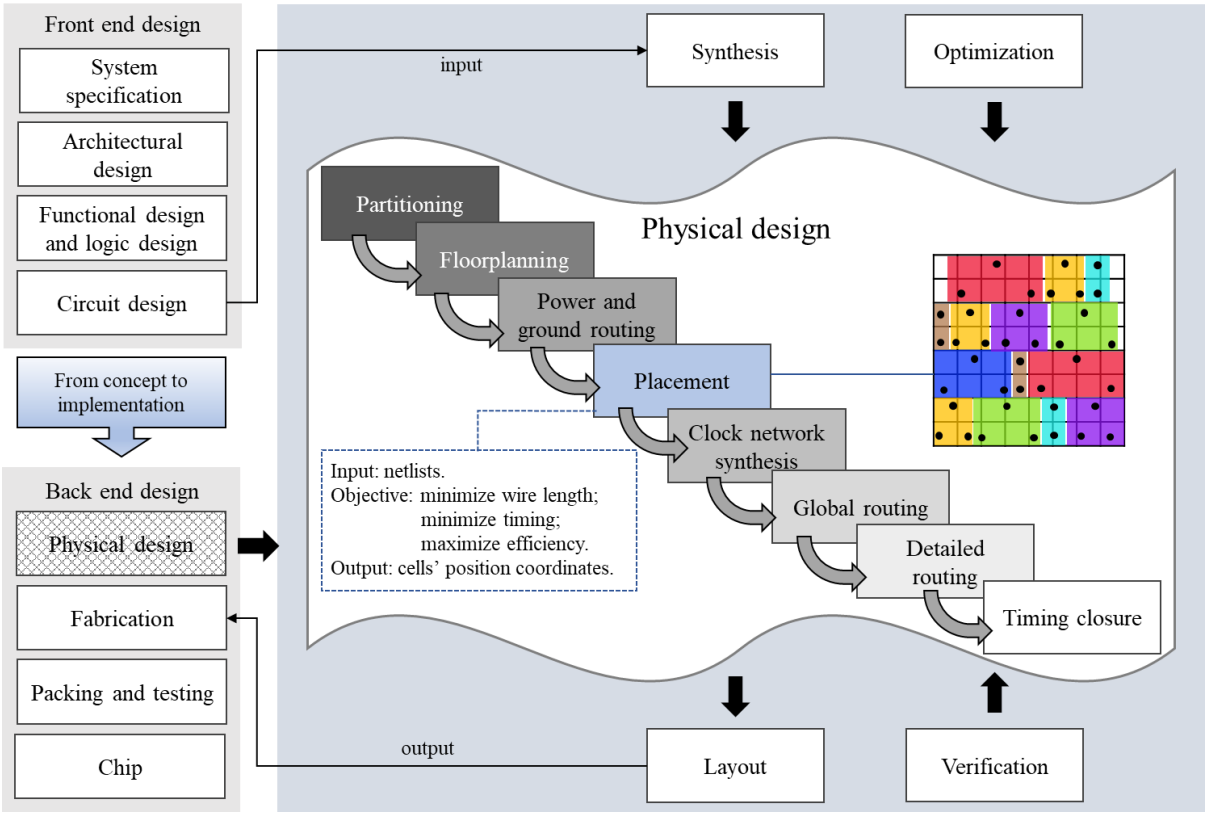

Figure 1: VLSI circuit design flow

In the PD process, all design elements become reality in their geometrical form. In other words, all components including macro cells, standard cells, logic cells etc. There is a designated placement area in the fabrication layer, and the arrangement of these components with fixed shapes and sizes compiles

with the routing conditions in the metal layer. PD is an iterative optimization process that results in a set of instances to be subsequently verified. The performance, size, and power of the circuit are three practical elements that PD directly influences, and the design principles are complicated. Because of this, PD is usually studied by dividing it into some key steps, including partitioning, floor-planning, power and ground routing, placement, clock network synthesis, global routing, detailed routing and timing closure (Farghadan *et al.*, 2017).

The circuit can be divided into more manageable parts by cutting horizontally and vertically, that is, the area is relatively small bins. Organizing the placement of bins and pins, and attempting to pinpoint the precise locations of standard and logic cells within the bins, placement is undoubtedly one of the most crucial phases in PD. VLSI PD automation greatly benefits from the multi-objective optimization problem of placement. In the following stages of grid design, clock tree synthesis, grid optimization, power optimization, global and detailed routing, post-placement simulation, and design variability, placement performance serves a significant role (Zhu *et al.*, 2018b). Additionally, several additional criteria and constraints, including as timing and power, have emerged as a result of modern sophisticated circuit design. Because the placement problem is NP-hard and has a large computing scale, research on VLSI placement design has been unable to find an exact optimal solution. In conclusion, it is vital to provide an efficient, precise, and reliable placement algorithm to optimize the placement problem for contemporary circuit designs which include millions of bins.

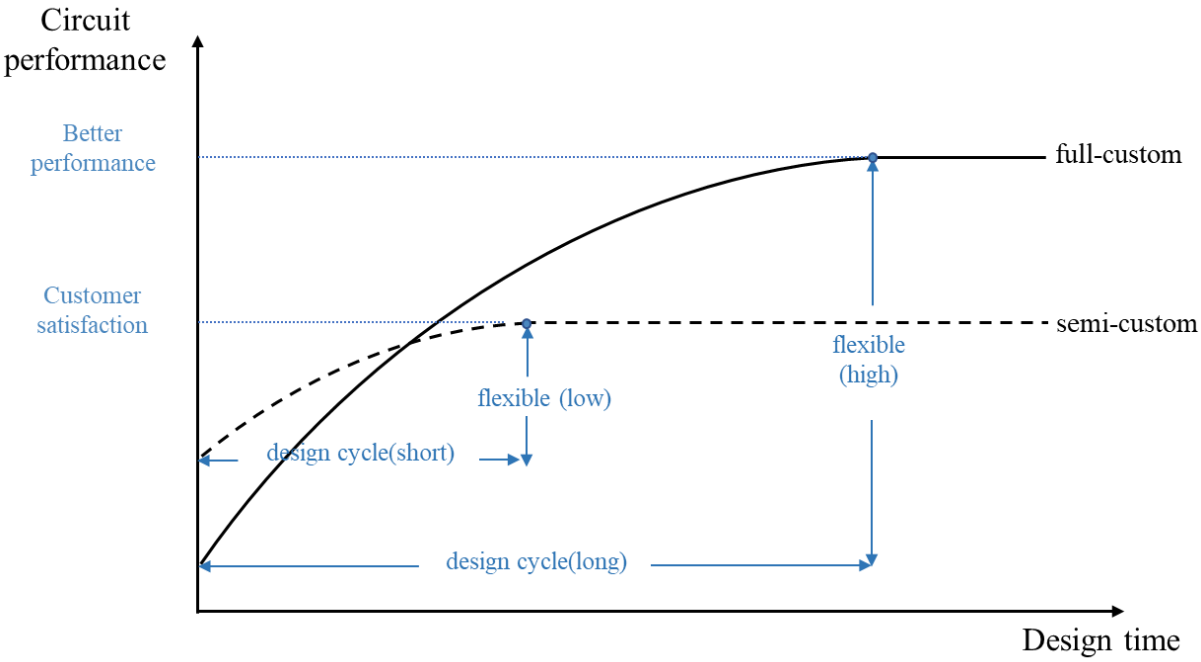

Figure 2: Two design styles of VLSI

Choosing the appropriate design style is crucial since it affects time costs. The two primary VLSI design techniques are full-custom and semi-custom, respectively. Figure 2 lists the features of two design styles, with full-custom allowing more flexibility for performance optimization improvement and semi-custom offering a shorter cycle time for design development. Integrated circuit implementation is shown in Figure 3, and semi-custom can be further divided according to different design perspectives. Both full-custom and semi-custom styles are appropriate for the design of application-specific integrated circuits (ASICs). Field-programmable gate arrays (FPGAs) are designed using a semi-custom approach that spreads out the high cost of a flexible design across multiple batch yields. ASICs are designed in response to specific user or system requirements, whereas FPGAs do not require user intervention in terms of chip placement and process issues. FPGA has the definite advantage of dramatically decreasing design cost and time-to-market within a certain yield (Kuno *et al.*, 2007), even though it operates more slowly and uses more power than ASIC (Chen *et al.*, 2020). For high-usage designs, clock routing capabilities are frequently limited, and extra clock limitations make placement more difficult (Boutros *et al.*, 2018).

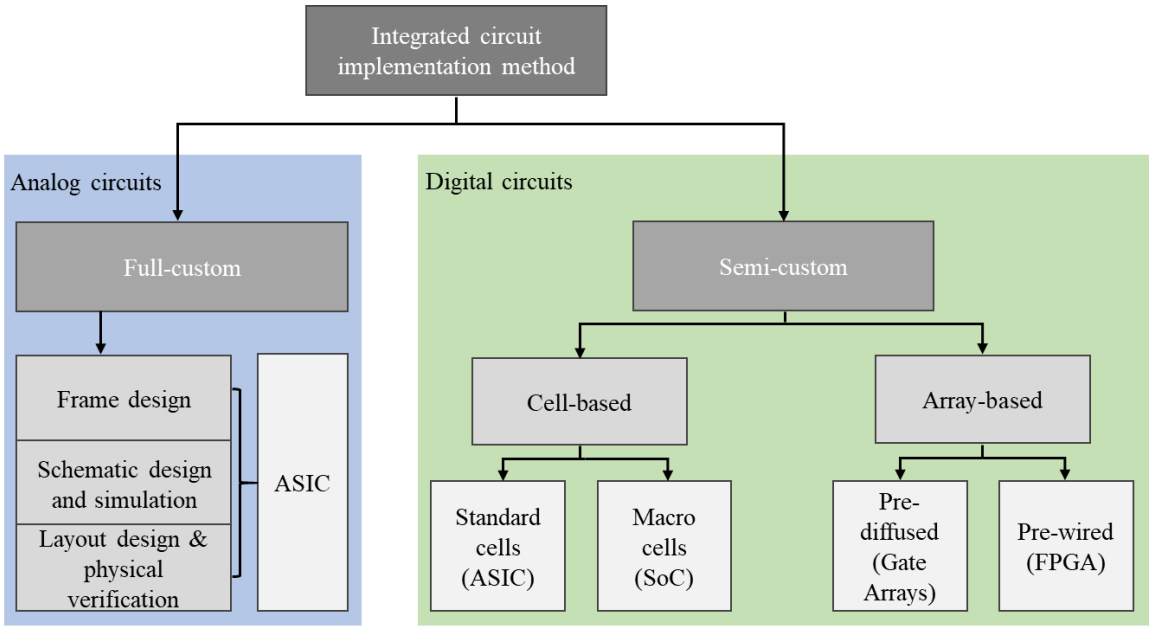

Figure 3: Integrated circuit implementation method

From the array point of view, prefabricated transistors or wires are integrated into arrays, and then the design of related functions can be accomplished by changing the connection method of transistors or wires at the time of use. Gate array as a master based on pre-fabricated transistor arrays, the designer only needs to design the metallization interconnections between the tubes and the necessary through holes and contact holes according to the functional requirements of each circuit. Gate Array as a master batch based on pre-fabricated transistor arrays (Wang *et al.*, 2015b), the designer just needs to design

the metallization interconnections between the tubes and the necessary vias according to the functional requirements of each circuit. To fulfill the design requirements of emerging circuits, many current studies suggest complicated clock topologies based on the characteristics of FPGA logic blocks and propose clock-aware placement techniques to improve circuit integration and thus achieve high performance.

Li *et al*. (2018b) optimize the routing length and routable rows based on the clock constraints and propose the high-performance FPGA placer, UTPlaceF 2.0, which iteratively allocates components by minimizing the cost flow. Failing to take into account clock feasibility might result in routing failure due to the time-based network's non-adjustable physical structure and its limited routing resources. A generic FPGA placement framework is put out by Li *et al.* (2019a) that explicitly constructs a clock tree to verify clock feasibility while simultaneously optimizing placement quality. According to Chen *et al.* (2020), an efficient timing-aware placement strategy for massive heterogeneity FPGAs has been carried out to address the issue of peculiar FPGA clock architecture. To simultaneously enhance the maximum possible relaxation and clock restrictions of heterogeneity FPGAs, Lin *et al.* (2021) propose a resolution placement approach. Zhu *et al.* (2022) develop a connection-aware and type-balanced clustering technique for the issue of massive heterogeneity FPGAs with clock limits, enabling the legality of the configurable logic block (CLB) in FPGAs.

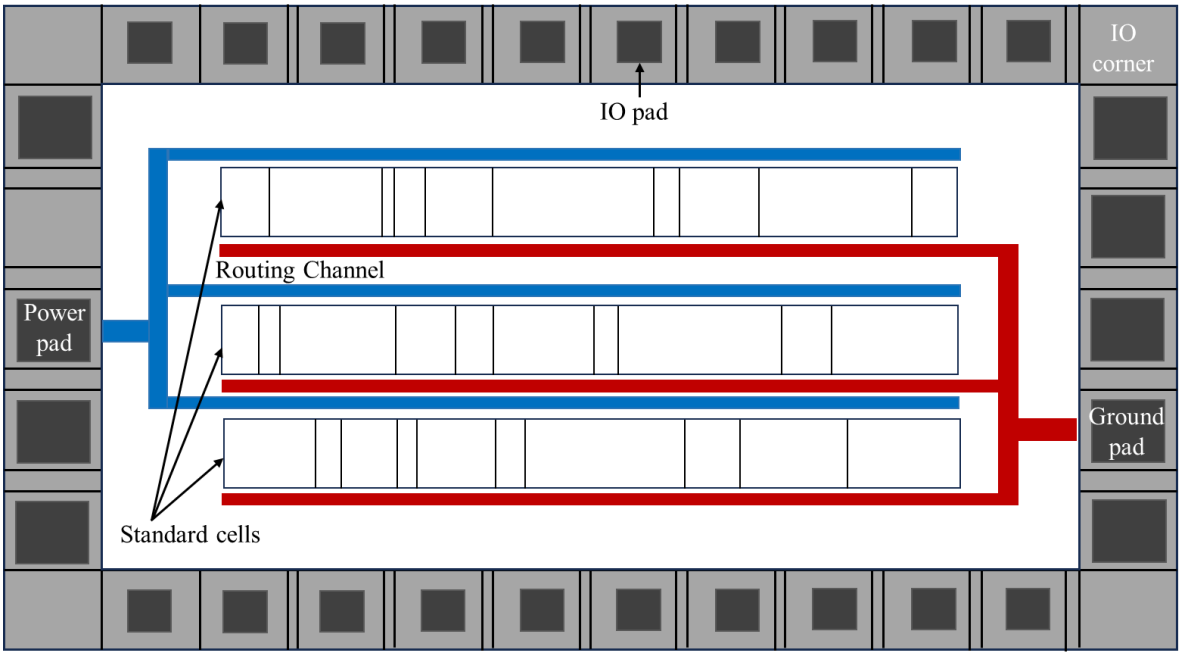

Figure 4: An instance of standard cell

In a cell-based circuit implementation, the function is seen as a standard cell and is designed using the mature standard cell connection. As shown in Figure 4, a standard cell in digital circuits is a

predefined component with a fixed size and function, whose height is designed to be multiples of the fixed cell elevation, and the width of it varies with the complexity of the function. Designs based on standard cells, such as ASICs, are less complex because there are fewer degrees of flexibility for standard cell placement. The time to market is shortened compared to full-custom, but metrics like power, placement density, or frequency of operation are sacrificed. Standard cells are constrained by their shape, whereas macro cells are not. Larger logical blocks called macro cells frequently carry out reusable tasks. Macro cells tend to be placed throughout the placement region to improve electrical properties or wiring distances. Taking the system-on-chip (SoC) placement in Figure 5 as an example, different versions have macro cells of different sizes distributed in various corners of the chip.

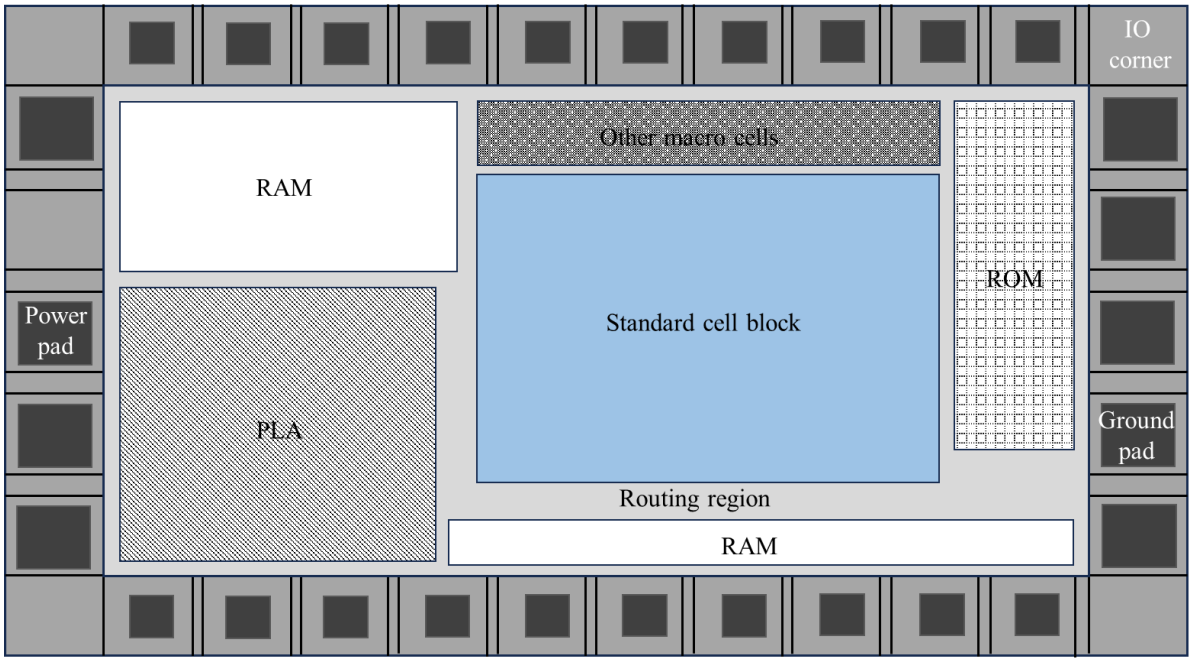

Figure 5: An instance of macro cell

VLSI can be implemented in a variety of ways through full-custom, standard cells, macro cells, gate arrays, and FPGAs. These options must be compared based on performance, cycle, economy, flexibility, and other requirements. For VLSI, standard cells and macro cells are currently the main implementation methods, except for full-custom within the cell. The design principle of an FPGA can be used if it prioritizes cycle and uses flexibility over performance and power consumption. In this study, we concentrate on standard cell placement design, transforming chip placement design problems into bin packing problems (BPP), presenting placement rules in the form of geometric constraints, and designing solutions from the perspective of operations optimization.

Single-row height and multi-row height are the two categories into which standard cells can be divided. Modern circuits utilize mixed-cell-height placements in order to improve performance as

opposed to traditional circuits, which solely take into consideration single-row-height cells. Under the evolving placement technique, which offers a new path for the creation of modern circuits, minimum-implant-area (MIA) limitations are a critical constraint. We present a thorough review of the placement progress in modern circuits and the effects of MIA restrictions, as well as a discussion of the fundamental requirements for traditional circuits from the perspective of standard cell placement.

The remainder of this essay is divided into subsequent sections. Section 2 introduces the single-row-height standard cell placement concept. After a thorough examination of the mixed-cell-height placement design without MIA constraints in Section 3, Section 4 provides a description of the design with MIA constraints. In Section 5, challenges and future works are organized for this optimization problem. This paper is concluded in Section 6.

2. Single-row-height standard cell placement design

2.1 Traditional circuit design

Placement in PD is a complicated optimization issue with multiple goals aimed at improving the performance and reliability of a circuit, among other metrics. The degree of alignment between the optimization objective and the actual PD determines the quality of the placement. It can be challenging to include various optimization objectives into an algorithm and objectives conflict with each other. The trade-offs between several aims, however, are typically well-represented by an objective function. The placement, in its essence, is the issue of arranging cells that must be suitably laid out in the given area in accordance with specific technical limitations and requirements, assuming that the position and shape of the cells to be placed, as well as the information regarding the placement space, are known.

Standard cells in traditional circuits are uniformly sized to facilitate design and optimization (Wang *et al.*, 2004). Three categories of constraints must be satisfied during placement optimization: technical constraints, electrical constraints, and aggregate constraints. Technical constraints enable the manufacture of technology-specific nodes. Electrical constraints guarantee the required electrical performance in the design, while geometric constraints are included to lessen the design's overall complexity.

Traditional circuit design models summarize some fundamental considerations for placement applied to traditional circuits. This model can be constructed by hypergraph with a set of cells and nets. The height and width of the placement area and cells need to be laid out. Taking the coordinates of the lower-left corner of the cell, setting the cell position after global placement, and the cell position after legalization. The objective function can minimize all cell displacements during the legalization process.

Constraints require cells must be situated in the planning area; cells must not overlap with each other, and the necessary power must be applied to the right cell.

Placement problems in traditional circuits are essentially one-dimensional BPP (Chen *et al.*, 2012a), both of which require that target components of the same size be packed into containers with a certain fixed area. Because of the introduction of multiple design rules, the process of placement is significantly more intricate than one-dimensional BPP. As a Knapsack Problem version, BPP is a combinatorial NP-hard problem, whose decisions are complete (Kucukyilmaz *et al.*, 2018; Pereira *et al.*, 2016). With the development of science and computational tools, the research on BPP has formed a system. In the classical one-dimensional BPP, due to the existence of boxes with the same capacity of the assumption, hence, the majority of algorithms are built using the following methodology: first of all, the packing order of the goods is sorted, and then according to the capacity of the box limitations in accordance with the order of the box. The algorithms designed on the basis of the above ideas are collectively referred to as the Fit algorithm (Balogh *et al.*, 2021).

The exact algorithms represented by branch-and-cut-and-price (Alves *et al.*, 2005), column generation (Alves *et al.*, 2006), and heuristic algorithms (López *et al.*, 2014; Crainic *et al.*, 2011; Haouari *et al.*, 2009) improved according to the task increasingly popular as BPP research progresses. It would be worthwhile to investigate how placement design can be solved using mature BPP methodologies.

In practice, cell placement involves considerably more than just aligning cells such that they do not overlap at their respective places. When specifications like pin shorts, and pin accesses are included, the placement problem becomes significantly more challenging. For traditional circuit placement design, Kennings *et al.* (2014) suggest a more cautious legalizing strategy to prevent meticulous routing from negatively affecting the final placement quality. Typically, the single-row-height standard cell that legalizes the technique is combined with restrictions on the fence region. Previous research had less considered the feasibility of this problem through various approaches. Through the use of three approaches, Huang *et al.* (2015) suggest an analytical standard cell placement method to optimize routability. Tetris (Dadaliaris *et al.*, 2016) and Abacus (Puget *et al.*, 2015) are the two most popular algorithms for proving the correctness of traditional single-row-height standard cells. In order to implement placement legalization, Wang *et al.* (2015a) used Abacus to first build a placement framework, then take into account global and detailed routing congestion, based on a location migration strategy, and finally form an entire solution. The development of the Abacus approach was further explained by Darav *et al.* (2016), who concentrated on resolving the deliverability, target density, and fence region constraints. By combining a clustering algorithm, a two-round quadratic placement, and a

dynamic penalty increment strategy to update the wire length and density model, Huang *et al.* (2017) improved upon the Abacus method, thus achieving global placement and legalization in the context of satisfying technical and regional constraints.

2.2 Placement design step

Placement techniques for large-scale circuits typically involve three main stages, which are global placement, legalization, and detailed placement (Kahng *et al.*, 2011). The shape and size of the placeable components are typically disregarded in global placement, and no effort is made to line up their location with legal grid rows and columns. Since the focus is on global placement and general dense dispersion, some overlaps between the components being laid out are permitted. Global placement's goal is to reduce the target cost by locating each cell in its most advantageous location while maintaining placement restrictions, such as density. The legalization process will take place before or during the detailed placement. While seeking to minimize displacement from global deployment places, the influence on connectors in length and circuit delay, it aims to align placeable components using vertical and horizontal lines and eliminate overlaps. Each standard cell in a detailed placement is gradually moved into a better place by employing regional techniques to move a few things in a row or switching two components to make room for another. As the runtimes of global and detailed placement are frequently comparable, it seems that global placement typically demands more memory and is more challenging to parallelize. The global placement, as the first step in the formulation of the scheme, plays a role equivalent to that of the initial solution, which has a greater impact on the sequential operations. According to Zhu *et al.* (2018b), the global placement generally has a significant impact on the effectiveness and quality of the placement system. This is due to the positioning issue is prone to fall into local optimums during the solution process.

As the complexity of the design increases, with just these three phases, the location design challenge cannot be fully resolved. Existing research has refined the placement flow into six steps (Liang *et al.*, 2021). Figure 6 shows an initial chip planning stage before global placement, followed by two steps of cell spreading and resource demand after global placement and before legalization. For initial chip planning, the entire circuit is first divided into several sizable bins. These large bins of circuits are then assigned relative positions, correlations between them are examined, the processing order is arranged, and finally, they are given to the subsequent optimization algorithm to produce an initial placement result. The components will disperse from the area where resources are scarce to other areas depending on the space requirements and the accessibility of that location at the time of placement. This prevents an excessive density of components on the placement, which is the process of spreading. By changing

the space requirements of some standard cells, and the area availability of some areas, depending on parameters like stacking capability and cabling congested degree, the placement area correction step is required to improve the placement quality. By matching the iterative algorithmic solution with the placement iteration and developing rules to further optimize results based on legality, optimization algorithms can be applied in the iteration process, packing, and detailed placement stage.

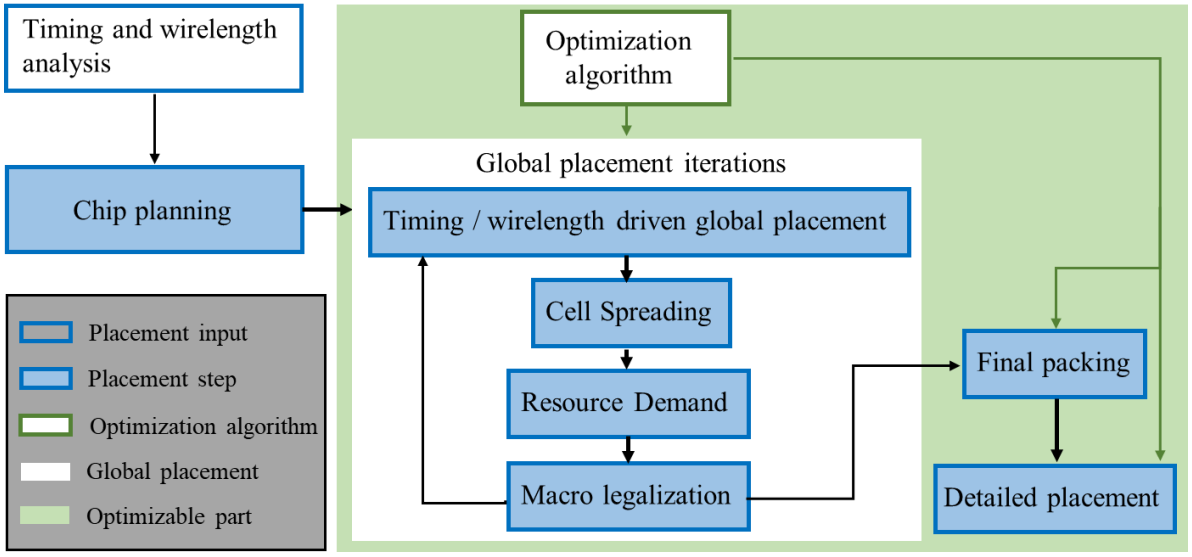

Figure 6: Placement design step

Actually, the real design process is far more complex than the steps mentioned above. Today's research focuses on placement design algorithms to achieve placement optimization, using optimization algorithms to iteratively design, modify, and validate the work in conjunction with the factory's manufacturing process.

2.3 Placement design algorithm

Three broad categories can be used to classify current placement methods: min-cut partitioning (Chow *et al.*, 2016b), simulated annealing (Chang *et al.*, 2009), and analytical formulation (Markov *et al.*, 2015). Eliminating cell overlap is a crucial strategy in the placement based on the analytical formulation method. Specific implementations of this method include frequency control and Poisson density control (Lu *et al.*, 2014; Hu *et al.*, 2009).

Recently, it has been demonstrated that placement schemes based on analytical formulation methods approach to produce the highest quality outcomes by virtue of their good scalability (Hsu *et al.*, 2010). The placement challenge is modeled analytically as a mathematical planning model with a function that is objective and an array of restrictions. Various approaches to optimization are used to address the issue. Both of the most popular analytical formulation techniques are quadratic and nonlinear displacement.

Due to the quadratic model's and the solution process's simplicity, the quadratic placement method is essentially more successful. The nonlinear placement method is superior in terms of solution quality because the model is more accurate and represents reality more closely (Hsu *et al.*, 2013).

Despite the fact that both solution efficiency and quality are critical metrics for evaluating a method, the majority of academics adopt a nonlinear strategy to address the problem in VLSI placement design. In order to save runtime when dealing with nonlinear optimization issues, a multilayer framework is typically used. The quadratic penalty approach, the Lagrange multiplier method, and the enhanced Lagrangian method are a few typical ways in the nonlinear placement process. (Guo *et al.*, 2021). By lowering the goal function's density requirement and altering the penalty parameter to control the density of components, the quadratic penalty method typically finds a solution to the minimization problem. However, since the density cost contributes too little to the overall goal cost, the solution process may fall into a local optimum (Kim *et al.*, 2012), resulting in poor placement quality. In contrast, since the multiplier value is variable, the Lagrange multiplier method is more capable of avoiding local optimums but is slower. Because of its remarkable performance in imprecise search environments, the augmented Lagrangian approach is frequently supplemented with other techniques to increase solution accuracy and speed.

By balancing the wirelength objective and density restrictions through dynamic density weights and adopting adaptive line lengths, Zhu *et al.* (2014) develop the generalized Lagrangian technique to handle the global placement problem and produced a superior placement within a time validity period. Lu *et al.* (2015) propose a placement strategy that utilizes electricity named ePlace-MS for VLSI. algorithm. The algorithm uses a backtracking method to optimize the topological differences between different types of cells, and references the idea of simulated annealing to legitimize the multi-stage placement. Zhu *et al.* (2018b) use the quadratic penalty technique with the generalized augmented Lagrangian approach to solve the VLSI globally placing issue, demonstrating the global convergence property. y, which can be applied to additional large-scale nonlinear optimization problems.

For the placement design of traditional circuits, many studies have contributed in exploring single-row-height cell arrangement. Kahng *et al.* (1999) and Brenner *et al.* (2000) both aim to minimize the total weighted wiring length by laying out cells in a fixed cell order. Kahng *et al.* (2004) go on to evaluate several row-based placement techniques to improve the cell overlap problem and standardize the placement method to enhance the routability and wiring length metrics. Gupta *et al.* (2005) dealt with standard cell placement using dynamic planning techniques in detailed placement to optimize the placement order of cells in the same group. Karimpour *et al.* (2017) suggested a flow-based placement method with the aim of limiting the great possible cell dislocation in the legalization phase with the

goal to decrease the largest cell motion for single-row-height standard cell legality. The key of this algorithm lies in the finding of critical paths, and the idea of pruning is used to find the legal paths between cells.

The arrangement placement of a single row-height standard cell is relatively simple because there are only constraints on the cells within the rows, but if the problem is extended to the placement design on a multi-row-height cell, the cells between those rows are no longer independent of each other (Baek *et al.*, 2008), and it is necessary to consider the coupling effect between them, which makes the difficulty of such a problem unsolvable by the single-row-height placement design method (Brenner *et al.*, 2013).

3. Non-MIA constraints mixed-cell-height placement design

3.1 Modern circuit designs

The application mode of uniform standard cells of the same height in traditional circuits can no longer satisfy design criteria due to the development of emerging chip design technologies. Modern circuits are therefore more complex to design since they need standard cells with mixed-cell height based on factors including area, power, and operating speed (Chen *et al.*, 2021). Shorter cells require less space as well as energy yet have lower driving velocity and strength, and also less pin availability and routability; taller cells, have stronger drive strength and speed, as well as higher pin accessibility and routability, but they also require more space and power. Simple standard cells are made of single rows of height, whereas complex standard cells are made of several rows of height (Baek *et al.*, 2008). Mixed-cell-height standard cell mode is now often used in modern circuit placement design to address the circuitry's increasing complexity.

Electrical effects have become more significant as the technology scales further. As a result, numerous researchers have introduced a variety of electrical limitations to guarantee the accuracy of the circuit. For modern designs, many constraints that were unnecessary at earlier technology nodes have become crucial as they may restrict connection impedance. To maintain signal truthfulness, and stop electrical migration impacts in interconnectors, while avoiding associated occurrences such as abnormal temperatures, modern circuits require more comprehensive design solutions.

One of the most fundamental challenges for modern circuits is the inability of new electrical effects to convert into new geometric principles that can affect placement design. For example, signal delay cannot be chosen whether to minimize the result by reducing the wire length bus or by decreasing the connection capacitor between different nets. Paths on other metal levels make the issue even more challenging and switching activities also affect the signal delay. Even though the electrical limitations

can only be described by relaxed geometric rules, effectively extracting the electrical characteristics from the architecture still enables physical simulations to derive metrics like estimation time, noise, and power, allowing them to evaluate the effectiveness of placement optimization.

For multi-row height standard cells, the legality and precise positioning issues are extremely challenging, because heterogeneous cell structures increase global cell interference, necessitate larger solution spaces, and impose additional constraint limitations like the power rail constraint (Wang *et al.*, 2017). In response to sophisticated power, location, routability, and efficiency trade-offs, mixed-cell-height circuits have gained popularity as a technology. The mixed-cell-height legalizing problem is fundamentally a strip packing problem, according to Chen *et al.*'s (2012a) description, it is NP-hard in general. In addition to the basic constraints involved in traditional circuits, must consider more intricate design guidelines and limitations, such as fence region constraints, etc. Failing to account for these constraints in the placement design will result in illegal placement schemes or even serious violations. Because resolving these issues in the post-processing stage will take a lot of time, it is best to take a variety of constraints into consideration at the design stage.

Modern circuit placement design without MIA influence adopts the same hypergraph modeling idea as the traditional one. These basic rules reflect the complexity of mixed-cell-height. Because of the diversity of cell heights, the cells are categorized when performing virtual device driver (VDD) or voltage source sink (VSS) calibration. Placement should ensure the orbital alignment of odd-row-height cells, even-row-height cells, and 6TPPNN cells, respectively. Fence region constraints that prevent overlap between cells and others in the same or different layers.

Placement algorithms for mixed-cell-height circuits should be designed to optimize the placement impact or efficiency as much as possible, satisfying the considered design rules while selecting the objective to achieve the maximum or minimum optimization. Additionally, overlaps between cells should be eliminated as much as possible. It is worth noting that the placement algorithm should be quick to solve, robust, and applicable to large-scale cells, due to the special characteristics of VLSI.

3.2 Special mixed-cell type

Undoubtedly, mixed-cell-height circuits involve the placement design with cells of various heights. The earlier discussion of shorter and higher cells was only based on the fuzzy classification of their efficacy. Hybrid cells can be carefully detailed into several categories. According to their absolute and relative heights, cells can be separated into even or odd-row-height cells as well as single or multiple types (Wu *et al.*, 2016); they can also be divided into even-row-height and odd-row-height cells based on the relative height. The following content of this section will go into detail about the use of special

cells in modern circuit design, the specific placement rules will be elaborated in the next paragraph.

Modern circuit design is growing more and more complex. cells with a combination of single and multiple-row height alone cannot be successfully handled in the face of some challenges (Wu *et al.*, 2016), thus 6T and 6TPPNN cells are also popular in modern circuit design (Lin *et al.*, 2011). Whether it is a single or multiple-row-height cell, its wiring is located on the upper and lower side boundaries of itself. The wiring of the 6TPPNN cell is located in the interior of the cell, which can satisfy the special needs of some circuits. Additionally, it realizes the trade-offs between routing rows, time, and other metrics and performances. However, this also puts forward a higher requirement in the design.

Mixed-cell-height circuits consisting of 6T and 6TPPNN cells are designed to obtain stronger driving power and improve area utilization. The definition of "6T cells" mentioned here serves as a generic name for cells ranging in height. The application of the complex 6TPPNN cell strengthens the driving power of the crucial path in the placement. Although the height of a 6TPPNN cell is only twice that of the cell's row, it can achieve driving strength that is equivalent to three times that of the unit's row, ensuring that driving while also utilizing less space, increasing the placement's effectiveness. It is inevitable that the fragmentation effect (FE) will have an impact on the application due to the unique properties of the 6TPPNN unit structure. If the FE cannot be eliminated, the 6TPPNN cell will not be able to achieve the desired level of efficiency and thus lose its advantages in placement design. Therefore, in the process of legalization, extra attention should be paid to the issue of rail alignment to ensure the correct alignment of cells and pins (Chen *et al.*, 2012b). Since circuits are usually designed with a combination of drive and leakage power in consideration of the effectiveness aspect, 6T and 6TPPNN hybrid circuits are generally combined with multi-threshold voltages (VTs) to balance time and power (Yang *et al.*, 2019; Tseng *et al.*, 2016).

Due to the limitation of technology protection and data, there are fewer studies on 6T and 6TPPNN cells, and the study of Zhu *et al.* (2020) is more representative. They consider the legalization of the hybrid 6T and 6TPPNN cells under the minimum width (MW) and the FE constraints. Firstly, a global placement result conforming to the VDD and VSS constraints is given based on the rail alignment requirement, then a clustering-based solution method is proposed to eliminate all MW violations, the issue of legalization problem with MW restrictions is formulated as a quadratic programming (QP) problem, and finally, the mathematical model is solved efficiently by using a modulus-based matrix splitting iteration method (MMSIM). Yang *et al.* (2019) first proposed a technique to solve the MIA and FE constraints for hybrid circuits with 6T and 6TPPNN. The MIA constraints are determined by a clustering algorithm, then the optimal region of wirelength for each cluster is determined, and the FE is mitigated by transforming the 6TPPNN cell clustering. Although above studies eliminated all MW

violations in the mixed cell circuit consisting of all 6T and 6TPPNN cells, they did not completely eliminate the FE, but only mitigated the effect to a certain extent, so the optimization of the effect of the FE on the placement can be continued in the future based on this study.

3.3 Placement technical constraints

The VDD and VSS lines in a standard cell design are spaced apart between rows in the placement area, and each cell needs to be set up so that the pins of the power and ground lines are aligned to the proper row in order for the cell to operate as it should (Wu *et al.*, 2018; Chen *et al.*, 2022c). Alignment for cells with odd row heights (such as cells with one or three rows) can be done either straight away or by rotating the vertically reversed cells (Dobre *et al.*, 2023). The placement conditions are stricter for cells with even row heights, which can't be altered out of legality, such as cells with a two or four-row height (Chen *et al.*, 2012b).

The mixed-cell-height standard cell legality issue with power rail alignment is shown in Figure 7. As indicated earlier, cells A and C with odd row heights can be directly positioned on the proper VDD/VSS power rails or flipped to any row (Karimullah *et al.*, 2022). In contrast, even row-height cell B has to link its bottom and top pins to the same type of power rails and cannot be accomplished with the correct rails in arbitrary rows (Lin *et al.*, 2022). It is forbidden to align Cell B's bottom border with the VDD line because it is built for the VSS, and flipping the cell will not fix this wiring issue with the power rails (Kahng *et al.*, 2022; Hao *et al.*, 2022). For 6TPPNN cell D, this question is transformed into making sure that the VDD/VSS pins inside the unit match the corresponding line.

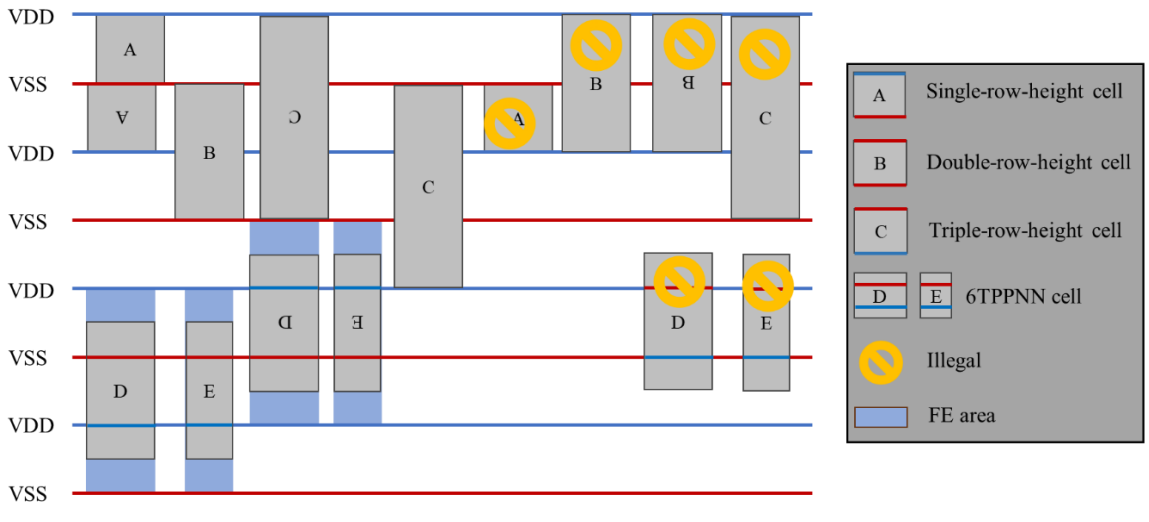

Figure 7: Basic placement rule of standard cells

The 6TPPNN cell has a significant placement design issue as a result of th+++ e complex FE. As shown in Figure 7, the 6TPPNN cells D and E are placed according to the rail alignment rule, and the

blue area represents the influence of the FE. Although FE itself is not in conflict with other constraints, FE cannot be ignored. If FE is not taken into account it may result in a large amount of dead space, which would increase area overhead and decrease chip performance. There are typically two approaches to eliminate FE: one is to directly insert fillers near individual 6TPPNN cells; the other is to first cluster 6TPPNN cells and then place clusters at the expected locations. The first method eliminates the FE but also enlarges the area of the 6TPPNN cells; the second one does not incur additional area overhead, so it is a better choice.

3.4 Placement design algorithm

Although there are more sophisticated solutions to the placement design problem for single-row height cells, still, current research shows earlier approaches are insufficient for resolving the multi-row height cell problem (Li *et al.*, 2018a). Due to the uniform cell height, only the scenario of overlapping cells within a row is required to be handled during the research of single-row high cells. Overlapping cells between rows with cells is a distinct problem. Relocating a cell in a particular row can lead it to overlap with cells in a different row, hence inter-row overlap and intra-row overlap must be considered simultaneously for the multi-row height cell legality topic. Selecting appropriate locations for both single and multi-row height cells simultaneously prove challenging when reviewing the mixed-cell-height issue, and the existing literature concentrates mostly on improving the algorithm to address the issue.

For the detailed placement problem with a mixture of single and double-row size cells, Wu *et al.* (2016) combine the shorter cells into taller ones by pairing them. The idea of the conventional detailed placement method is expanded as a result, turning the mixed-cell-height placement problem into a single-cell-height positioning issue. Although the above study involved the mixed-cell-height placement problem, it did not take into account the condition of power-rail alignment.

The power-rail alignment condition is viewed as a fundamental element in many traditional circuit design studies. According to Chow *et al.* (2016b), the legalization and detailed placement problems were taken into consideration. They combined the power track matching condition based on global placement to solve the legalization difficulty and reduce the cell moving distance, they took into consideration the overlap restriction to design the local area legalization algorithm for detailed placement. The algorithm can swiftly determine the unit ranking position, but the solution quality is general and global legalization cannot be guaranteed. Wang *et al.* (2017) develop an algorithm applicable to hybrid height standard unit legalization based on Abacus, fix the issue with dead spaces, and derive the corresponding objective function to optimize the design plan. This work emphasizes the

value of initial cell ordering.

Power-rail alignment conditions are just one of the numerous placement restrictions that the modern circuit design must adhere to. To achieve significant placement outcomes, Lin *et al.* (2017) offer an innovative density-based precise placement technique on diversely shaped netlists based on Chow *et al.* (2016a). This placer optimizes single and multi-row-height cell placement in an identical stage. Based on the multi-row local legalization algorithm in Chow *et al.* (2016a), Li *et al.* (2018a) legalizing technique that uses mixed-cell-height, taking into account fence region, employing a window-based implantation strategy including several afterward networking flow-based improvements. To ensure global placement efficacy, Chen *et al.* (2017) first determine cell placement order and then implement a linear transformation of the problem through the release boundary constraint, and this algorithm can quickly obtain a high-quality solution that approximates the ideal case. Based on Chen *et al*.'s algorithm, Zhu *et al.* (2018c) offer an aware-based strategy to solve for uniform cell assignment and placement legitimization while taking into account technical and regional constraints. With the development of chip strategies and solution approaches, research on VLSI mixed-cell-height continues.

In addition to legalizing the offending cells one by one, the idea of parallel legalization can also be used to improve the placement quality. Hung *et al.* (2017) divide the placement area evenly and then adjust the cell density of each sub-region to obtain a high-quality placement scheme by minimizing the total cell displacement distance and utilizing the integer linear programming (ILP) model, but this method does not have an advantage as a matter of execution time. The above research on the legalization of mixed-cell-height circuits starts from a perspective that optimizes wiring length and obtains a placement scheme by designing algorithms with different ideas. Due to the large scale and high-efficiency nature of mixed-cell-height circuits, the existing methods are still on the path of pursuing fewer technical violations. However, they do not achieve zero violations in the true sense of the word. Liang *et al.* (2023) proposes a new cell-based design paradigm, which can effectively solve the placement legalization problem of mixed row height designs. This method incorporates a cell version change mechanism in the legalization process by taking advantage of the existence of numerous copies of the same cell with different heights and widths. The experimental results show that the placement scheme obtained by this method does not have illegal cells.

The above research focuses the optimization objective on overall cell relocation, which happens to be an especially common operation in a study of mixed-cell height legalization. However, cells placement can be further optimized from timing, power, etc. Chen *et al.* (2022b) consider both the variation in the proportion of supply nodes compared with drain sites and the overall cells relocation, and integrate them with the modern circuit. The new challenges regarding the drain-to-drain abutment

(DDA) and fence region are applied to the Robust Modulus-based Matrix Splitting Iteration Method (RMMSIM) and ILP methodology for gradually determining the cell locations in the order of broad assignment, legality, and specific distribution. This approach has a higher cell legalizing rate than the shortest path method and determines the locations of the cells. Li *et al.* (2019b) represent the mixed-cell-height placement problem as Mixed Integer Quadratic Programming (MIQP) by relaxing the discrete constraints to linear constraints, thus realizing the model conversion from MIQP to QP, followed by solving the Linear Complementarity Problem (LCP) using the MMSIM method.

Due to the complexity of the placement criteria, it is exceedingly challenging to obtain the cell placement results straight from commercial solvers. Thus, some of the current studies, which transform the original problem into a convex quadratic programming (QP) problem (Bai, 2010), offer a fresh and general solution idea that may be achieved either directly by a solver (Gertz *et al.*, 2003) or by the use of an algorithm. There are two main common ways of solving polygonal problems: primal-dual interior-point methods and active-set methods (Forsgren *et al.*, 2016). The former requires fewer iterations whereas the latter requires more iterations but has a greater temporal complexity. By appropriately cutting the transformed matrix using a technique known as RMMSIM, Zhu *et al*. (2021) convert the mixed-cell-height legalized issue into a comparable linear complementarity problem (LCP). This technique can be effectively applied to other massive convex linear programming difficulties, including buffering and line sizing (Chu *et al.*, 1999), virtual filler implantation (Tao *et al.*, 2016), as well as analog circuitry improvement (Vichik *et al.*, 2016).

The majority of the literature that already exists bases its approximation of a solution approach upon the features of the placement challenge. Traditional methods have many shortcomings in problem-solving, such as the difficulty of achieving a balance between the objective function and restrictions when using the linear penalized method. Facing the demands raised by modern circuit design, designing or improving optimization algorithms to deal with placement problems has certain feasibility. The problem is constructed into a multi-stage model according to the l placement steps, and the difficulties are focused on the implementation of mathematical expressions and linearization of geometric constraints. Finally, according to the complexity and robustness of the algorithms, appropriate optimization algorithms are chosen to effectively solve large-scale and nonlinear placement design problems by combining the scenarios of each stage of design.

4. Mixed-cell-height placement design considering MIA constraints

4.1 MIA constraints

The MIA constraint is a physical constraint associated with the assignment of VTs. Localized VTs can form the implant-area at different locations on the chip during the fabrication process. The ion in the implanted region to which the cell belongs influences the VT of the cell after placement. The constraints imposed by the manufacturing process on the VT implant regions contributed to the formation of the MIA design rules (Kahng *et al.*, 2014a, 2014b, 2015). The MIA restrictions mandate a certain width in every VT implantation region and a minimal separation between a pair of VT implanted locations of the same kind.

As feature sizes shrink, MIA constraints have been formalized into the considerations of modern circuit placement design (Kahng *et al.*, 2014a). Modern circuit placement designs have width, spacing, and MIA constraints for each metal layer, and these constraints, which are influenced by patterning techniques, are translated into geometric problems in the placement. The ion implantation region determines the voltage of the transistor, and the implantation dimensions are usually matched to the width of a standard cell. MIA constraints were not necessary in the context of previous design rules, when cells were not small enough to create MIA violations. However, as the state of the art continues to advance, the minimum width of a standard cell is now smaller than the limit of the MIA constraint, so the MIA rule has been emphasized as a non-negligible part of modern circuit design. Because filler substances with activity can increase the activity density and manage the effect (Remy *et al.*, 2009), the MIA rule has also been applied to many commercial placement solvers.

Modern circuits apply VTs as an advanced high-performance power design to the placement design of standard cells to optimize both time (Tseng *et al.*, 2016) and power. Ion injection allows for the voltage diversity of cells, but it also makes placement more challenging because VTs make cells more heterogeneous. Depending on the doping concentration, the cells are divided into three categories with different voltages. Cells that have a low threshold voltage (LVT) operate quicker, yet have higher energy loss; standard cells with high threshold voltage (HVT) have reduced leakage power, but are slower. Standard threshold voltage (SVT) improves timing by utilizing LVT cells on the critical path, and HVT cells within the unimportant path to decrease energy loss, allowing semiconductor designs that attain outstanding efficiency with costs down (Roy *et al.*, 2003; Shebaita *et al.*, 2007). In order to optimize both time and cost in a multi-VT system, a specific VT needs to be assigned to each cell.

In addition, advanced lithography and patterning techniques create MIA limitations as the advanced process nodes progress. Narrower cells work well in circuit designs that are cost- or power-driven, but too small a cell width triggers MIA violations. As feature sizes shrink, MIA constraints are increasingly used in placement and are also a new problem in contemporary circuit design. No matter if it is a 6TPPNN cell with an unusual placement, a cell with several rows of height, or a single row of height,

the MIA constraints need to be considered due to the limitations of the fabrication process. MIA constraints are equivalent to setting a lower limit for the width of all types of cells, and when the width of a cell is smaller than the specified value, MIA violation is caused (Chen *et al.*, 2021).

MIA constraints can be specifically categorized as intra-row and inter-row (Roy *et al.,* 2003), Minimum Implantation Width (MIW) (Tao *et al.*, 2016) is a fixed value, violations occur when the width of the cell or cluster is less than the MIW value. For intra-row MIA constraints, the area of different VT cells within the same row is restricted. Cell E in Figure 8 violates the intra-row MIA constraint by having a different VT type and too narrow width than other cells located on either side. In terms of the inter-row MIA constraint, which restricts the area of multiple cells overlapping in the longitudinal direction, the rows of cells H and I result in an inter-row MIA violation.

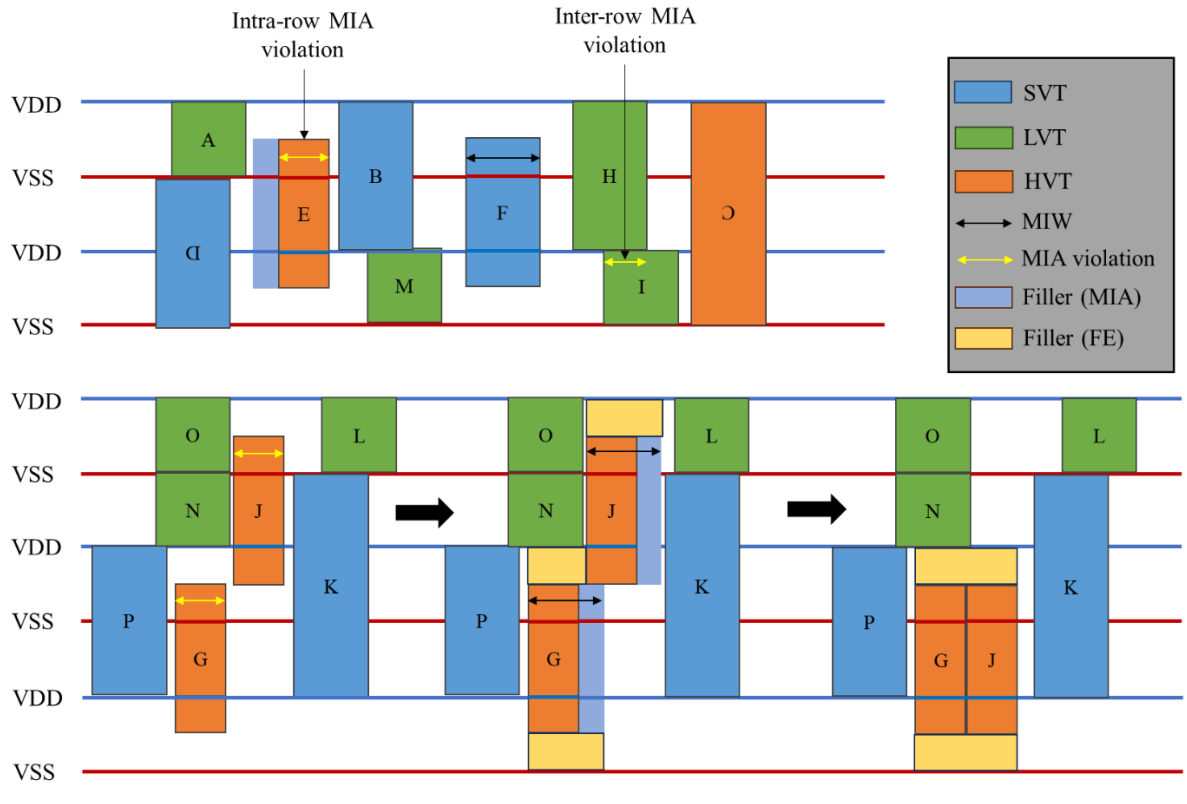

Figure 8: Standard cells placement with MIA constraints

Similar to the idea of solving the FE, there are two common ways to eliminate the MIA violation, either by adding a substitute of the exact identical sort as its VT, or by aggregating cells with the same VT (Chen *et al.*, 2022a). An example of the two ways of eliminating MIA violation is shown in Figure 8. Cell E is affected by cells that are at both of its sides should be filled by direct filling. For cells H and I, it would be more economical to use clustering. The cases of 6TPPNN cells D and J are more special are affected by FE and are generally not treated separately. For cell J, the operation of moving cell K to

the right so as to obtain enough space to fill it would incur additional costs. Therefore, it is usual to cluster this class of cells into clusters with the same VT before processing other constraints.

Ma *et al.* (2022) propose a detailed placement algorithm for multiple rows of high-standard cells perceived by MIA. They first calculate the optimal region for all cells and then reshape the cell clusters with the same threshold voltage and a standard whose width is less than the minimum implant width. Minimize the total width by designing an enhanced legalization algorithm, and solve the remaining inter-line violations with the help of the idea of the greed algorithm. Not only the MIA violation in the benchmarks be solved, but also the width is reduced by 6% compared to Chen (2021). Compared to Chen *et al.* (2021), this work not only solves the MIA violation in all benchmarks but also reduces the width by 6%.

Considering other constraints on the basis of MIA is a new challenge for advanced technology nodes, such as the combination of MIA and DDA constraints. From the above perspective, Chen *et al.* (2023) divide the placement into three stages and gradually refine the coordinates of components. They first implement the global placement through the conjugate gradient and shortest path method, then design a combined algorithm to achieve legalization, and finally complete the detailed placement without increasing MIA violations. This method can solve all MIA and almost all DDA violations, and has higher placement efficiency and better placement results than similar work.

4.2 Multi constraint bin packing problem algorithm

The chip placement design problem considering MIA constraints can be reduced to a two-dimensional or multi-dimensional BBP, so it is beneficial to summarize the algorithms for solving the BBP issue as to tackle the placement challenge. With the development of science and technology and computational tools, the research on the bin packing problem has continued to deepen and evolve, and a large research system has been formed, with new types of problems and solutions emerging continuously.

Alves and Carvalho (2005) first propose the use of column generation methods to solve the variable size bin packing problem (VSBPP). A year later, Alves and Carvalho (2006) utilize the branch-and-cut-and-price approach by tackling the multiple length cutting stock problem (MLCSP). Correia *et al.* (2008) use the discretized model reformulation technique approach for VSBPP, discretize model reformulation technique method to develop a new model for the problem. They introduce new effective inequalities to enhance the relaxation bounds of the original linear programming based on the parameters of the discretized model, and quantitative trials on 1000 items and 12 various types of boxes were used to demonstrate the usefulness of the strategy. Based on this study, Bettinelli et al. (2010) develop a new

583 model for this problem with more robustness and less symmetry but the same range of bounds. The
584 VSBPP problem is extended to study the BPP with minimum filling constraint (BPPMFC) problem.
585 For the BPPMFC problem, two branching strategies are designed to solve the problem using a new
586 heuristic algorithm and the branching pricing method. Additionally, fast meta-heuristic, lower bound
587 rounding technique and dyadic cutting planes are used to for speeding the convergent phase with the
588 column generation in the branching pricing method. Numerical experiments on three arithmetic cases
589 are carried out to validate the validity of the method. Baldi *et al.* (2014) address the previous findings,
590 proposed a more generalized problem, namely Variable Cost and Size bin packing problem with
591 optional items (VCSBPPo), classified all packing problems into this type of problem, which led to the
592 conclusion that the method for solving the VCSBPPo problem also works well for other problems of
593 the same type. good results. Baldi *et al.* (2014) model the Set Covering Formulation representation for
594 this problem and design exact upper and lower bounds. The problem was solved using a branching
595 strategy designed by Bettinelli *et al.* (2010) use branch pricing and heuristic algorithms named bundle
596 search. The problem was solved using three iterative methods to obtain lower bounds for the sub-nodes,
597 after pricing a tighter lower bound was obtained using rounding to improve the performance of the
598 algorithm, and extensive test experiments were used for both methods to illustrate the effectiveness of
599 the methods.

600 The above exact algorithms for solving BPP are dominated by the idea of enumeration, branch-and-
601 bound. In addition to this, many new ideas and methodologies have been researched and proposed by
602 scholars for approximation algorithms to achieve fast solutions. Kang and Park (2003) introduce a new
603 approximation method using the greedy strategy, Haouari and Serairi (2009) propose a set covering
604 heuristics to solve this limited variable-size boxing issue, and Crainic *et al.* (2011) design new lower
605 bounds and heuristic algorithms to solve related problems. Lee *et al.* (2013), inspired by flange-cutting
606 of wind turbines, gave a knapsack problem-based approach to tackle a multifaceted undercutting issue
607 as the variable-size crating problem. Wei *et al.* (2013) for the variable-size multifaceted BPP issue give
608 more efficient algorithms than before to solve the problem by using the method of decomposition of the
609 search space into subsets and sorting them. Fernández *et al.* (2013) design a concurrent multiple goals
610 modal method with a specific search method for the rotatable two-dimensional BBP with loading
611 equilibrium.

612 Two-dimensional chip placement design focuses optimization on one metal layer, but with the
613 development of design technology, chip placement design is gradually expanding to the multi-metal
614 level. The three-dimensional chip placement design challenge becomes a combinatorial optimization
615 issue involving complicated restrictions, and if an exact solution algorithm is used, the combinatorial

explosion may occur as the problem size continues to expand. Heuristic solution algorithms, which can search for the best solution within acceptable computational cost, are mostly used for solving nondeterministic polynomial problems, and have become the preferred choice for BPP. George *et al.* (1980) propose heuristic algorithms based on "layers"; based on this, Araya *et al.* (2020) use a cluster search algorithm to deal with the two-objective problem. Bischoff *et al.* (1990) design a block algorithm based on similar objects, where the block consists of identical objects. Based on this theory, Eley *et al.* (2002) propose a tree algorithm, and Mack *et al.* (2004) suggest an area-based search strategy and combine a block generation algorithm. Various solution techniques are indicated within studies (Bang *et al.*, 2012), especially for the complex three-dimensional BPP. The current heuristic algorithms have all achieved good results in solving BPP with simple constraints, but there are few algorithms for three-dimensional BPP with multiple constraints. For the chip placement design problem, different design rules need to be formulated for different functional requirements, which leads to the impossibility of forming a generalized solution algorithm to solve a specific problem. This requires a model that covers a wider range of practical scenarios in the placement design solution formulation process.

The exact algorithm is mainly based on the idea of enumeration algorithm to solve the exact solution of small-scale problems, the exact algorithm is more accurate but slower to deal with the actual problem. The heuristic algorithm applies self-designed placement rules to generate the solution to the problem. These placement rules are primarily based on the characteristics of rectangular items, such as length, area, and the geometric characteristics of the area to be laid out. By designing appropriate matching rules, the algorithm sequentially places units of mixed heights into the placement area. Heuristic algorithms are obtained based on different matching rules, but the heuristics are difficult to guarantee high-quality solutions for all the arithmetic cases. So fusing heuristic and exact algorithms is an idea to deal with the placement design problem. With the speed advantage of heuristic algorithms, the optimization mechanism of exact algorithms is improved to achieve a certain balance between solution speed and accuracy.

4.3 Placement design algorithm

The use of inserting identical fillers to deal with MIA violations has been applied in many studies. Yella and Sechen (2017) implement voltage-aware insertion of filler cells from the perspective of user requirements, which can be customized to place fillers between cells with different voltage types. Kahng and Lee (2014a) solve the chip placement optimization considering gate size in the inter-row MIA problem, using the idea of inserting fillers row by row to eliminate MIA violation. Although this approach achieves threshold voltage classification and guarantees space utilization. it does not achieve

zero MIA violations. They also propose the idea of intra-row MIA, restricting the order of cell placement. These ideas theoretically resolve all MIA violations, however, are not practical as they cause huge space cost. Han *et al.* (2015) build on this foundation and use mixed integer linear programming (MILP) for handling two types of MIA violations for the characteristics of the detailed placement process. Lei *et al.* (2016) employ integer linear programming (ILP) to address the issue of multiple threshold voltages. However, the solution space of these research schemes is limited and incurs significant area overhead.

Another way to solve the MIA violation is to aggregate offending cells among additional cells with a comparable threshold voltage type to form a larger implanted area, which can save the area cost. Tseng *et al.* (2016) perform the meticulous placement with the support of the second solution, but do not consider the intra-row MIA violation. Chen *et al.* (2022a) deal with both MIA violations based on the idea of global placement framework and further repair in the legalization phase, but do not view the MIA limits during the meticulous positioning phase. Wu *et al.* (2016) prioritize the repair of intra-row MIA infractions through aggregating cells with a comparable height and the same VT type. They use an algorithm of dynamic planning calculus combined with a network flow formulation to repair intra-row MIA violations. Compared with the padding method, the clustering method makes it easier to deal with all MIA violations within the specified running time and limited cost.

Since the optimization of mixed-cell-height circuits is very demanding in terms of area, time, and power (Li *et al.*, 2012; Lin *et al.*, 2022), mixed-cell-height placements are usually designed in conjunction with MIA constraints. Tseng *et al.* (2016) propose a detailed placement algorithm based on MIA-awareness, which efficiently solves the assignment challenge on MIA constraints via grouping offending cells. They identify VT MIA constraints and apply the clustering-based comprehensive placing algorithm to address the placement issue. This study extends the existing cell-based detailed placement algorithms and proposes a network flow-based algorithm to perturb the clustering to further minimize the design area. Chen *et al.* (2021) first solve the inter-row MIA violation by rearranging the mixed-height cells which have the same VTs and then fix the intra-row MIA violation by a detailed placement that aims at minimizing displacement. They solve all MIA violations without increasing area costs. Based on the above studies, Chen *et al.* (2021) also consider the mixed-cell-height positioning challenge by applying grouping along with reshaping methods. Chen *et al.* (2018) solve the placement problem by designing algorithms to concurrently take account of rail accordance limitations, MIA limitations, cell delivery, and displacements. They use cost functions for alignment constraints and a dynamic weighted network approach for MIA violations, respectively. Finally, the problem is transformed into a QP model, the MMSIM approach is used to solve it.

Considering the placement problem in modern circuit design from the perspective of operation optimization, the difficulty lies in how to build a mathematical programming model according to the actual placement. The source of parameters can be referred to existing research, or filter and obtain data from relevant competitions. After determining the research topic, the decision variables and their definition domains can be determined according to the design rules. The basic idea of model construction is to select specific indicators as optimization objectives, and to find numerical relationships between parameters and decision variables. This must be considered for linearization issues before being verified by commercial solvers. Because of the large scale of the placement problem, it is unrealistic to rely solely on the model to solve the problem. In order to meet the requirements of the placement, it is also important to design an appropriate algorithm based on the model.

Regarding MIA restrictions, the chip placement design issue is complicated, and nonlinear optimization methods have taken the mainstream advantage. Although this type of method can describe the placement design process precisely, the degree of model fitting and the accuracy of the solution are not stable. Linear optimization methods, that reflect the geometric design and specification requirements of the placement mathematical expressions, make it easier to grasp the degree of validation. Although the linearization process is hard to deal with, there are various algorithmic choices to optimize the placement problem. In summary, the design of methods needs to be based on the complexity and applicability of the model, so that accurate and reliable placement results can be obtained.

5. Challenges and future works

In VLSI, placement is actually the methodical positioning of components in a given space in accordance with the appropriate process design guidelines, predicated on a provided netlist, and continuously optimized in accordance with predetermined goals (Zhu *et al.*, 2018a). Placement belongs to the key steps in the PD of VLSI. Placement results have a disproportionately large impact on circuit performance as the technological node transitions into the era of billion-transistor integration levels. (Zhu *et al.*, 2015). Therefore, the development of algorithms that can handle components of the order of millions for the VLSI placement design problem is a study of both value and challenge. Data collection, algorithm application and its fitness are two fundamental difficulties in VLSI placement design. These researchers (Chan *et al.*, 2017; Huang *et al.*, 2019) address the data challenges while protecting commercial privacy, integrating benchmarks, metrics, and models to contribute to the advancement of placement design.

The challenges encountered in placement optimization can be summarized as follows.

(1) Increasingly complex chip designs present engineers with three challenges: performance, power, and area. It is crucial to link the chip's performance to the sophisticated process since these design difficulties are directly related to the chip's development objectives. When these three factors are considered simultaneously in placement design, there are conflicting optimization goals. Aggressively minimizing wire lengths can lead to area congestion, while excessive wire lengths can reduce chip efficiency. It is difficult to optimize multiple metrics to achieve an optimal placement solution. The result may be a negative change in other metrics towards the overall goal due to the unconscious prioritization of one metric during the optimization process.

(2) Artificial intelligence (AI) and machine learning (ML) methods are emerging in placement design, yet their reliability is yet to be fully established. By analyzing and learning from extensive data, AI technology can enhance chip performance by optimizing models and their parameters. Nevertheless, the accuracy of AI models depends on the quantity and quality of input data, and the resulting models are often highly nonlinear. This not only makes understanding the model challenging, but also impacts the decision-making process. Furthermore, every chip company attempts to maintain control over open-source data while refusing to disclose private data, which increases the likelihood of discrepancies in the data used for AI. Although ML can self-correct errors, it may not operate as effectively when encountering inaccessible or incorrect data that impacts the training model. This lack of robustness compared to traditional EDA design tools can hinder the overall performance of AI-based design solutions.

(3) In the model of VLSI chip placement design, the number of parameters and decision variables can reach up to 100,000, resulting in an enormous amount of data to be processed. The model involves numerous multiplication and accumulation operations, which consume a significant amount of computational resources. Therefore, even with the help of neural network training and inference, it is challenging to find the optimal solution. Although neural network training models have shown a capability to grow at a significant rate of up to an order of magnitude per year, they still face a considerable amount of pressure in meeting the market demand for continuous reduction in chip power consumption, cost, area, and so on.

In response to the above placement design problems, this paper combines recent research results and puts forward some constructive suggestions as ideas for future placement optimization research.

(1) In the pursuit of higher performance, lower power consumption, and smaller areas, it is difficult to achieve the goals directly by adding constraints, and multiple optimization iterations are required. Imposing geometric constraints can simplify the placement design problem, e.g., a standard cell design based on rows is easier to implement than a fully customized placement. The trade-off is that it increases

the cost of design optimization and may deprive the circuit of the opportunity to achieve better performance. Therefore, when faced with a complex design process, the conditional use of geometric transformations incorporates spatial placement constraints into the algorithmic rules. A step-by-step optimization effort through multiple flows of the placement, with optimization objectives evaluated independently within each operation, can lead to better results while meeting technical constraints.

(2) Although there are more ways to perform placement design in the context of mega data, optimization algorithms still play a crucial role in placement. Constructing optimization algorithms for the iterative characteristics of placement design, writing technical constraints into algorithmic rules, and combining the iterative solution ideas of algorithms with the iterative process in placement problems are all design ideas for placement algorithms. In addition to developing new algorithms, improving existing algorithms is also considerable. Existing methods have not been able to eliminate all the negative effects of emerging technologies within a reasonable time, so there is still space for improvement in the pursuit of algorithmic accuracy and operating speed.

(3) From the perspective of saving design costs for semiconductor companies, it is crucial to apply AI techniques to the placement design process. As advanced nodes become twice as expensive, cost remains a top priority in placement optimization. By using AI technology, many low-level tasks such as data classification and processing can be automated, saving labor costs and reducing the possibility of human error. In addition, AI algorithms can analyze data, find patterns, and make more accurate predictions and decisions to help companies better utilize resources and improve production efficiency. AI algorithms can also be combined with ML to reduce computational tasks in the verification stage, shorten the design cycle, and reduce costs. AI technology is also suitable for different application scenarios, helping designers select appropriate design styles and optimize design frameworks, which can also promote efficient resource utilization.

6. Conclusions

Starting from the framework of placement design optimization, we provide a detailed review of the contents and methods of placement for various circuits' qualities. After determining the status of VLSI digital circuit placement, the circuits are divided based on design style and technology characteristics. An overview of basic placement design and methodology is emphasized in the case of traditional circuits, and an understanding of emerging technologies from existing research is added in the case of modern circuits. For each circuit placement design section, the literature on representative methods is listed and summarized. Finally, the technical and methodological challenges of existing placement

design are compiled, and future research ideas are organized with the latest research.

Algorithms are the most critical aspect of placement design research. Whether it is the placement algorithm as enlightenment or the optimization algorithm that is becoming popular, there is much space for progress. With the updating of data sets and the development of key technologies, the advantages of optimization algorithms gradually come to the fore, and overcoming the difficulties of linearization and geometric design can help the breakthrough of automated placement design for VLSI.

References

Alves C., & Valério D. (2005) Accelerating column generation for variable sized bin-packing problems. *European Journal of Operational Research* 183(3): 1333–1352.

Alves C., & Valério D. (2006) A stabilized branch-and-price-and-cut algorithm for the multiple length cutting stock problem. *Computers & Operations Research* 35(4): 1315–1328.

Araya I., Moyano M., & Sanchez C. (2020) A beam search algorithm for the biobjective container loading problem. *European Journal of Operational Research* 286(2): 417−431.

Baek S. H., Kim H. Y., Lee Y. K., Jin D. Y., Park S. C., & Cho J. D. (2008) Ultra-high density standard cell library using multi-height cell structure. *Smart structures, devices, and systems IV*: 72680C-8.

Bai Z. Z. (2010) Modulus-based matrix splitting iteration methods for linear complementarity problems. *Numerical Linear Algebra with Applications* 17(6): 917–933.

Baldi M., Crainic T., Perboli G., & Tadei R. (2014) Branch-and-price and beam search algorithms for the Variable Cost and Size Bin Packing Problem with optional items. *Annals of Operations Research* 222(1): 125−141.

Balogh J., Békési J., Dósa G., Epstein L., & Levin A. (2021) A new lower bound for classic online bin packing. *Algorithmica* 83(7): 2047–2062.

Bang J., & Larsen R. (2012) Efficient algorithms for real-life instances of the variable size bin packing problem. *Computers & Operations Research* 39(11): 2848−2857.

Bettinelli A., Ceselli A., & RighiniI G. (2010) A branch-and-price algorithm for the variable size bin packing problem with minimum filling constraint. *Annals of Operations Research* 179(1): 221−241.

Bischoff E., & Marriott M. (1990) A comparative evaluation of heuristics for container loading. *European Journal of Operational Research* 44(2): 267−276.

Brenner U., & Vygen J. (2000) Faster optimal single-row placement with fixed ordering. *Proceedings Design, Automation and Test in Europe Conference and Exhibition 2000*: 117–121.

Brenner U. (2013) BonnPlace legalization: minimizing movement by iterative augmentation. *IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems* 32(8): 1215–1227.

Boutros A., Yazdanshenas S., & Betz V. (2018) You cannot improve what you do not measure: FPGA vs. ASIC efficiency gaps for convolutional neural network inference. *ACM Transactions Reconfigurable Technology System* 11(3): 1–23.

Chan W. J., Ho P. H., Kahng A. B., & Saxena P. (2017) Routability optimization for industrial designs at sub-14nm process nodes using machine learning. *The 2017 ACM on International Symposium on Physical Design*: 15–21.

Chang Y. W., Jiang, Z. W., & Chen T. C. (2009) Essential issues in analytical placement algorithms. *IPSJ Transactions on System LSI Design Methodology* 2: 145–166.

Chen G. H., Zeng Z., Zhu B. C., Li J. W., Wang K., Yu J., & Chen J. L. (2023) Mixed-cell-height placement with minimum-implant-area and drain-to-drain abutment constraints. *2023 60th ACM/IEEE Design Automation Conference (DAC)*: 1–6.

Chen J. L., Zhu W. X., & Peng Z. (2012a) A heuristic algorithm for the strip packing problem. *Journal of Heuristics* 18(4): 677–697.

Chen J. L., Zhu Z. R., Zhu W. X., & Chang Y. W. (2012b) A robust modulus-based matrix splitting iteration method for mixed-cell-height circuit legalization. *ACM Transactions on Design Automation of Electronic Systems* 26(2): 1–28.

Chen J. L., Zhu Z. R., Zhu W. X., & Chang Y. W. (2017) Toward optimal legalization for mixed-cell-height circuit designs. *The 54th Annual Design Automation Conference 2017*: 1–6.
Chen J. L., Lin Z. F., Kuo Y. C., Huang C. C., Chang Y. W., Chen S. C., Chiang C. H., & Kuo S. Y. (2020) Clock-Aware placement for large-scale heterogeneous FPGAs. *IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems* 39(12): 5042–5055.
Chen J. L., Chang Y. W., & Wu Y. Y. (2021) Mixed-cell-height detailed placement considering complex minimum-implant-area constraints. *IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems* 40(10): 2128–2141.
Chen, J. L., Lin Z., Xie Y. Y., Zhu W. X., & Chang Y. W. (2022a) Mixed-cell-height placement with complex minimum-implant-area constraints. *IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems* 41(11): 4639–4652.
Chen J. L., Zhu Z. R., Guo L., Tseng Y. W., & Chang Y. W. (2022b) Mixed-cell-height placement with drain-to-drain abutment and region constraints. *IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems* 41(4): 1103–1115.
Chen J. W., Di Z. X., Shi J. Y., Feng Q. Y., & Wu Q. (2022c) NBLG: a robust legalizer for mixed-cell-height modern design. *IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems* 41(11): 4681–4693.
Chow W. K., Pui C. W., & Young E. Y. (2016a) Legalization algorithm for multiple-row height standard cell design. *The 53rd Annual Design Automation Conference*: 1–6.
Chow W. K., & Young E. Y. (2016b) Placement: from wirelength to detailed routability. *IPSJ Transactions on System LSI Design Methodology* 9: 2–12.
Chu C. N., & Wong D. F. (1999) A quadratic programming approach to simultaneous buffer insertion/sizing and wire sizing. *IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems* 18(6): 787–798.
Correia I., Gouveia L., & Saldanha F. (2008) Solving the variable size bin packing problem with discretized formulations. *Computers & Operations Research* 35(6): 2103−2113.
Crainic T. G., Perboli G., Rei W., & Tadei R. (2011) Efficient lower bounds and heuristics for the variable cost and size bin packing problem. *Computers & Operations Research* 38(11): 1474−1482.
Dadaliaris A. N., Nerantzaki E., Koziri M. G., Oikonomou P., Loukopoulos T., & Stamoulis G. I. (2016) Performance evaluation of Tetris-based legalization heuristics. *The 20th Pan-Hellenic Conference on Informatics*: 1–6.
Darav N. K., Kennings A., Tabrizi A. F., Westwick D., & Behjat L. (2016) Eh?Placer: a high-performance modern technology-driven placer. *ACM Transactions on Design Automation of Electronic Systems* 21(3): 1–27.
Dobre S. A., Kahng A. B., & Li J. J. (2018) Design implementation with noninteger multiple-height cells for improved design quality in advanced nodes. *IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems* 37(4): 855–868.
Eley M. (2002) Solving container loading problems by block arrangement. *European Journal of Operational Research* 141(2): 393−409.
Farghadan A., and Mohammadzadeh N. (2017) Quantum circuit physical design flow for 2D nearest-neighbor architectures: quantum circuit design flow. *International Journal of Circuit Theory and Applications* 45(7): 989–1000.
Fernández A., Gil C., Baños R., & Montoya M. G. (2013) A parallel multi-objective algorithm for two-dimensional bin packing with rotations and load balancing. *Expert Systems with Applications* 40(13): 5169–5180.
Forsgren A., Gill P. E., & Wong E. (2016) Primal and dual active-set methods for convex quadratic programming, *Mathematical Programming* 159(1): 469–508.
George J., & Robinson D. (1980) A heuristic for packing boxes into a container. *Computers & Operations Research* 7(3): 147−156.
Gertz E. M., & Wright S. J. (2003) Object-oriented software for quadratic programming. *ACM Transactions on Mathematical Software* 29(1): 58–81.
Gupta P., Kahng A. B., & Park C. H. (2005) Detailed placement for improved depth of focus and CD control. *The ASP-DAC 2005. Asia and South Pacific Design Automation Conference*: 343–348.
Guo Z., Mai J., & Lin Y. (2021) Ultrafast CPU/GPU kernels for density accumulation in placement. *2021 58th ACM/IEEE Design Automation Conference (DAC)*: 1123–1128.

879 Hao R., Cai Y. C., Zhou Q. (2022) Intelligent and kernelized placement: A survey. *Integration-the VLSI*
880 *Journal*: 86: 44–50.
881 Han K., Kahng A. B., & Lee H. (2015) Scalable detailed placement legalization for complex sub-14nm
882 constraints. *2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*: 867–
883 873.
884 Haouari M., & Serairi M. (2009) Heuristics for the variable sized bin-packing problem. *Computers &*
885 *Operations Research* 36(10): 2877−2884.
886 Hsu M. K., & Chang Y. W. (2010) Unified analytical global placement for large-scale mixed-size circuit
887 designs. *2010 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*: 657–662.
888 Hsu M. K., Balabanov V., & Chang Y. W. (2013) TSV-aware analytical placement for 3-D IC designs
889 based on a novel weighted-average wirelength model. *IEEE Transactions on Computer Aided Design*
890 *of Integrated Circuits & Systems* 32(4): 497–509.
891 Hu V. P., Wu Y. S., & Su P. (2009) Investigation of electrostatic integrity for ultra-thin-body GeOI
892 MOSFET using analytical solution of Poisson's equation. *Semiconductor Science and Technology*
893 24(4): 1–7.
894 Huang C. C., Chien H. C., Tseng K. H., & Chang Y. W. (2015) Detailed-routing-driven analytical
895 standard-cell placement. *The 20th Asia and South Pacific Design Automation Conference*: 378–383.
896 Huang C. C., Lee H. Y., Lin B. Q., Yang S. W., Chang C. H., & Chen S. T. (2017) NTUplace4dr: a
897 detailed-routing-driven placer for mixed-size circuit designs with technology and region constraints.
898 *IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems* 37(3): 669–681.
899 Huang Y. H., Xie Z. Y., Fang G. Q., Yu T. C., Ren H. X., Fang S. Y., Chen Y. R., & Hu J. (2019)
900 Routability-driven macro placement with embedded CNN-based prediction model. *2019 Design,*
901 *Automation & Test in Europe Conference & Exhibition (DATE)*: 180–185.
902 Hung C. Y., Chou P. Y., & Mak W. K. (2017) Mixed-cell-height standard cell placement Legalization.
903 *The on Great Lakes Symposium on VLSI 2017*: 149–154.
904 Kahng A. B., Tucker P., & Zelikovsky A. (1999) Optimization of linear placements for wirelength
905 minimization with free sites. *The ASP-DAC '99 Asia and South Pacific Design Automation*
906 *Conference 1999*: 241–244.
907 Kahng A. B., Markov I. L., & Reda S. (2004) On legalization of row-based placements. *The 14th ACM*
908 *Great Lakes symposium on VLSI*: 214–219.
909 Kahng A. B., Lienig J., Markov I. L., & Hu L. (2011) *VLSI Physical Design: From Graph Partitioning*
910 *to Timing Closure*.
911 Kahng A. B., and Lee H. (2014a) Minimum implant area-aware gate sizing and placement. *The 24th*
912 *edition of the great lakes symposium on VLSI*: 57−62.
913 Kahng A. B. (2014b) Lithography-induced limits to scaling of design qualit. *the SPIE Advanced*
914 *Lithography*: 905302.
915 Kahng A. B. H. (2015) New game, new goal posts: a recent history of timing closure. *The 52nd Annual*
916 *Design Automation Conference*: 1−6.
917 Kahng A. B., Kuang J., Liu W. H., Xu B. Q. (2022) In-route pin access-driven placement refinement
918 for improved detailed routing convergence. *IEEE Transactions on Computer Aided Design of*
919 *Integrated Circuits & Systems* 41(3): 784–788.
920 Kang J., & Park S. (2003) Algorithms for the variable sized bin packing problem. *European Journal of*
921 *Operational Research* 147(2): 365−372.
922 Karimullah S., Vishnuvardhan D., Bhaskar V. (2022) An improved harmony search approach for block
923 placement for VLSI design automation. *Wireless Personal Communications*: 127(4): 3041−3059.
924 Karimpour Darav N., Bustany I. S., Kennings A., & Behjat L. (2017) A fast, robust network flow-based
925 standard-cell legalization method for minimizing maximum movement. *The 2017 ACM on*
926 *International Symposium on Physical Design*: 141–148.
927 Kennings A., Darav N. K., & Behjat L. (2014) Detailed placement accounting for technology
928 constraints. *2014 22nd International Conference on Very Large Scale Integration (VLSI-SoC)*: 1–6.
929 Kim M. C., & Markov I. L. (2012) ComPLx: A competitive primal-dual Lagrange optimization for
930 global placement. *The 49th Annual Design Automation Conference*: 747–752.
931 Kucukyilmaz T., & Kiziloz H. E. (2018) Cooperative parallel grouping genetic algorithm for the one-
932 dimensional bin packing problem. *Computers & Industrial Engineering* 125: 157–170.
933 Kuon I., & Rose J. (2007) Measuring the gap between FPGAs and ASICs. *IEEE Transactions on*

Computer Aided Design of Integrated Circuits & Systems 26(2): 203–215.
Lee J., Kim B., & Johnson A. (2013) A two-dimensional bin packing problem with size changeable items for the production of wind turbine flanges in the open die forging industry. *IIE Transactions* 45(12): 1332−1344.
Lei S. I., Mak W. K., and Chris C. (2016) Minimum implant area-aware placement and threshold voltage refinement. *The 21st Asia and South Pacific Design Automation Conference (ASP-DAC)* 36(7): 1103−1112.
Li H. C., Chow W. K., Chen G. J., Young E. Y., & Yu B. (2018a) Routability-driven and fence-aware legalization for mixed-cell-height circuits. *The 55th Annual Design Automation Conference*: 1–6
Li W. X., Lin Y. B., Li M., Dhar S., & Pan D. Z. (2018b) UTPlaceF 2.0: A high-performance clock-aware FPGA placement engine. *ACM Transactions on Design Automation of Electronic Systems* 23(4): 1–23.
Li W. X., Dehkordi M. E., Yang S., & Pan D. Z. (2019a) Simultaneous placement and clock tree construction for modern FPGAs. *The 2019 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*: 132–141.
Li X., Chen J. L., Zhu W. X., & Chang Y. W. (2019b) Analytical mixed-cell-height legalization considering average and maximum movement minimization. *The 2019 International Symposium on Physical Design*: 27–34.
Liang S. H., Hsiung T. L., Mak W. K., & Wang T. C. (2023) Hybrid-row-height design placement legalization considering cell variants. *Great Lakes Symposium on VLSI*: 363–367.
Liang T., Chen G., Zhao J., Sinha S., & Zhang W. (2021) AMF-Placer: high-performance analytical mixed-size placer for FPGA. *2021 IEEE/ACM International Conference on Computer Aided Design (ICCAD)*: 1–9.
Lin M. H., Hsu C. C., & Chang Y. T. (2011) Recent research in clock power saving with multi-bit flip-flops. *2011 IEEE the 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*: 1–4.
Lin Y. B., Yu B., Xu X. Q., Gao J. R., Viswanathan N. Liu W. H., Li Z., Alpert C. J., & Pan D. Z. (2018) MrDP: multiple-row detailed placement of heterogeneous-sized cells for advanced nodes. *IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems* 37(6): 1237–1250.
Lin Z. F., Xie Y. Y., Qian G., Chen J. L., Wang S. F., Yu J., & Chang Y. W. (2021) Timing-driven placement for FPGAs with heterogeneous architectures and clock constraints. *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*: 1564–1569.
Lin Z. F., Xie Y. Y., Zou P., Wang S. F., Yu J., & Chen J. L. (2022) An incremental placement flow for advanced FPGAs with timing awareness. *IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems* 41(9): 3092–3103.
López-Camacho E., Terashima-Marin H., Ross P., & Ochoa G. (2014) A unified hyper-heuristic framework for solving bin packing problems. *Expert Systems with Applications* 41(15): 6876–6889.
Lu J. W., Chen P. W., Chang C. C., Lu S., Huang D. H., Teng C. C., & Cheng C. K.（2014） ePlace: Electrostatics-based placement using fast fourier transform and nesterov's method. *2014 51st ACM/EDAC/IEEE Design Automation Conference (DAC)*: 1–6.
Ma J., Yu W. X., Fu Z. Q., & Cheng X. (2022) Optimal region-based mixed-cell-height detailed placement considering complex minimum-implant-area constraints. *Great Lakes Symposium on VLSI*: 173–176.
Mack D., Bortfeldt A, & Gehring H. (2004) A parallel hybrid local search algorithm for the container loading problem. *International Transactions in Operational Research* 11(5): 511−533.
Markov I. L., Hu J., & Kim M. C. (2015) Progress and challenges in VLSI placement research. *Proceedings of the IEEE* 103(11): 1985–2003.
Pereira J. (2016) Procedures for the bin packing problem with precedence constraints. *European Journal of Operational Research* 250(3): 794–806.
Puget J. C., Flach G., Johann M., & Reis R. (2015) Jezz: An effective legalization algorithm for minimum displacement. *The 28th Symposium on Integrated Circuits and Systems Design*: 1–5.
Quiroz M., Cruz L., Torres J., Gomez G., Huacuja H. F., & Alvim A. (2015) A grouping genetic algorithm with controlled gene transmission for the bin packing problem. *Computers & Operations Research* 55: 52−64.

Remy L., Coll P., Picot F., Mico P., & Portal J. M. (2009) Definition of an innovative filling structure for digital blocks: the DFM filler cell. *The 16th IEEE International Conference on Electronics, Circuits and Systems*: 73–76.

Roy K., Mukhopadhyay S., & Mahmoodi-Meimand H. (2003) Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits. *Proceedings of the IEEE* 91(2): 305–327.

Shebaita A., & Ismail Y. (2008) Multiple threshold voltage design scheme for CMOS tapered buffers. *IEEE Transactions on Circuits Systems* 55(1): 21–25.

Tao Y. D., Yan C. H., Lin Y. B., Wang S. G., Pan D. Z., & Zeng X. (2016) A novel unified dummy fill insertion framework with SQP-based optimization method. *The 35th International Conference on Computer-Aided Design*: 1–8.

Tseng K. H., Chang Y. W., & Liu C. C. (2016) Minimum-implant-area-aware detailed placement with spacing constraints. *The 53rd Annual Design Automation Conference*: 1–6.

Vichik S., Arcak M., & Borrelli F. (2016) Stability of an analog optimization circuit for quadratic programming. *Systems & Control Letters* 88: 68–74.

Wang C. H., Wu Y. Y., Chen J. L., Chang Y. W., Kuo S. Y., Zhu W. X., & Fan G. H. (2017) An effective legalization algorithm for mixed-cell-height standard cells. *The 22nd Asia and South Pacific Design Automation Conference (ASP-DAC)*: 450–455.

Wang C. K., Huang C. C., Liu S. Y., & Chin C. Y. (2015a) Closing the gap between global and detailed placement: techniques for improving routability. *The 2015 Symposium on International Symposium on Physical Design*: 149–156.

Wang J., Wong A. K., & Lam E. Y. (2004) Standard cell layout with regular contact placement. *IEEE Transactions on Semiconductor Manufacturing* 17(3): 375–383.

Wang X. Y., Liu C., Wei Y. N., Feng S., Sun D. M., & Cheng H. M. (2023a) Three-dimensional transistors and integration based on low-dimensional materials for the post-Moore's law era. *Materials Today* 63: 170–187.

Wang Y. C., Lin B. S., & Chan M. C. (2015b) Electro-optical measurement and process inspection for integrated gate driver circuit on thin-film-transistor array panels. *Measurement* 70: 83–87.

Wang Z. Q., Hua Y., Aubry N., Zhou Z. F., Feng F., & Wu W. T. (2023b) Fast optimization of multichip modules using deep learning coupled with Bayesian method. International Communications in Hear and Mass Transfer 141: 106592.

Wei L., Oon W., Zhu W. B., & Lim A. (2013) A goal-driven approach to the 2D bin packing and variable-sized bin packing problems. *European Journal of Operational Research* 224(1): 110-121.

Wu G., & Chu C. (2016) Detailed placement algorithm for VLSI design with double-row height standard cells. *IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems* 35(9): 1569–1573.

Wu C. H., Mak W. K., & Chu C. (2023) Linear-time mixed-cell-height legalization for minimizing maximum displacement. *The 31st edition of the ACM International Symposium on Physical Design (ISPD)*: 211–218.

Yang P., Chen Y. H., Chen J. L., Zhou H. B., & Dong S. H. (2019) 6T&6TPPNN cell legalization considering complex minimum width constraint. *2019 China Semiconductor Technology International Conference (CSTIC)*: 1–3.

Yella A. K., & Sechen C. (2017) Improved lagrangian relaxation-based gate size and VT assignment for very large circuits. *2017 1st Conference on PhD Research in Microelectronics and Electronics Latin America (PRIME-LA)*: 1–4.

Yu M. Y., & Iris H. J. (2010) Analog placement and global routing considering wiring symmetry. *2010 11th International Symposium on Quality Electronic Design (ISQED)*: 618–623.

Zhu W. X., Chen J. L., & Li W. Q. (2014) An augmented Lagrangian method for VLSI global placement. *Journal of Supercomputing* 69(2): 714–738.

Zhu W. X., Chen J. L, Peng Z., & Fan G. H. (2015) Nonsmooth optimization method for VLSI global placement. *IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems* 34(4): 642–655.

Zhu W. X., Huang Z. P., Chen J. L., & Chang Y. W. (2018a) Analytical solution of Poisson's equation and its application to VLSI global placement. *The International Conference on Computer-Aided Design*: 1–8.

Zhu Z. R., Chen J. L., Peng Z., Zhu W. X., & Chang Y. W. (2018b) Generalized augmented lagrangian and its applications to VLSI global placement. *The 55th Annual Design Automation Conference*: 1–6.

Zhu Z. R., Huang Z. P., Yang P., Zhu W. X., Chen J. L., & Zhou H. B. (2020) Mixed-cell-height legalization considering complex minimum width constraints and half-row fragmentation effect. *Integration, the VLSI journal* 71: 1–10.

Zhu Z. R., Mei Y. J., Li Z. J., Lin J. W., Chen J. L., Yang J., & Chang Y. W. (2022) High-performance placement for large-scale heterogeneous FPGAs with clock constraints. *The 59th ACM/IEEE Design Automation Conference*: 643–648.

Zhu, Z. R., Li X. Q., Chen Y. W., Chen J. L., Zhu W. X., & Chang Y. W. (2018c) Mixed-cell-height legalization considering technology and region constraints. *The International Conference on Computer-Aided Design*: 1–8.