WIWO Topology Analysis for Tapped-Inductor Converters with Consideration of Parasitic Elements

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***Abstract* –In this paper, a new circuit topology of tapped-inductor DC-DC converter has been introduced, considering the impacts of parasitic elements. The converter is able to provide wide input and wide output voltage (WIWO) range with high efficiency, including Buck, Boost and Buck-Boost modes. First, the principle and algorithm of the new converter has been investigated in detail. Then, the power conversion efficiency has been examined under different duty ratios. The voltage gain and efficiency have simultaneously been analyzed with various loads. Finally, the experimental results show that the efficiencies of the new topology are high in most ranges, thus verified the correctness of theory and the effectiveness of the proposed topology.**

***Index Terms*—DC-DC converter, Boost, Buck, Buck-Boost, Tapped inductor, Power supply, wide step-down, wide step- up, wide-input-wide-output (WIWO)**

I. INTRODUCTION

Conventional topologies of DC-DC converter include buck, boost and buck-boost modes with a single inductor. Theoretically, the boost circuit can provide high voltage conversion of input to output with a relatively large duty ratio. However, for boost circuit, the higher the voltage gain is, the bigger the duty ratio is and thus the lower efficiency will be produced. Similarly, the efficiency of the buck converter will also be poor when the duty ratio is small [1]. The poor efficiency is mainly due to the energy storage in the magnetic components that is not efficiently processed under extreme value of large or small duty ratio. The consequence is that high pulsation current will be generated, deteriorating the performance in semiconductor power processing. Also, the poor efficiency limits the applications of converters in the industry and this limitation is investigated in [2-3]. Recently, most researches usually focus on studying suitable topologies of Buck, Boost and Buck-Boost converters which can provide a simple and non-isolation method for power conversion with high efficiency, because in the industry, converters need to operate in a wider range of duty ratio when the isolation is negligible. A conventional bidirectional integrated configuration of the converter with a single inductor is proposed in [4] as shown in Fig.1 (a). It not only controls the MOSFETs 1 to 4, and can realize the function of converter without diode, but also the converter can transfer energy bidirectionally under the Buck, Boost and Buck-boost modes.

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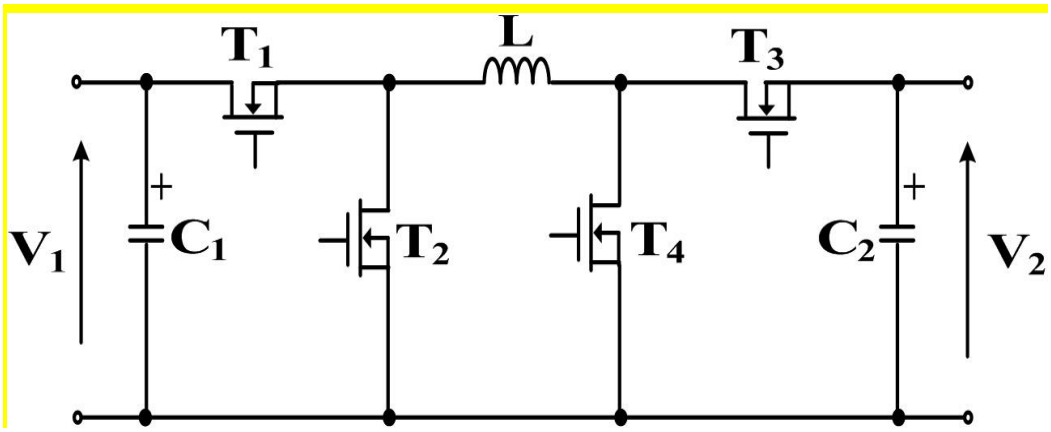
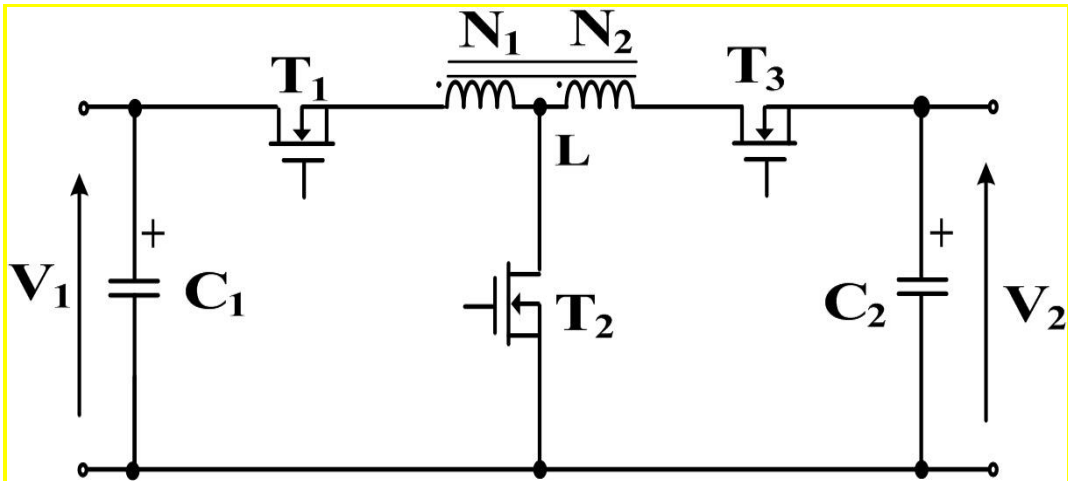
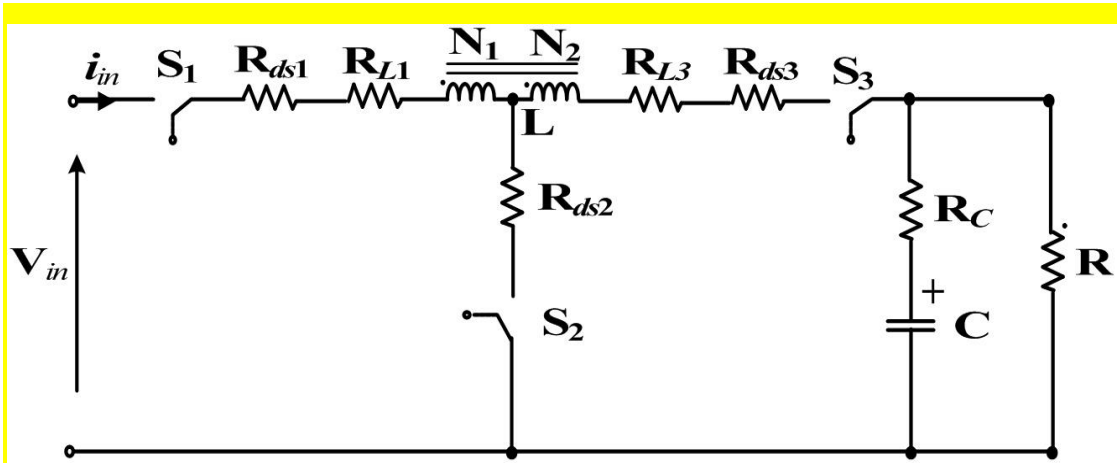


(a) A Conventional bidirectional Buck/Boost DC-DC Converter



(b) Tapped-inductor topology



(c) Tapped-inductor with parasitic components

Fig 1: Circuit topology of various formats of Buck-Boost converters

For the conventional DC-DC converter with a single inductor under the pulse width modulation (PWM) control, the voltage gain V_o/V_{in} is determined by the duty ratio, however,

the range of voltage gain are so strikingly limited by the turns of the single inductor that limits the actual conversion achievement as compared with the non-isolation counterpart [5]. Therefore, in theory, tapped inductor converter is employed and its turns can be controlled for the adjustment of the range of duty ratio. The range of voltage gain, the high conversion efficiency and reliability can be extended finally [6]. The concept is similar to the 50/60Hz auto-transformer design.

In order to achieve prominently high/low voltage gain with high efficiency, various topologies tapped inductor DC-DC converters have been explored recently. Grant et al. proposed and categorized the topologies of tapped-inductor converter based on the static performance [7-12]. Significantly, tapped inductor buck converter has been proposed for simple configuration and low cost, and that to change the duty ratio and to maintain the high efficiency [13]. Moreover, a higher efficiency is the ultimate goal of research achievement to the tapped inductor techniques [14-18]. The application to AC-DC [19] using a tapped inductor is reported to be successful.

The comparisons of the voltage gain, efficiency and component stress between the traditional and tapped-inductor converters with parasitic components have been explored. Analysis of the tapped-inductor boost converter with parasitic parameters shows that under the same duty ratio, not only the voltage gain but also the conversion efficiency of tapped-inductor converter are always higher than the traditional converter. Therefore, the range of voltage conversion of the tapped-inductor converter has been extended further than that of conventional converter [20-21]. However, only has boost circuit been analyzed in the previous researches. The buck and buck-boost modes have not been studied yet.

This paper presents a new tapped-inductor converter topology, which focuses on wide input and wide output voltage conversion range (WIWO). Especially, on the static performance, the new converter is applied with an appropriate control method to the three active switching devices without diode and with existence of parasitic parameters that has never been discussed. At the same time, there are three modes for basic principle of operation to be described, including Buck, Boost and Buck-Boost.

In Section II, the basic circuit configuration and theoretical derivation have been elaborated in detail. Section III shows the analysis of the comparisons between the voltage conversion ratio and power conversion efficiency, and the relationship of voltage conversion ratio and power conversion efficiency with different loads to three modes of operation in Buck, Boost and Buck-Boost of proposed converter. Then, the experimental results are shown in Section IV. Finally, conclusions are made in section V.

II. CIRCUIT DESCRIPTION

The basic tapped inductor DC-DC converter consists of two active switches, a tapped-inductor, a diode and a capacitive output filter. Although the modified tapped-inductor converters are prominently similar, there are three active switches without diode, thus providing the potential wider input and wider output voltage conversion range (WIWO) with higher efficiency. Therefore, the new tapped inductor converter topology consists of three actives switches, a tapped-inductor and two output filter capacitors as shown in Fig.1 (b). It is significant to note that the tapped-inductor converter is bidirectional for both the conventional topology and the proposed topology.

Fig.1 (c) shows this converter with consideration of parasitic components. In the circuit topology, R_{L1} and R_{L3} is the Equivalent Series Resistance (ESR) of primary N_1 and secondary N_2 windings, respectively. $R_{ds1,\,2,\,3}$ is the on-state resistance of active switching devices S_1, S_2 and S_3, respectively. R_c is the ESR of capacitor, R is the load resistance, and C is the capacitance of capacitor. V_{in} and V_o are the input voltage and output voltage, respectively. In particular, N_1 is equal to N_2 and all represented by N, then L is a quarter of the inductance of total tapped inductor, and the insurance of each side of the tapped-inductor is proportional to the number of turns N_1 or N_2. Assume $R_{L1}=R_{L3}=R_L$, $R_{ds1}=R_{ds2}=R_{ds3}$ in this paper. Table 1 shows the parameters used in the simulation of voltage gain and efficiency.

Table.1 Parameters used in the simulation of voltage gain and efficiency

Resistance	R_L (mΩ)	R_C (mΩ)	R_{ds} (mΩ)	R (Ω)
Values	50	70	55	10 , 20 , 50 , 100 , 200

The analysis in the following sections (*A*) to (*C*) is using the following expression for simplification and neatness:

1) The equation of the series connection of parasitic resistances two R_L, two R_{ds}, R_c parallel with load R is $\left(2R_{ds}+2R_L+\frac{R\cdot R_c}{R+R_c}\right)$ or $\left(2R_{ds}+R_L+\frac{R\cdot R_c}{R+R_c}\right)$ in different conditions of the switches, which as defined as X_1 and X_2, respectively.

2) The equation of $\frac{1}{(R+R_c)}$ is defined as Y_1.

A. Buck Converter

Fig.2 shows the modified converter that is controlled by the PWM in Buck mode. Active switches S_3 is always maintained at on-state, and S_1 and S_2 are complementary conducting. When S_1 is maintained at on-state; S_2 is maintained at off-state, the input voltage V_{in} - V_o is

developed across the tapped inductor causing an increase in current, and the capacitance C is being charged. However, when the S_2 is maintained at on-state; S_1 is maintained at off-state, the current will be reduced through the inductor L in the N_2 side. It is significant to note that S_1 and S_2 are never turned on or off at the same time.

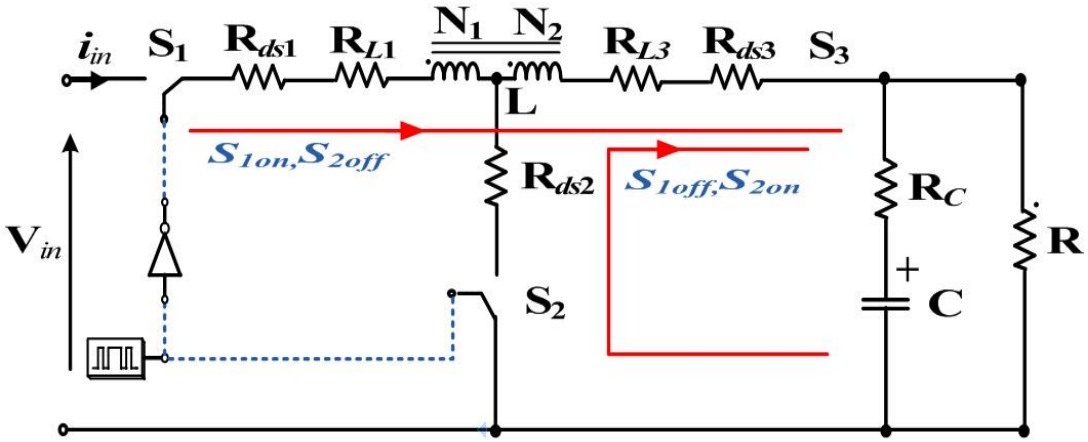


Fig.2 A tapped-inductor Buck converter with parasitic components

Formulas (1) to (6) describe the state of proposed buck converter with parasitic resistors. In all formula, φ is the flux of magnetic core, v_c is the voltage of capacitor, and which are identified as state variables. The duty ratio is represented by u .

S_3 is on-state, during S_{1on}, and S_{2off}

$$i_{Lon} = \frac{N \cdot \varphi}{2L} \tag{1}$$

$$\dot{\varphi} = \frac{V_{in}}{2N} - X_1 \cdot \frac{1}{4L} \cdot \varphi - \frac{R}{2N} \cdot v_c \cdot Y_1 \tag{2}$$

$$\dot{v}_c = \frac{N \cdot R}{2L \cdot C} \cdot \varphi \cdot Y_1 - \frac{v_c}{C} \cdot Y_1 \tag{3}$$

S_3 is on-state, during S_{1on}, and S_{2off}

$$i_{Loff} = \frac{N \cdot \varphi}{L} \tag{4}$$

$$\dot{\varphi} = -X_2 \cdot \frac{1}{L} \cdot \varphi - \frac{R}{N} \cdot v_c \cdot Y_1 \tag{5}$$

$$\dot{v}_c = \frac{N \cdot R}{L \cdot C} \cdot \varphi \cdot Y_1 - \frac{v_c}{C} \cdot Y_1 \tag{6}$$

The average state-space formula is (7), (8)

$$\dot{\varphi} = u \cdot \left(\frac{V_{in}}{2N} - X_1 \cdot \frac{1}{4L} \cdot \varphi - \frac{R}{2N} \cdot v_c \cdot Y_1 \right) + (1-u) \cdot \left(-X_2 \cdot \frac{1}{L} \cdot \varphi - \frac{R}{2N} \cdot v_c \cdot Y_1 \right) \tag{7}$$

$$\dot{v}_c = u \cdot \left(\frac{N \cdot R}{2L} \cdot \varphi - v_c \right) \cdot \frac{1}{C} \cdot Y_1 + (1-u) \cdot \left(\frac{N \cdot R}{L} - v_c \right) \cdot \frac{1}{C} \cdot Y_1 \tag{8}$$

At steady-state

$$\dot{\varphi} = 0 \tag{9}$$

$$\dot{v}_c = 0 \tag{10}$$

The average output voltage

$$V_o = \overline{v}_o = \overline{v}_c \tag{11}$$

Combining the formulas (7) (8) with (9) (10), respectively, (12) (13) are obtained to represent the V_{in} and v_c

$$\begin{cases} V_{in} = \dfrac{N \cdot \varphi}{2L} \cdot X_1 + \dfrac{(2-u)^2 \cdot R^2 \cdot N \cdot \varphi}{2L \cdot u} \cdot Y_1 + \dfrac{2(1-u) \cdot N \cdot \varphi}{L \cdot u} \cdot X_2 & (12) \\ v_c = \dfrac{(2-u) \cdot N \cdot R \cdot \varphi}{2L} & (13) \end{cases}$$

The voltage conversion ratio and flux with steady-state can be obtained as (14) and (15)

$$\begin{cases} \xi(\overline{u}) = \dfrac{V_o}{V_{in}} = \dfrac{\overline{u} \cdot (2-\overline{u})}{\overline{u} \cdot X_1 \cdot (1/R) + 4(1-\overline{u}) \cdot X_2 \cdot (1/R) + (2-\overline{u})^2 \cdot R \cdot Y_1} & (14) \\ \overline{\varphi} = \dfrac{2L}{(2-\overline{u}) \cdot N \cdot R} \cdot V_o & (15) \end{cases}$$

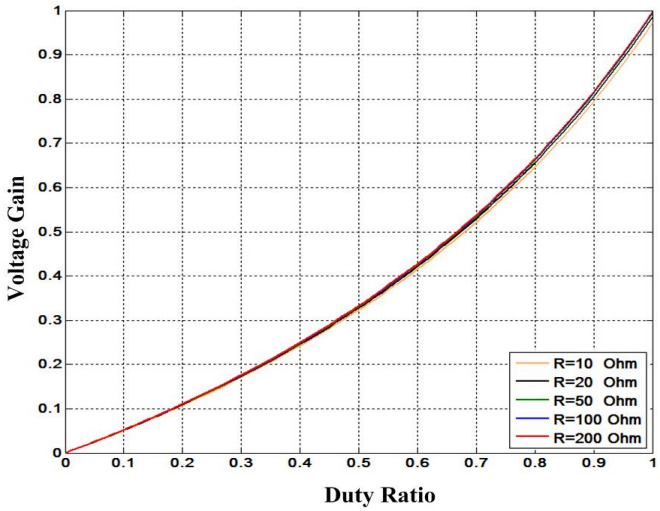
And the $\overline{i}_{in}$ is obtained as (16), (17) and (18)

$$\begin{cases} \overline{i}_{Lon} = \dfrac{N \cdot \overline{\varphi}}{2L} & (16) \\ \overline{i}_{Loff} = \dfrac{N \cdot \overline{\varphi}}{L} & (17) \\ \overline{i}_{in} = \overline{u} \cdot \overline{i}_{Lon} = \dfrac{\overline{u} \cdot N}{2L} \cdot \overline{\varphi} = \dfrac{\overline{u}}{(2-\overline{u})} & (18) \end{cases}$$

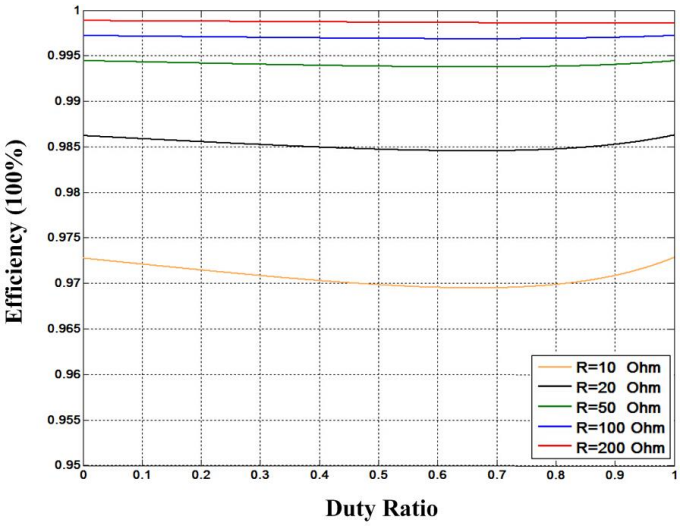
So the efficiency is (19)

$$\eta(\overline{u}) = \frac{V_o^2 / R}{V_{in} \cdot \overline{i}_{in}} = \frac{(2-\overline{u})^2}{\overline{u} \cdot X_1 \cdot (1/R) + 4(1-\overline{u}) \cdot X_2 \cdot (1/R) + (2-\overline{u})^2 \cdot R \cdot Y_1} \tag{19}$$

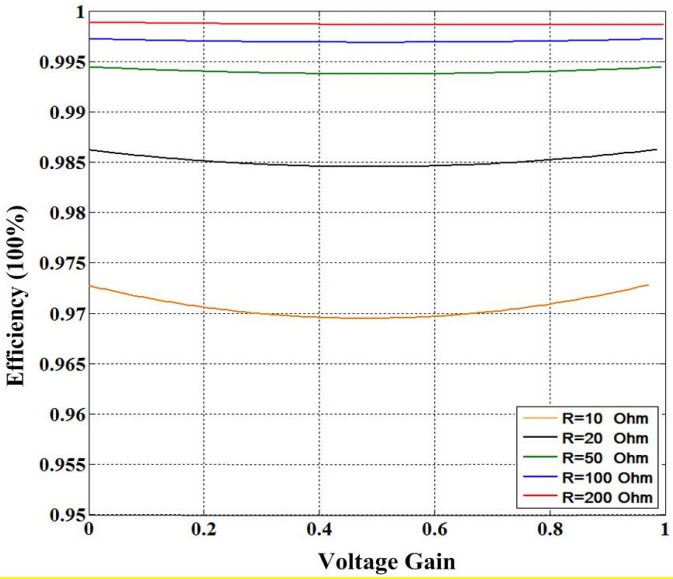
Fig.3 (a), (b) and (c) exhibit the voltage gain against duty ratio, the conversion efficiency with duty ratio and the relationship between voltage gain and conversion efficiency of buck converter, respectively.



(a) Voltage gain with duty ratio of tapped-inductor buck converter



(b) Conversion efficiency with duty ratio of tapped-inductor buck converter



(c) Comparison of the relationship between voltage gain and conversion efficiency

Fig.3. Characteristics of the Buck Converter

B. Boost Converter

Fig.4 shows a tapped-inductor Boost converter version. The switches S_1, S_2 and S_3 work in the similar pattern. S_1 is always maintained at on-state, when the S_2 is maintained at on-state, S_3 is off, the input voltage $V_{in}-V_o$ is developed across the inductor L in the N_1 side that causes the inductor current to increase, the load current is supplied by the capacitor C. When S_3 is maintained at on-state; S_2 is at off-state, the $V_{in}-V_o$ is developed across the tapped inductor causing an increase in current, i.e. capacitance C is under charging.

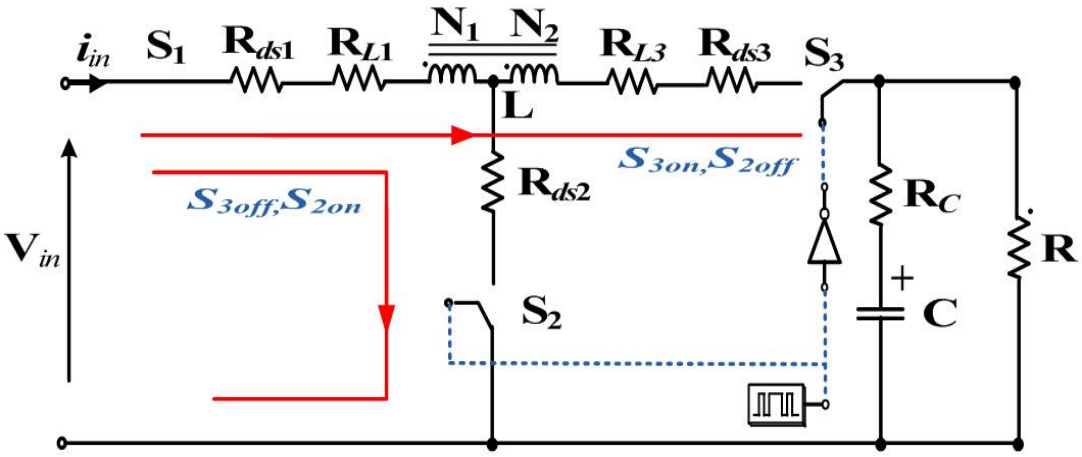


Fig.4 A new tapped-inductor Boost converter with parasitic components

Formulas (20) to (25) describe the model state of tapped-inductor buck converter with consideration of all parasitic resistors.

S_3 is in on-state, during S_{2on}, and S_{3off}

$$\begin{cases} i_{Lon} = \dfrac{N\cdot\varphi}{L} & (20) \\ \dot{\varphi} = \dfrac{V_{in}}{N} - \dfrac{R_L + 2R_{ds}}{L}\cdot\varphi & (21) \\ \dot{v}_c = -\dfrac{v_c}{C}\cdot Y_1 & (22) \end{cases}$$

S_3 is in on-state, during S_{3on}, and S_{2off}

$$\begin{cases} i_{Loff} = \dfrac{N\cdot\varphi}{L} & (23) \\ \dot{\varphi} = -X_2\cdot\dfrac{1}{L}\cdot\varphi - \dfrac{R}{N}\cdot v_c\cdot Y_1 & (24) \\ \dot{v}_c = \dfrac{N\cdot R}{L\cdot C}\cdot\varphi\cdot Y_1 - \dfrac{v_c}{C}\cdot Y_1 & (25) \end{cases}$$

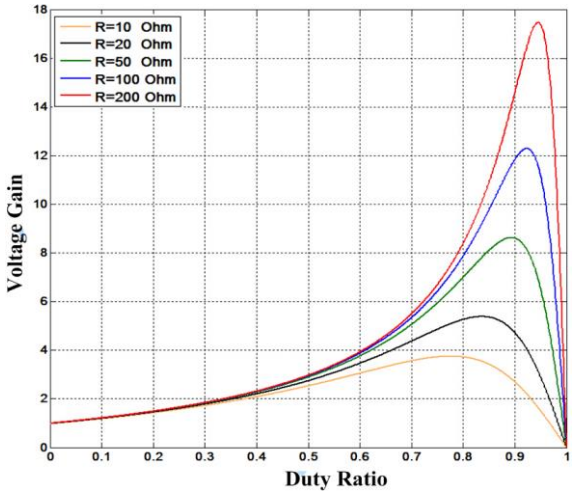
The voltage conversion ratio is then obtained as (26)

$$\xi(\bar{u}) = \frac{V_o}{V_{in}} = \frac{(1-\bar{u})\cdot(1+\bar{u})}{4\bar{u}\cdot\left((2R_{ds}+R_L)/R\right)+(1-u)\cdot X_1\cdot(1/R)+(1-\bar{u})^2\cdot R\cdot Y_1} \tag{26}$$

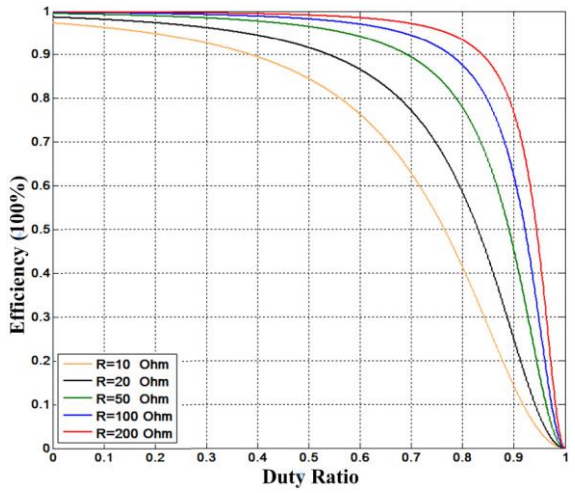
So the efficiency is then

$$\eta(\bar{u}) = \frac{V_o^2/R}{V_{in}\cdot\bar{i}_{in}} = \frac{(1-\bar{u})^2}{4\bar{u}\cdot\left((2R_{ds}+R_L)/R\right)+(1-u)\cdot X_1\cdot(1/R)+(1-\bar{u})^2\cdot R\cdot Y_1} \tag{27}$$

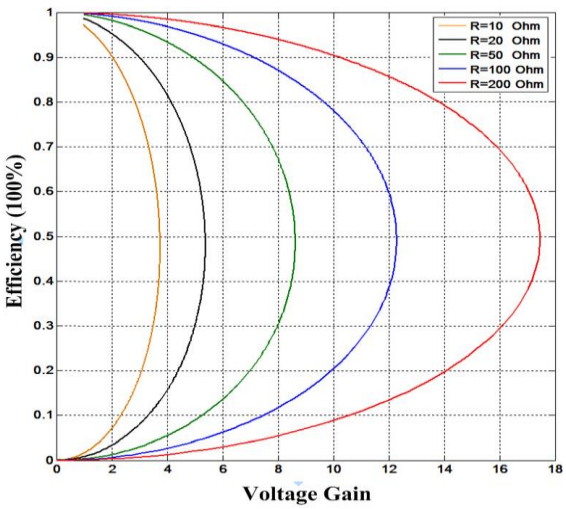
Fig.5 (a), (b) and (c) describe the voltage gain with duty ratio, the conversion efficiency with duty ratio and the relationship between voltage gain and conversion efficiency of boost converter, respectively.



(a) Voltage gain with duty ratio of tapped-inductor boost converter



(b) Conversion efficiency with duty ratio of tapped-inductor boost converter



(c) Comparison of the relationship between voltage gain and conversion efficiency

Fig.5. Characteristics of the Boost Converter

C. Buck-Boost Converter

Fig.6 shows a tapped-inductor Buck-Boost converter version. S_2 is always maintained at on-state, and the operation for S_1, S_3 and the inductor current are similar to Section A and *B* above.

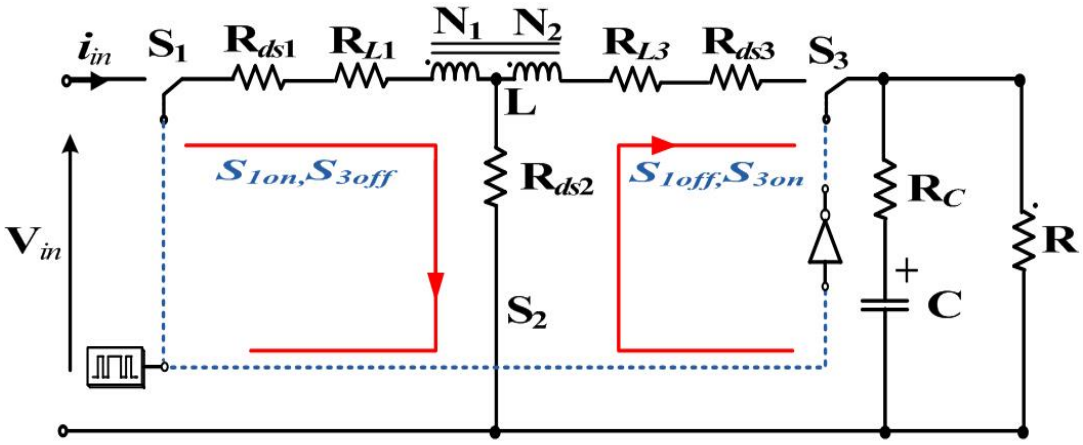


Fig. 6 A new tapped-inductor Buck-Boost converter with parasitic components

Formulas (28) to (33) again describe the model state of proposed buck-boost converter with parasitic resistors.

S_2 maintains on-state, during S_{1on}, and S_{3off}

$$\begin{cases} i_{Lon} = \dfrac{N \cdot \varphi}{L} & (28) \\ \dot{\varphi} = \dfrac{V_{in}}{N} - \dfrac{\left(R_L + 2R_{ds}\right)}{L} \cdot \varphi & (29) \\ \dot{v}_c = -\dfrac{v_c}{C} \cdot Y_1 & (30) \end{cases}$$

S_2 maintains on-state, during S_{3on}, and S_{1off}

$$\begin{cases} i_{Loff} = \dfrac{N \cdot \varphi}{L} & (31) \\ \dot{\varphi} = -X_2 \cdot \dfrac{1}{L} \cdot \varphi - \dfrac{R}{N} \cdot v_c \cdot Y_1 & (32) \\ \dot{v}_c = \dfrac{N \cdot R}{L \cdot C} \cdot \varphi \cdot Y_1 - \dfrac{v_c}{C} \cdot Y_1 & (33) \end{cases}$$

The average state-space formula is (34), (35)

$$\begin{cases} \dot{\varphi} = u \cdot \left(\dfrac{V_{in}}{N} - \dfrac{(2R_{ds} + R_L)}{L} \cdot \varphi \right) + (1-u) \cdot \left(-X_2 \cdot \dfrac{1}{L} \cdot \varphi - \dfrac{R}{N} \cdot v_c \cdot Y_1 \right) & (34) \\ \dot{v}_c = -\dfrac{u \cdot v_c}{C} \cdot Y_1 + (1-u) \cdot \left(\dfrac{N \cdot R}{L \cdot C} \cdot \varphi \cdot Y_1 - \dfrac{v_c}{C} \cdot Y_1 \right) & (35) \end{cases}$$

In steady-state

$$\dot{\varphi} = 0 \quad (36)$$

$$\dot{v}_c = 0 \quad (37)$$

The average output voltage

$$V_o = \overline{v}_o = \overline{v}_c \quad (38)$$

Integrating the formulas (34) (35) with (36) (37), respectively, we can get (39) (40) to represent V_{in} and v_c

$$\begin{cases} V_{in} = \dfrac{(1-u)^2 \cdot R^2 \cdot N \cdot \varphi}{u \cdot L} \cdot Y_1 + \dfrac{(1-u) \cdot N \cdot \varphi}{u \cdot L} \cdot X_2 + \dfrac{(2R_{ds} + R_c) \cdot N \cdot \varphi}{L} & (39) \\ v_c = \dfrac{(1-u) \cdot N \cdot R}{L} \cdot \varphi & (40) \end{cases}$$

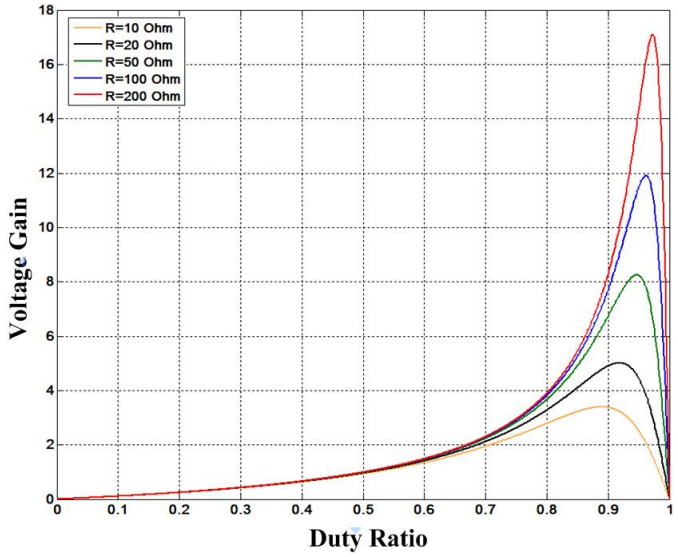
The voltage conversion ratio can be obtained as (41)

$$\xi(\overline{u}) = \frac{V_o}{V_{in}} = \frac{\overline{u} \cdot (1-\overline{u})}{\overline{u} \cdot \left((2R_{ds} + R_L)/R \right) + (1-\overline{u}) \cdot (1/R) \cdot X_2 + (1-\overline{u})^2 \cdot R \cdot Y_1} \quad (41)$$

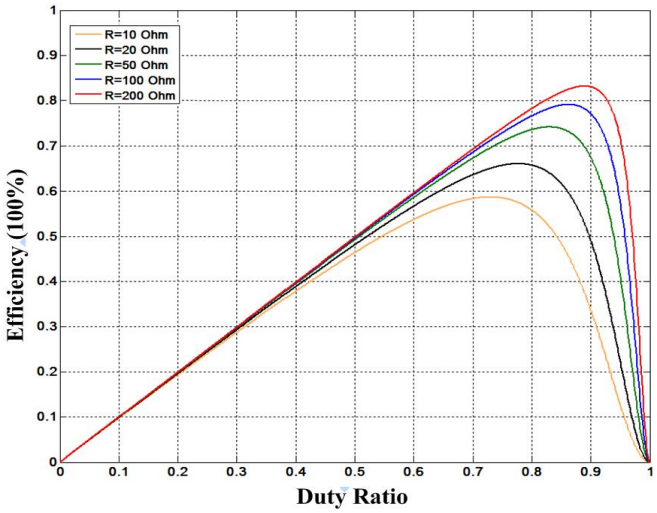
So the efficiency is (19)

$$\eta(\overline{u}) = \frac{V_o^2 / R}{V_{in} \cdot \overline{i}_{in}} = \frac{\overline{u} \cdot (1-\overline{u})^2}{\overline{u} \cdot \left((2R_{ds} + R_L)/R \right) + (1-\overline{u}) \cdot (1/R) \cdot X_2 + (1-\overline{u})^2 \cdot R \cdot Y_1} \quad (42)$$

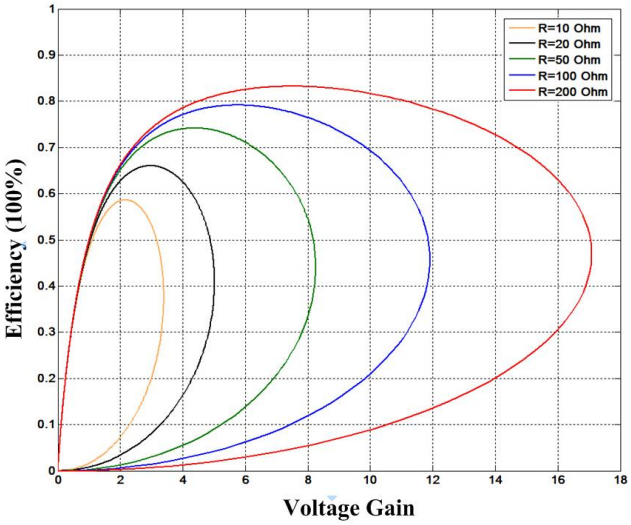
Fig.7 (a), (b) and (c) shows the voltage gain with duty ratio, the conversion efficiency with duty ratio and the relationship of voltage gain and conversion efficiency of tapped-inductor buck-boost converter, respectively.



(a) Voltage gain with duty ratio of tapped-inductor boost converter



(b) Conversion efficiency with duty ratio of tapped-inductor boost converter



(c) Comparison of the relationship between voltage gain and conversion efficiency

Fig.7. Characteristics of the Buck-Boost Converter

D. Switching loss and Magnetic loss

Except the conduction loss, there is two significant factors in the total power loss for tapped-inductor converter that cannot be ignored: switching loss and magnetic loss.

The size of passive components will be increased to reduce by the switching frequencies in the circuit of the converter. Therefore, the switching loss of MOSFET is a dominant parameter for the tapped-inductor converter. As we know, the junction temperatures and the efficiencies of converter could be predicted by the estimated MOSFET switching loss from the device datasheet. However, for the non-linear of MOSFET parasitic capacitance and traditional inductive load converters, the switching loss is too complex and difficult to analysis and estimate [22].

In the tapped-inductor converter, the switching loss will be calculated based on the processes of the charging and discharging of the capacitance of switched [23]. A commonly used equation for calculating the switching loss P_{SW_loss} is given by,

$$P_{SW\_loss} = f_{sw} C_{sw} V_D^2 \quad (43)$$

where f_{sw}, C_{sw}, V_D^2 are the switching frequency of the MOSFET, the output capacitance of the MOSFET and the voltage of the MOSFET increases from zero to V_D^2, respectively. However, f_{sw} and C_{sw} can be estimated form the datasheet of the MOSFET. Accordingly, V_D^2 is an only parameter need be calculated.

In the buck and boost mode, the V_{D_sw1} is equal to V_{D_sw3}, so the relationships of the V_{D_sw1}, V_{D_sw2} and V_{D_sw3} are given by,

$$V_{D\_sw1} = V_{D\_sw3} = (V_o + V_{in}) \quad (44)$$

$$V_{D\_sw2} = \left(\frac{V_o + V_{in}}{2}\right) \quad (45)$$

$$V_D = V_{D\_sw1} + V_{D\_sw2} \quad \text{Or} \quad V_D = V_{D\_sw3} + V_{D\_sw2} \quad (46)$$

So the switching loss P_{SW_loss} of the buck and boost converter is equal and which is given by,

$$P_{SW\_loss} = \frac{5}{4} f_{sw} C_{sw} (V_o + V_{in})^2 \quad (47)$$

From the above, we can see clearly that $V_o + V_{in}$ is an only influence factor on the switching loss in the converter. In other words, the parasitic elements have no relationships with switching loss. Therefore, firstly the parasitic elements of the tapped-inductor converter as the core have be explored and analyzed as in this paper, which is no impact on the power switching loss. Secondly, the all analyses and calculations of this paper are invented in the general condition, but only in the specific situation, according to the actual requirements of various converters, then the switching loss of MOSFET should be focused and calculated by the exact V_o and V_{in}.

The magnetic loss is also a complicated factor in the power electronics converter,

according to the turns of inductance coil winding, thickness of inductance coil winding, and the size of the inductive iron core, etc. As above discussed, in the different converters with actual requirements, the magnetic loss is also varied. Therefor in the general situation, the magnetic loss also does not need to be considered.

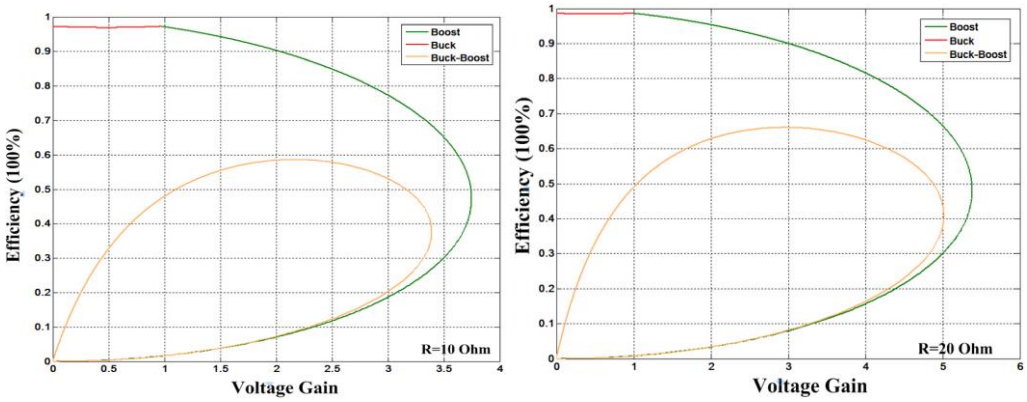
III. Comparison Of Voltage Conversion Ratio And power conversion Efficiency

A. Comparison of the Voltage Conversion Ratio and power conversion efficiency of tapped-inductor Buck, Boost and Buck-Boost converters

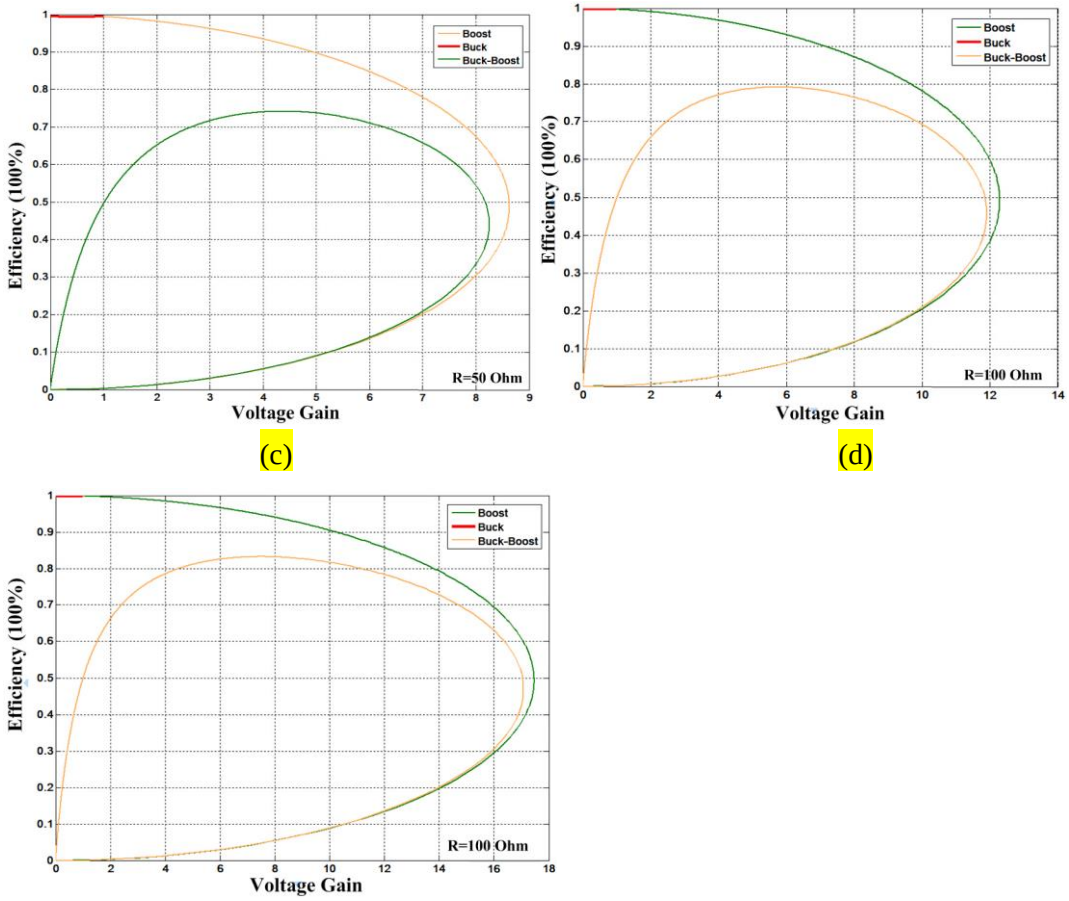
The voltage conversion ratio and power efficiency with different loads of the tapped-inductor buck, boost and buck-boost converters obtained above in Fig 3, 5 and 7 are analyzed. In the case of the voltage conversion ratio, it is obvious to see that the efficiency increases with the increase of the loads. However, In the case of the load, there are different variations in three modes. In the buck mode, with the increase of the voltage conversion ratio, the efficiency is decreased, and then increased. In the boost mode, the efficiency decreases with the increase of the voltage conversion ratio. In the buck-boost mode, with the increase of the voltage conversion ratio, the efficiency is increased, and then decreased.

B. Power conversion comparison with different loads in buck, boost and buck-boost modes

This simulation is conducted to analyze the proposed circuits in terms of the relationship between conversion efficiency and voltage gain. Five sets of resistances are used for the loads.



(a) (b)



(c) (d)

(e)

Fig.8. Power conversion comparison with different loads in buck, boost and buck-boost modes

(a) 10 Ω, (b) 20 Ω, (c) 50 Ω, (d) 100 Ω, (e) 200 Ω

Fig.8 shows the conversion efficiency comparisons among buck, boost and buck-boost modes in different loads. Firstly, no matter how the resistance and voltage gain change, buck mode maintains higher efficiency than 95%, also the range of voltage gain covers the whole range from 0 to1. Secondly, in boost mode, voltage gain and conversion efficiency becomes larger and higher respectively as the resistance increases, similar to the trend of change of the buck mode mentioned above. Lastly, buck-boost mode is not recommended due to its low conversion efficiency.

Consequently, the results review that the performance of buck mode and boost mode outweigh the buck-boost mode, in terms of the efficiency and the range of voltage gain. Therefore, the proposed converter is a promised candidate for its simple structure, also the integration of buck and boost converter shows splendid improvements in conversion efficiency.

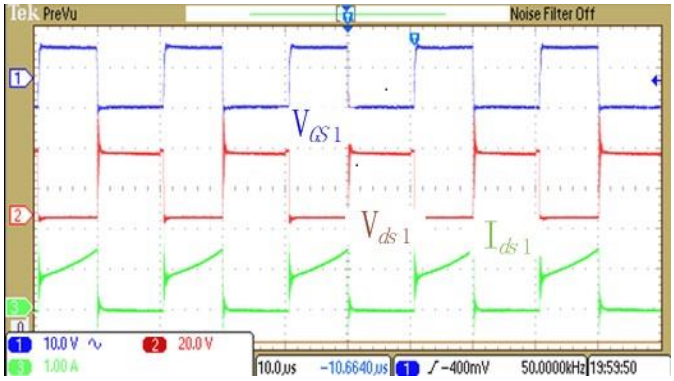
IV. EXPERIMENTAL RESULTS

A bidirectional WIWO tapped-inductor DC-DC converter has been built for the experimental verification. The parameters of experiment are shown in Table.3.

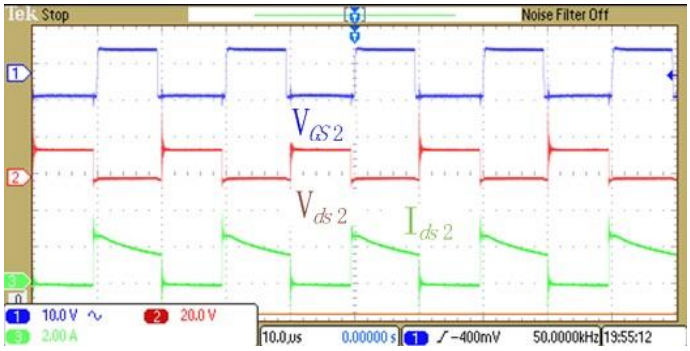
Table.3 Parameters of experimental setup

Duty Ratio	0.2-1
Load R	5 Ω (buck) and 50 Ω (boost)
Switching Frequency	50 kHz
Total Inductance	509μH
Transistor Side Inductance	128μH
Secondary Side Inductance	128μH
Input Voltage of Converter	5-24V

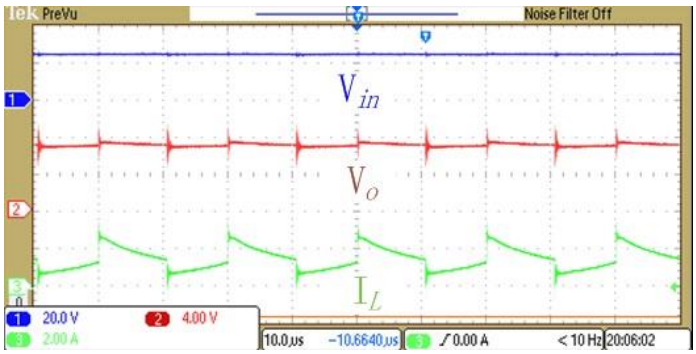
Firstly, in buck mode, the input voltage is constant at 24V controlled by three IRF541 MOSFETs, and one of them is kept to be open states, the waveforms of experiment are shown in Fig.9 (a), (b) and (c).



(a) Top trace: gating voltage of S_1 switch (10us/15V/div); middle trace: drain voltage of S_1 switch (10us/25V/div); bottom trace: current of S_1 switch (10us/1.5A/div)



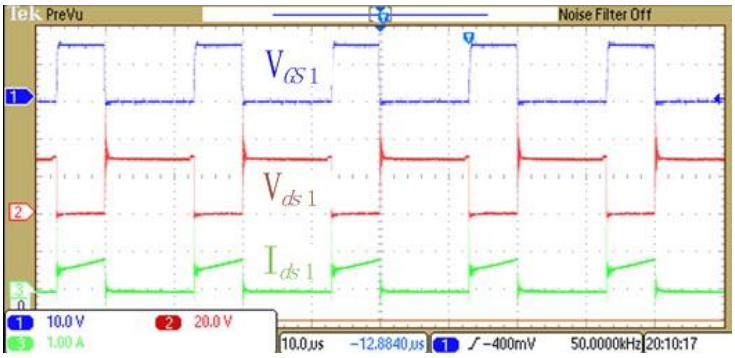
(b) Top trace: gating voltage of S_2 switch (10us/12V/div); middle trace: drain voltage of S_2 switch (10us/18V/div); bottom trace: current of S_2 switch (10us/2.2A/div)



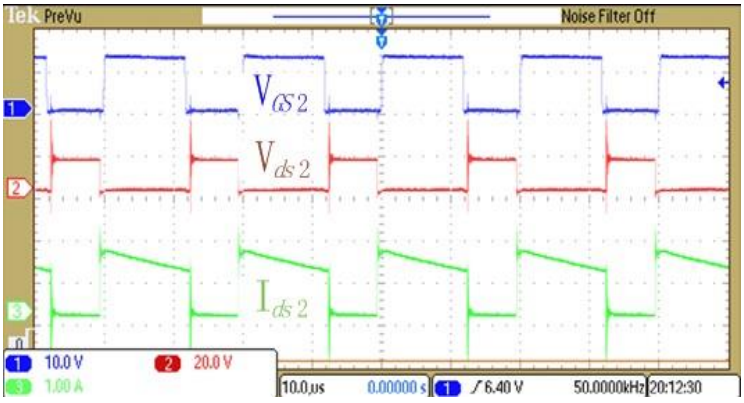
(c) Top trace: input voltage (10us/24V/div); middle trace: output voltage (10µs/7V/div); bottom trace: current of inductor L (10us/2.4A/div)

Fig.9. Measured waveforms of experimental of buck converter (a) S_1 switch, (b) S_2 switch, (c) V_o, V_{in}, I_L

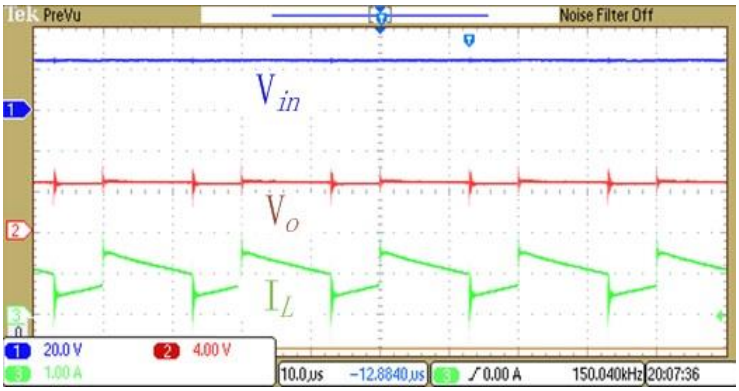
Fig.9 (a) is the measured waveforms of MOSFET S_1, V_{GS1} is the gating voltage, V_{ds1} is drain voltage and I_{ds1} is the current. The waveforms of MOSFET S_2 are similar to MOSFET S_1 above as shown in (b), and (c) that are input voltage, output voltage, and current of tapped-inductor. Significantly, keeping the input voltage to be 24V and output voltage to be 5V, the measured waveforms of buck converter are shown in Fig.10 (a), (b) and (c). When the load is 5 Ω, the duty ratio is then varied to maintain the output voltage to be 5V.



(a) Top trace: gating voltage of S_1 switch (10µs/15V/div); middle trace: drain voltage of S_1 switch (10us/24V/div); bottom trace: current of S_1 switch (10µs/0.8A/div)



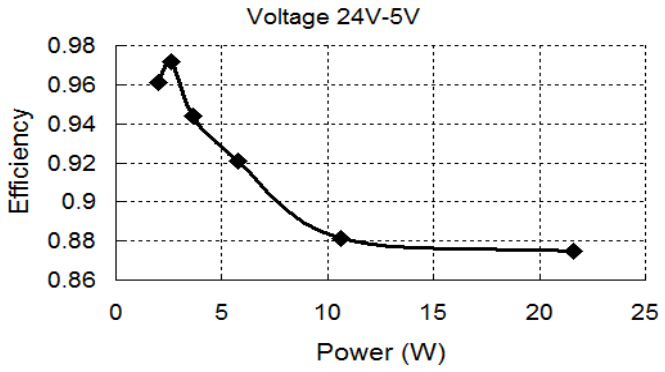
(b) Top trace: gating voltage of S_2 switch (10µs/12V/div); middle trace: drain voltage of S_2 switch (10us/28V/div); bottom trace: current of S_2 switch (10µs/1.8A/div)



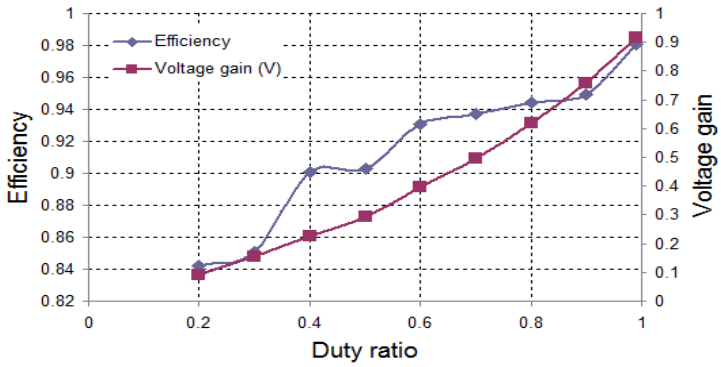
(c) Top trace: input voltage (10μs/24V/div); middle trace: output voltage (10μs/5V/div); bottom trace: current of inductor L (10μs/1.5A/div)

Fig.10. Measured waveforms of experimental results of 24-input and 5V-output voltage buck converter. (a) S1 switch, (b) S2 switch, (c) V_{in}, Vo, I_L

And then the relationship of conversion efficiency and output power is shown is Fig.11 (a). The relationship of duty ratio, conversion efficiency and voltage gain is shown in Fig.11 (b).



(a) The relationship of conversion efficiency and output power

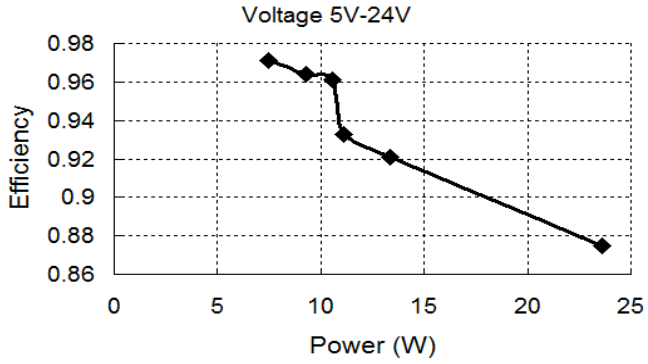


(b) Relationship of duty ratio, conversion efficiency and voltage gain

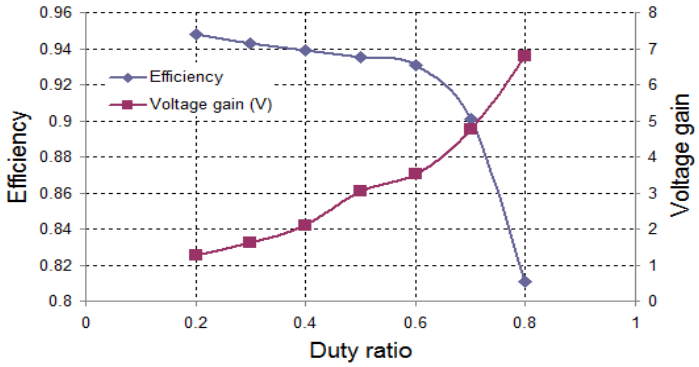
Fig.11. Experimental results of the Buck mode

As it is shown in Fig.11 (a) (b) and Fig.3 (a) (b), the conversion efficiency is increased with the duty ratio and voltage gain increase. Therefore, the trend and direction of the analysis are similar to the results of experiment approximately, so the characteristics of the preferred WIWO buck converter have been verified.

Secondly, in boost mode, the input voltage is kept at 5V and the output voltage is then 24V, with the load to be 50 Ω, the duty ratio is adjusted to keep the output voltage to be 24V. The corresponding measured relationship between conversion efficiency and output power is shown is Fig.12 (a). The corresponding relationships of duty ratio, conversion efficiency and voltage gain are shown in Fig.12 (b).



(a) Measured the relationship of conversion efficiency and output power



(b) Measured the relationship of duty ratio, conversion efficiency and voltage gain

Fig.12 Measured result of the Boost mode

Comparing the Fig.12 (a) (b) with Fig.5 (a) (b), the conversion efficiency improves as the duty ratio decreases whereas as voltage gain increases with the duty ratio increases. Therefore, the trend and direction experimental results agree with the analysis mainly. The boost mode operation of the proposed converter gives superior topology variation structure, and advantages of characteristics have been confirmed with experiment.

The achievements of experiment have shown that the converter has higher conversion efficiency than classical converter. Even the duty ratio reduces to 0.2 or increases to 0.8. Therefore a wide range of the voltage conversion is now feasible. However, the experimental error is difficult to avoid, because of the precision of the inductance coil winding or the losses of the circuit connection, etc. So the direction and trend of the results of analysis and experiment should be compared as the key.

V. CONCLUSIONS

This paper has proposed a new wide-input-wide-output converter topology, which is integrated with buck and boost modes with a tapped-inductor. The circuit development started with a synchronous MOSFET to reduce the losses of conduction effectively and reduce the voltage spike. The modified topology is then accomplished, which consists of three MOSFETs and a tapped-inductor to realize a unified topology that is able to work under buck, boost and buck-boost modes. Two MOSFETs are activated to operate complementary to realize the directional power flow.

The analysis in both theoretical and simulation has been conducted to study correlation among the ratio, conversion efficiency and voltage gain. The comparisons between duty ratio and conversion efficiency, and the other are about conversion efficiency under load variation. In boost mode, the conversion efficiency is increased as output power reduces, but the conversion efficiency and voltage gain are increased with increasing duty ratio. The preferred range of duty ratio is from 0.2 to 0.8. In buck mode, the conversion efficiency is similar to the boost above, but the conversion efficiency increases with the duty ratio increasing and the preferred range of duty ratio is from 0.2 to 1. Compared with conventional converter, the conversion efficiency of the proposed converter is higher, especially when the duty ratio is less than 0.2 or greater than 0.8.

Finally, the correctness of theory and the effectiveness of new circuit topology have been verified by experiment. The improvements of proposed WIWO converter are the wider conversion range of voltage and higher power conversion efficiency up to 95%. Application of the converter can be used in the charging for super-capacitor due to its wide range of operation.

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The Answer Sheet

Editors:

Comments to Authors:

We noticed that your manuscript is covering a topic that has been widely addressed in our journal. We would therefore like to ask you to update your references with a significant number of the latest (years 2013 to 2015) relevant papers from the IET Power Electronics Journal.

Z.H. Shi, K.W.E. Cheng, S.L.Ho, 'Static performance and parasitic analysis of tapped-inductor converters', IET, Power Electronics, vol:7, no 4, February 2014,pp.366 - 375

Associate Editor

Comments to Author:

The switching and magnetization losses have not been considered in this work. These are fundamental to the operation and key contributors to loss in power switching circuits. These must be included in the next revision.

Reply :- The question has been answered in the paper from p12-14.

Reviewer: 1

Comments to the Author

Please see the pdf file attached, just some minor comments. I am not too much into tapped inductor converters, therefore I cannot give too much advices.

Reply :- The questions have been revised in all the paper.

Reviewer: 2

Comments to the Author

This paper analyzes the efficiency vs. gain optimization for a tapped-inductor converter which can be performed in Buck, Boost and Buck-boost modes. The reviewers thought the several important issues should have been considered:

1. The model only consider the losses of the equivalent series resistances of branches . However the main losses of the power electronic converters are the switching loss during the switches are turning on and off, as well as the magnetic loss in the inductor. There two main factors are not considered;

Reply :- The question has been answered in the paper from p13-14.

2. The author might have through that the switching losses and magnetic losses could be estimated. However, the truth is that they are rather complicated because they are dependent on the shapes of the voltage and current. Therefore they cannot be eliminated. However in Fig. 3, the variation of load has almost no impact on the efficiency, this is beyond the reviewer's understanding.

Reply :- In Fig.3 is shown in:

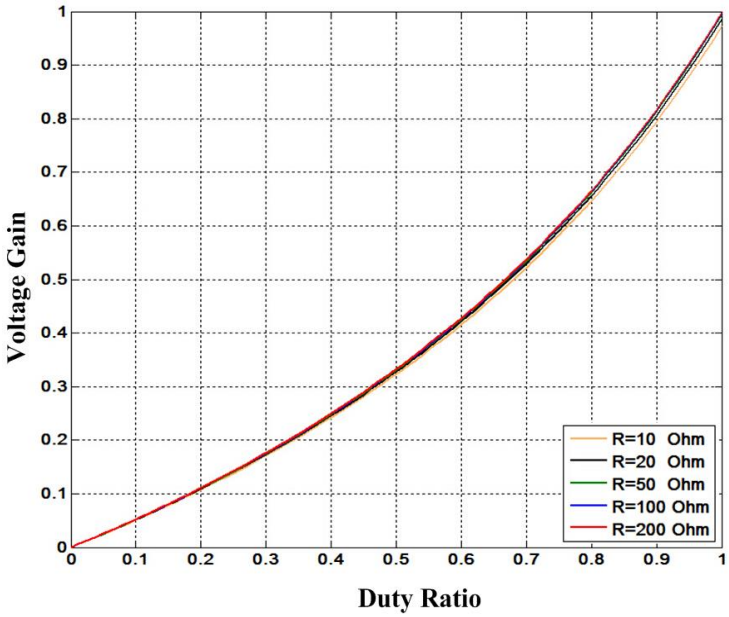

Fig.3 (a)

The Fig.3 (a) has described the relationship of the voltage gain with duty ratio of tapped-inductor buck converter. There is not the efficiency. However, the Fig.3 (b) and (c) have shown the relationships of the efficiency with duty ratio and voltage gain. We can see clearly that the variation of load has impact on the efficiency.

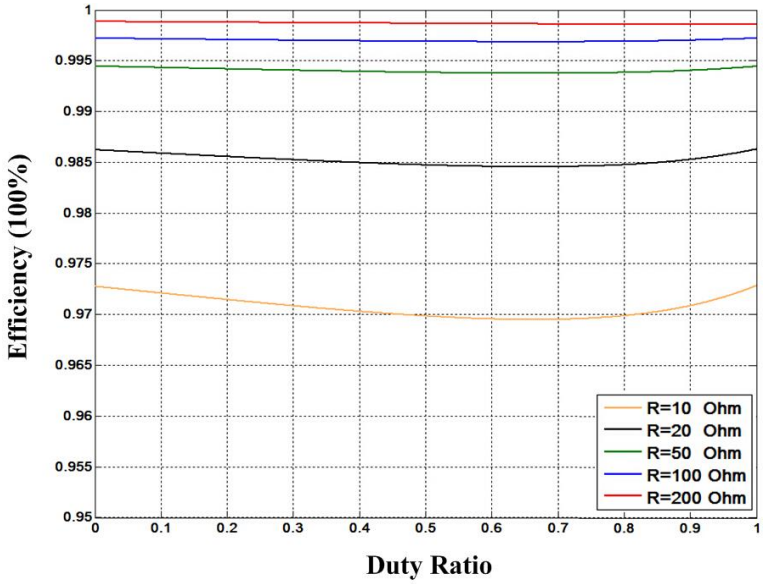

Fig.3 (b)

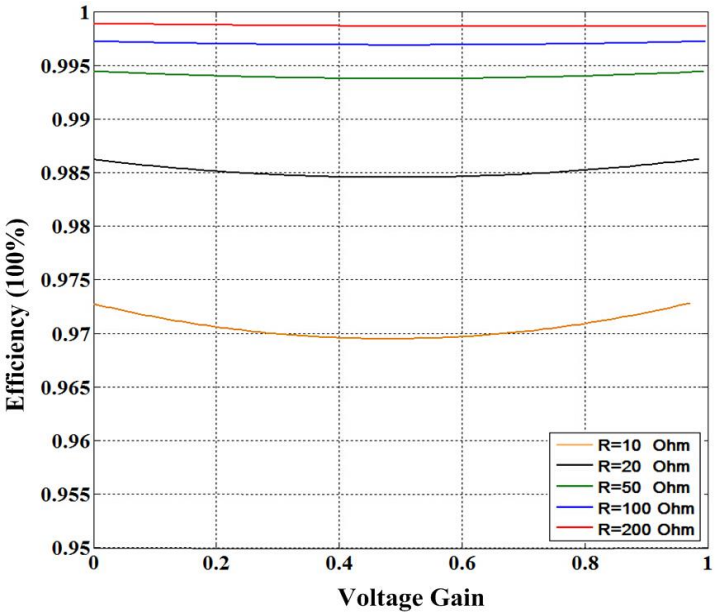

Fig.3 (c)

3. Some conclusions given in the manuscript are the well-known knowledge, for example Table 2.

Reply :-The Table 2 has been deleted.

4. The experimental results in Fig. 9 and 10 are the detail and switching-period waveforms which are used to verify the availability of the topology design. They cannot verify the analysis presented in this paper.

Reply :- In this paper, it is significant to analyze the influences of the parasitic elements in the tapped-inductor converter in the generalized situation, therefore the input/output voltage has not been assigned the values in the analyses and calculations in the circuit description as shown in Fig.11 and Fig.12. The analysis has been verified in the experimental results

5. The efficiency performances between the analysis and experiments should be given. And it seems that, in the current version, they are not matched very well.

Reply :- There are many possibilities will lead to the problem, for example, the precision of the inductance coil winding, the losses of the circuit connection, and the unreasonable experimental device selection, etc.

In my opinion, the error in the process of the experiment that should be ignored, if the trend and direction of the analysis has been verified by the experimental results yet.