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Steep Slope p-type 2D WSe_2 Field-Effect Transistors with Van Der Waals Contact and Negative Capacitance

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Abstract - Steep-slope p-type 2D WSe_2 back-gated field-effect transistors (FETs) are realized by using van der Waals Pt-WSe_2 contact and $HfZrO_2/Al_2O_3$ as the dielectric layer. The van der Waals Pt-WSe_2 contact is free from disorder and Fermi level pinning and decreases the sub threshold slope. The WSe_2 NCFET with van der Waals contact shows low subthreshold slope for both forward and reverse gate voltage sweep (the minimum $SS_{forward}$ = 18.2 mV/dec and $SS_{reverse}$ = 44.1 mV/dec) with a hysteresis as small as 20 mV at sub threshold region.

I. Introduction

With the scaling of the MOSFET, efficient gate control and ultra-thin body is needed to reduce the power consumption and the subthreshold slope (SS) [1]. Recently CMOS compatible HZO was used in NCFET to achieve efficient gate control and SS less than 60 mV/dec [2-5]. Two dimensional (2D) transition metal dichalcogenides (TMDs) are semiconductors with ultrathin body and are considered promising candidates for future low power electronics [5-8]. Tungsten diselenide (WSe_2) has balanced conduction and valence band edges, providing an appropriate channel material for realizing complementary FETs [5-6]. However pristine multilayer WSe_2 FET usually shows ambipolar behavior and large Schottky barrier [5, 6]. The incomplete covalent bond at the contact region leads to surface states in the bandgap and result in Fermi level pinning effect. The disorder at the interface influences the band alignment of the metal/semiconductor and increase the contact resistance [7, 9]. The Schottky barrier reduce the on-state current and the contact gating phenomenon significantly affects the carrier injection, which result in a large SS at the sub threshold region [7-9]. In this way reducing Schottky barrier is of significant to fabricate WSe_2 device with small SS.

In this work, we fabricated a steep slope p-type WSe_2 FETs with van der Waals (vdWs) Pt contact and HZO/Al_2O_3 gate stack. The vdWs metal/semiconductor contact enables an interface without chemical bonding and disorder [7]. The electrical contact without Fermi level pinning reduces the Schottky barrier and the sub threshold slope. With HZO/Al_2O_3 gate stack, sub thermionic SS for both forward and reverse gate voltage sweep is obtained with minimum $SS_{forward}$ = 18.2 mV/dec and $SS_{reverse}$ = 44.1 mV/dec. The drain current can be modulated by 5×10^4 within 220 mV, making it promising for low power device applications.

II. Fabrication of Devices

Fig. 1 is the schematic illustration of the fabrication process flow. We prepared 30-nm-thick Pt electrode on a Si substrate using standard photolithography and electron-beam lithography. The deposition rate is set to be 0.1 Å/s. Dry transfer method was applied to fabricate the van der Waals contact to 2D materials. A PVA film was used to mechanically peel the electrodes from the Si substrate. The temperature was set to be 55 °C for 3 min to avoid strong interaction between the electrode and the Si substrate. The PVA film was attached to a PDMS stamp together with the electrode. The PDMS stamp was then attached to a glass and then an 2d material transfer platform WSe_2 flakes (~ 10 nm) were mechanically exfoliated onto the substrate using scotch tape. After we aligned the electrode and the WSe_2 flake, the PVA thin film with electrodes was physically contacted to the WSe_2 flake. After the heat treatment, the PVA film was washed away with deionization water and isopropanol.

Atom layer deposition (ALD) was used to deposit HZO film on p++ silicon at 180 °C. We used tetrakis (dimethylamido) hafnium as Hf source, tetrakis (dimethylamido) zirconium as Zr source and H_2O as oxidant. The HfO_2/ZrO_2 ratio was controlled to be 1:1. For capacitance matching and gate leakage reduction, 4-nm-thick Al_2O_3 was deposited by using trimethylaluminium as Al source and H_2O as oxidant. A rapid thermal annealing in nitrogen environment was performed to crystallize the HZO and enhance the ferroelectricity.

III. Van Der Waals Contact

We fabricated the Pt contact electrode by using photolithography and electron beam evaporation. Fig. 2 shows the transfer characteristics of a typical WSe_2 FET on 15 nm ZrO_2 with the V_{ds} from - 0.1 V to - 1.0 V at room temperature. Obviously, the device shows an ambipolar transport behavior. Its p-branch current is almost 3 orders of magnitude larger than that of the n-branch. Fig. 3 is the corresponding output characteristics of the WSe_2 device. The I_d-V_{ds} exhibits

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nonlinear behavior at the low V_{ds} region, indicating a relative high Schottky barrier Φ_p for holes [8, 9].

For the WSe_2 devices with transferred vdWs Pt electrode, its transfer curve is given in Fig. 4. The ambipolar effect is greatly suppressed. The p-branch is enhanced while the n-branch vanishes, indicating a higher barrier Φ_n for electron and reduced Schottky barrier Φ_p for hole [7, 8]. Fig. 5 shows the corresponding output characteristics of the device with vdWs contact. The linear behavior of the output curve indicates small barrier between the Pt electrode and the valence band of WSe_2. With reduced hole Schottky barrier, the SS is also greatly decreased. Fig. 6 shows the point SS versus I_d of the devices. The average SS of the FETs with vdWs Pt is 134 mV/dec; while the device with the evaporated Pt electrode exhibits a SS of 226 mV/dec. The SS in the low current region is similar; while in the high current region, the devices with vdWs contact show much smaller SS than that with the evaporated electrode. The device with vdWs contact exhibits minimum forward $SS_{forward}$ = 96 mV/dec and reverse $SS_{reverse}$ = 71 mV/dec, as shown in Fig. 7. The point SS analysis is given in Fig. 8. Fig. 9 is the transfer characteristic of a WSe_2 FET with transferred Au electrode. The device shows significant ambipolar behaviors. The nonlinear behavior of the output characteristics at the low V_{ds} region indicating that the Fermi level of Au electrode lies in the middle of the WSe_2 band gap, and Schottky barrier exists for both electron and hole (Fig. 10). Compared with vdWs Au, vdWs Pt is more suitable for a p-type contact.

Fig. 11 (a) illustrates the simplified band diagrams of the FETs with evaporated and transferred Pt electrode. Fig. 12 is the corresponding transfer curve. In the thermionic region ($|V_{gs}| < |V_{fb}|$), the band position changes equivalent to V_{gs} (irrespective of depletion and interface trap capacitance) [8, 10]. The slope is given by $SS = k_bT/q \cdot \ln 10 = 60$ mV/dec, which is the thermionic limit. When $|V_{fb}| < |V_{gs}| < |V_{th}|$, the tunneling barrier decreases the current and the Slope is given by $SS = \eta k_bT/q \cdot \ln 10$ (η is the ideal factor related to barrier width, $\eta > 1$), which is larger than in the thermionic region. With smaller SB height, the V_{fb} will be close to V_{th} and the tunneling region is reduced, thus result in a larger magnitude within all the sub threshold region (Fig. 12), which is the key factor in low power electronics. This phenomenon is also observed in Fig. 6. The SS in both cases are small in low current region. With high current, the devices with vdWs electrode maintain a smaller SS, while the evaporated one start to increase.

IV. NEGATIVE CAPACITANCE GATE

Then we use negative capacitance gate to further reduce the SS. Fig. 13 is the high angle annular dark field scanning transmission electron microscopy (HAADF-STEM) image and the energy dispersive spectrum (EDS) of the NCFET gate stack, confirming the element distribution. High-resolution cross-sectional TEM image clearly reveals the structure of the $HZO/AlO_x/WSe_2$ stack with clean interfaces. After the annealing process at 450 °C, the HZO layer is highly crystalline, as shown in Fig. 14 (a). Benefiting from the vdWs contact, the transferred metal/WSe_2 junctions feature an atomically sharp and clean interface within a few angstrom (Fig. 14 (b)). For the deposited metal/TMD junction, there are considerable defects, strain and disorder at the interface [7]. These interfacial defects cause metal-induced gap states and interfaces dipoles and influence the Schottky barrier [7, 9].

Fig. 15 is the polarization versus electric field hysteresis loop of the HZO film. After the annealing at 450 °C, the transition from dielectric to ferroelectric characteristics is clearly observed (measured at 1 kHZ). Fig. 16 is the transfer characteristics of the WSe_2 NCFET with van der Waals contact. The device exhibits minimum forward $SS_{forward}$ = 44 mV/dec and reverse $SS_{reverse}$ = 18 mV/dec. The $SS_{forward}$ and $SS_{reverse}$ is given in Fig. 17. The drain current can be modulated by 5×10^4 within 220 mV, which is among the smallest in published NCFETs, especially for p-type FET. Fig. 18 is the transfer characteristics with various V_{ds} from - 0.1 V to - 0.5 V. The DIBL is observed, the shift is calculated to be 200 mV/V. The DIBL effect conclusively confirm the realization of negative capacitance effect in this gate stack [3, 5]. Fig. 19 is the output characteristics of the NCFET. The output characteristics of the NCFET shows good saturation at V_{ds} = 1 V.

Fig. 20 is the on state current versus on/off ratio at $V_{dd} = V_{ds} = V_{gs}(on)-V_{gs}(off)$ of the WSe_2 devices with negative capacitance gate. At V_{dd} = 0.5 V, the WSe_2 devices exhibit the on/off ratio over 10^5, which is much better than that of the device with ZrO_2 ones (Fig. 21). Compared with previous works, the performance of our NCFET is outstanding, especially for p-type NCFETs. The device can achieve 5×10^4 modulation within 220 mV, among the best devices in published p-type NCFETs [2-5].

V. CONCLUSION

In summary, we fabricated WSe_2 NCFET devices with HZO/AlOx gate stack. Van der Waals Pt contact is used to reduce the fermi level pinning at the metal/WSe_2 interface. This fermi level pinning free contact turns an ambipolar FET into a unipolar one and reduce the SS. With HZO/AlO_x gate stake SS less than 60 mV/dec is obtained (minimum 18.2 mV/dec) and the hysteresis in the sub threshold region is as small as 20 mV. Moreover the device can be modulated by 5×10^4 within 220 mV, which makes it a promising candidate in ultra-low power electronics.

ACKNOWLEDGMENT

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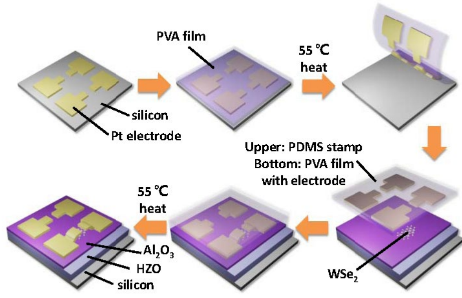


Fig 1. Transfer process flow of the van der Waals contact.

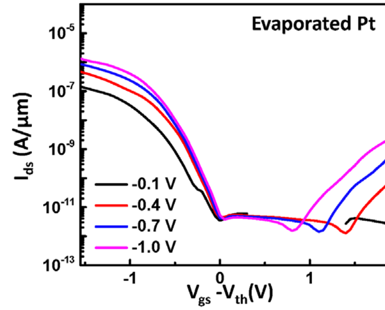


Fig 2. Transfer characteristics of the WSe_2 FET evaporated Pt electrode. The device shows ambipolar behavior. Channel length is 5 μm. Channel thickness is 10 nm.

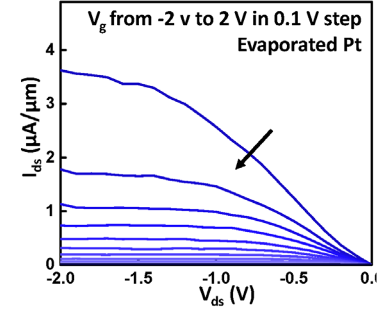


Fig. 3. Output characteristics of the WSe_2 FET evaporated Pt electrode. The output curve is nonlinear at small bias, indicating Schottky contact.

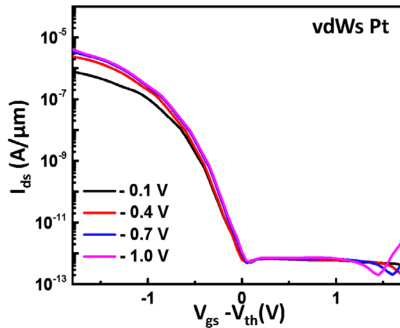


Fig. 4. Transfer characteristics of the WSe_2 FET with transferred vdWs Pt electrode. The device shows unipolar p type behavior. Channel length is 5 um.

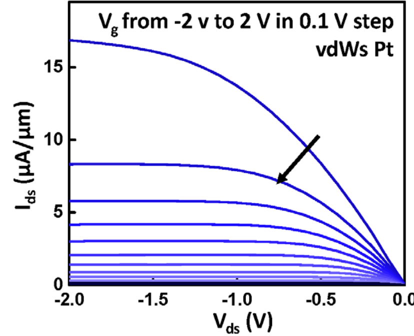


Fig. 5. Output characteristics of the WSe_2 FET with van der Waals Pt electrode. The output curve is nonlinear at small bias.

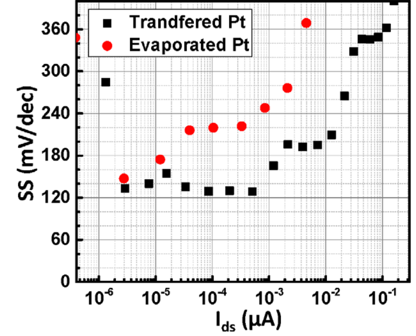


Fig. 6. Point SS of the WSe_2 FET with evaporated and transferred vdWs Pt electrode. The SS is similar in low current region and changes at higher current.

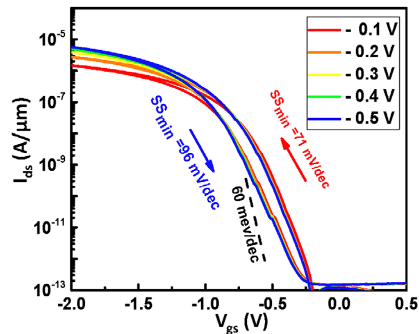


Fig. 7. Transfer characteristics of the WSe_2 FET transferred vdWs Pt electrode with minimum SS.

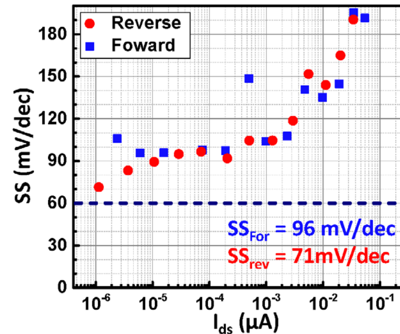


Fig. 8. Point SS of the WSe_2 FET with vdWs Pt electrode.

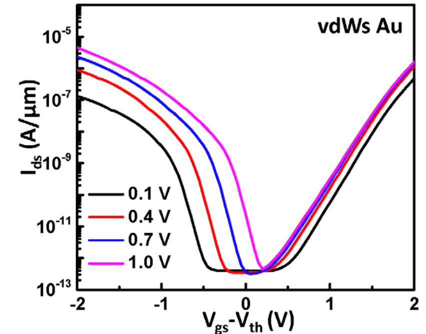


Fig. 9. Transfer characteristics of the WSe_2 FET with vdWs Au electrode. Channel length is 5 um.

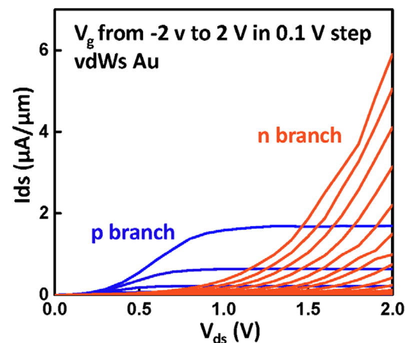


Fig. 10. Output characteristics of the WSe_2 FET with vdWs Au electrode.

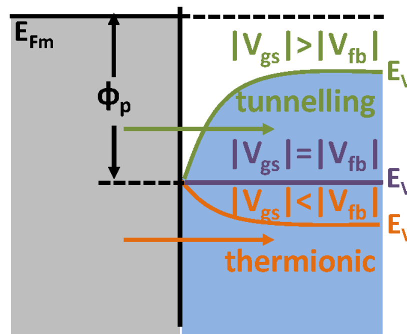


Fig. 11. Simplified band diagram of the FET with evaporated and transferred vdWs Pt electrode.

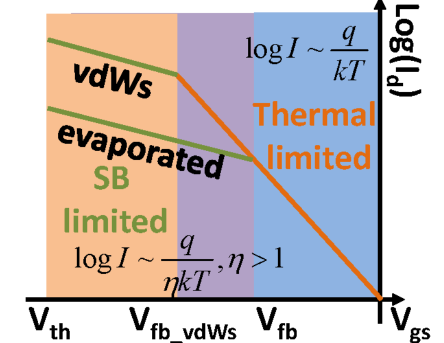
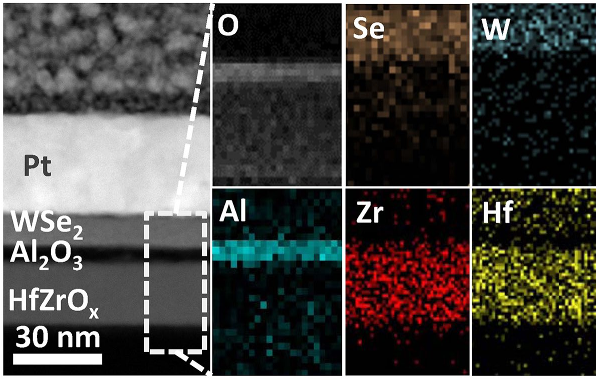


Fig. 12. Corresponding transfer curve of the FET for evaporated and vdWs Pt electrode.



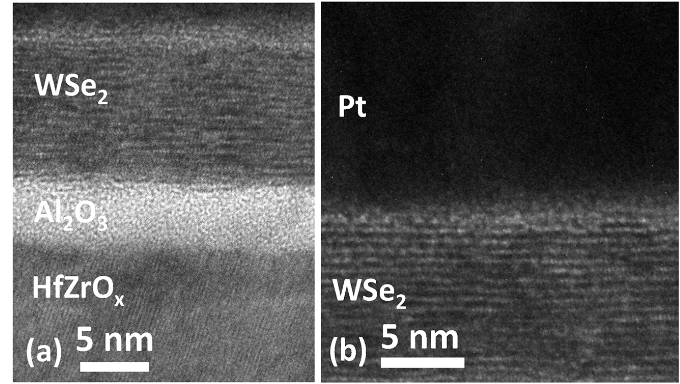


Fig. 13. (a) HAADF-STEM image of the WSe_2 NCFET and (b) EDS mapping of the element distribution within the marked region. Please leave some space between TEM images

Fig. 14. (a) High-resolution TEM of the gate stack of a WSe_2 NCFET. The HZO is highly crystallized. (b) Interface of the Pt/WSe_2 contact region.

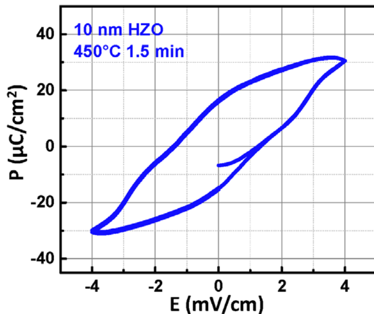


Fig. 15. P-E lop of HZO stack. Describe sth. Do we have PFM image?

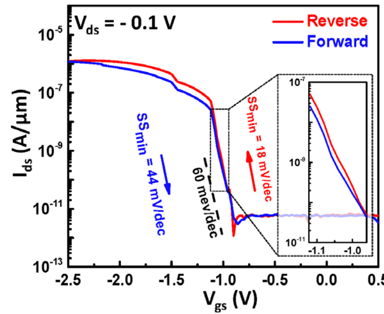


Fig. 16. Transfer characteristics of the WSe_2 NCFET with vdWs Pt electrode.

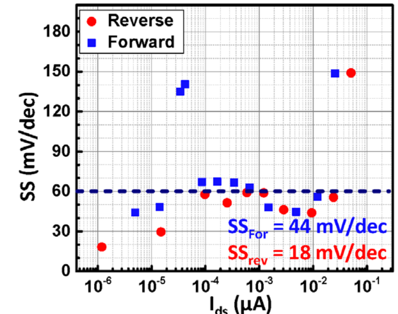


Fig. 17. Point SS of the WSe_2 NCFET with transferred vdWs Pt electrode.

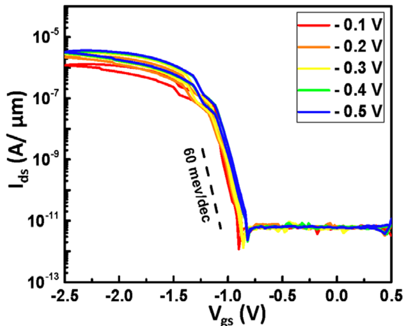


Fig. 18. transfer characteristics of the vdWs contact WSe_2 NCFET with various V_{ds} from -0.1 V to -0.5 V. DIBL is observed with 200mV/V.

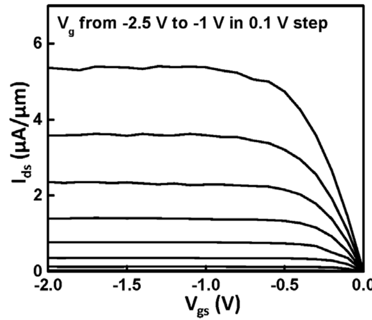


Fig. 19. Output characteristics of the vdWs contact WSe_2 NCFET. The output curve shows linear behavior at small bias.

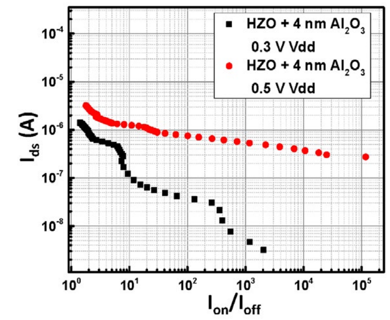


Fig. 20. On state current versus on/off ratio at $V_{dd} = V_{ds} = V_{gs}$ (on)-V_{gs} (off) of the WSe_2 NCFET.

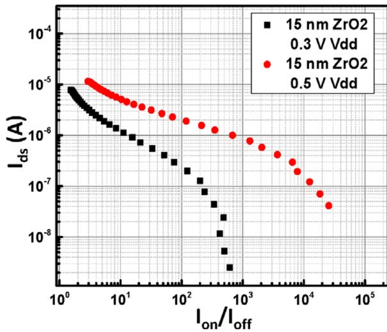


Fig. 21. On state current versus on/off ratio at $V_{dd} = V_{ds} = V_{gs}$ (on)-V_{gs} (off) of the WSe_2 FET on ZrO_2.

Table.1 comparison of this work with published NCFET devices

Device type	**Minimum SS**	**Hysterysis**	**Drive magnitude**
HZO MoS_2 n-NCFET [3]	23 mV/dec	24 mV	232 mV for 10^5
PZT, Si n-NCFET [2]	32 mV/dec (forward), 13 mV/dec (reverse)	10 V	2.15 V for 10^5
HZO.Ge&GeSn p-NCFET [4]	47 mV/dec (foward), 43 mV/dec (reverse)	40 mV	~ 0.3 V for 10^3
HZO with MIG, WSe_2 p-NCFET [5]	41.2 mV.dec (forward) 14.4 mV/dec (reverse)	120 mV	650 mV for10^5
This work	44.1 mV/dec (forward), 18.2 mV/dec (reverse)	20 mV	220 mV for $5*10^4$