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Recent Progress in Printable Organic Field Effect Transistors

Wei Tang,^{a,b} Ruili Liu,^a Yuezeng Su,^a Xiaojun Guo,^{a*} and Feng Yan^{b*}

^{*a*} Department of Electronic Engineering, School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China ^{*b*} Department of Applied Physics, The Hong Kong Polytechnic University, Kowloon, China

* To whom correspondence should be addressed.

* E-mail: x.guo@sjtu.edu.cn (X. Guo), apafyan@polyu.edu.hk (F. Yan).

Abstract

Printable organic field effect transistors (OFETs) have been investigated for more than 20 years, aiming at various emerging applications including flexible/wearable electronics, displays and sensors. Since many comprehensive review articles for this field have been published, here we will focus on the recent progress of this field and address the following issues critical to the future applications of OFETs. First, the technologies for the printing of OFETs with fine resolution will be reviewed. The approaches for short channels and small overlapping as well as patterning of organic semiconductors are summarized. Second, various approaches for preparing low-voltage OFETs will be presented, which are important for realizing low power consumption of organic devices. Third, the research activities of developing OFET biochemical sensors will be addressed. This review will provide guidelines for material design and fabrication processes of OFETs with high performance and advanced applications.

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Acknowledgements

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1. Introduction

Organic field-effect transistors (OFETs), utilizing organic semiconductor and dielectric layers, show several competitive advantages over their inorganic counterparts, such as low temperature and low cost processing, excellent mechanical flexibility, and great potential for performance improvement and functionalization via molecule structure tailoring.¹ Therefore, OFETs have attracted wide research attention and commercial interests to develop various flexible or conformal electronics on non-flat surfaces, or low cost item-level electronic devices for internet of things.²⁻⁴

In the last decades, achieving high mobility organic semiconductor channel layer has been continuously pursued for OFETs.⁵ There have been several review papers on material design and processing methods for this purpose.^{6, 7} Mobility values higher than 20 cm²/V·s were reported with several p-type organic small molecule and polymer semiconductors,^{8, 9} and for n-type organic semiconductors, the highest reported mobility also exceeds 10 cm²/V·s.¹⁰

However, these reported high mobility materials or OFETs were not converted to practical circuits and systems of equivalent performance. Recent studies showed that mobility overestimation could happen to many reported high-mobility OFETs mainly due to non-ideal field effect transistor electrical behaviors.^{11, 12} More importantly, it is rather difficult to integrate high-mobility organic semiconductors into a manufactural device stack that could meet the circuit and system design requirements, especially for many envisioned low voltage applications.

The most desirable manufacturing approach for OFETs is full additive printing for low cost, ease of customization, and large differentiation from the current mature technologies.^{13, 14} However, due to material and process limitations, it is challenging to realize all printing fabrication of the backplanes for high resolution displays or sensor arrays, which have strict requirements on refresh rate, integration density, and reliability.^{15, 16} On the other hand, for these applications, it is important to develop OFET processes compatible with existing manufacturing processes to minimize barriers for mass production.¹⁷ Meanwhile, lots of research has been carried out on improving printing based processes for finer resolution OFETs.¹⁸ Thanks to their inherent amplification, biocompatibility, and ease of miniaturization/integration, such "manufacturing-on-demanded" OFETs would be promising to construct transducers and simple signal processing circuitry for various bio-chemical sensing applications, such as pH, enzyme, DNA, cells, neuron, and protein sensors.¹⁹⁻²⁴ For these sensors, low-voltage operated OFETs with steep subthreshold swing is required to meet the system power constraints and avoid the generation of interference signals at large voltage bias.²⁵ Steeper subthreshold swing can also help to achieve larger transconductance efficiency for higher sensitivity.²⁶

With motivation of developing full printed low-voltage OFET and their applications for biochemical sensors and circuits, this paper will provide a review of research progress in three aspects, including printing processes for fine resolution OFETs, approaches for realizing low voltage OFETs, and device design for various bio-chemical sensors. Improving the printing process resolution to reduce both the channel length and gate to source/drain electrode overlap as well as the challenges of using printing processes to fabricate low voltage OFET transducers with efficient interactions to biological analytes will be discussed.

2. Printing fine resolution OFETs

2.1 Requirements for fine resolution



Figure 1. Schematic cross section illustrating (a) the bottom-gate, bottom-contact organic fieldeffect transistor structure and indicating the extent of the channel length (L_{ch}) and of the contact length ($L_{overlap}$), and (b) the self-aligned structure.

For most of transistor applications, improving the device operation speed is pursued. In biochemical sensor applications, high speed OFETs can help to achieve transducer with fast response to sensed signal. To fabricate a fully integrated sensor system with OFETs, integration of subsequent signal processing and antenna driving functions requires even higher operation speed.^{27, 28} The maximum operation speed of a field effect transistor is characterized by the cut-off frequency (f_T) as expressed by the following equation:²⁹

$$f_{\rm T} \approx \frac{\mu_{\rm eff}(V_{\rm GS} - V_{\rm th})}{2\pi L_{\rm ch}(L_{\rm ch} + 2L_{\rm overlap})} \tag{1}$$

where μ_{eff} is the effective charge-carrier mobility, V_{GS} is the gate–source voltage, V_{th} is the threshold voltage, L_{ch} and L_{overlap} are the channel length and gate to source/drain overlap length, respectively (Figure 1(a)).

Therefore, for developing high speed OFETs, in addition to the channel mobility, the process resolutions need to be improved for shorter channel length and smaller gate to source/drain overlap. As shown in Figure 1(a), the self-aligned structure has a most minimized parasitic capacitance by eliminating the overlap between gate and source/drain (S/D) electrodes. Reduction of L_{ch} and $L_{overlap}$ also helps to decrease possible gate leakage current, which is important to reduce the detection limit for weak signal sensing, and also brings benefits for general digital and analog circuit design. Meanwhile, OFETs of finer feature sizes will enable to make sensor arrays with smaller area for high throughput multi-parametric sensing with less required test solution.³⁰

Device performance and feature sizes of the reported fully printed or solution-processed OFETs are summarized in Table 1, with the electrodes being formed by different printing approaches, such as gravure, flexography, reverse-offset, screen, and inkjet printing. It can be found that the L_{ch} of most devices are larger than 20 µm, due to limited line resolution and registration accuracy achieved with the printing processes. Meanwhile the full overlapping of the gates to source/drain electrodes, which is mostly adopted for facile and reliable processing, will result in relatively large $L_{overlap}$ since it depends on the line width of the latter. Many research efforts have thus been devoted to either re-design the printing equipment for improved process accuracy, or developing new process techniques based on existing printing equipment.^{31, 32} For example, short channel length less than 1 µm can be achieved with subfemtoliter inkjet system and applied for partially solution-processed OFETs.³¹ However, few self-aligned gate structures with near-zero $L_{overlap}$ were achieved.³³ In addition to process issues, when the channel becomes short, the contact resistance becomes

dominating the device performance, and counteract the benefits brought be scaling of the channel length.³⁴ Thus, it will be important to consider how to reduce the contact resistance when developing fine resolution OFET processes. For complex circuit and array integration of OFETs, fine patterning of the organic semiconductor layer with simple printing or solution based approaches is also key to eliminating possible leakage current paths out of the gate control, and suppressing crosstalk among different OFETs. Based on these requirements, the work in the literature on processes to achieve short channel, fine line width, self-aligned gate structure and organic semiconductor patterning will be reviewed.

f							
Year	Process and materials for Semiconductor/Dielectric/Electrodes	Patt.	$L_{\rm ch}$	Overl.	μ (cm	ON/	$V_{\rm GS}$
S			(² /Vs)	OFF	(V)
emioon	ductor;	ofNgate	to180	urcø/dra	ain <u>,</u> 00N	/QFF,	onstof
c	(S/D: Ag)						
u2011 ³⁶	Inkjet (TIPS-pentacene)/Inkjet (c-PVP)/Inkjet (Ag)	Inkjet	47	Full	0.02	10^{4}	60
r 2011 ³⁷	Inkjet (NDI2OD-DTYM2)/Spin-coat (PAN)/Inkjet (Ag)	N/A	N/A	N/A	0.45	10^{6}	60
r 2012 ³⁸	Drop-cast (PBTTT)/Spin-coat (Teflon)/Spin-coat (G: Ag); Inkjet	N/A	40	Full	0.043	105	40
e	(S/D: Ag)						
n _{2013³⁹}	Drop-cast (PBTTT)/Spin-coat (c-PVP)/Inkjet (Ag)	By bank	20	Full	0.03	10^{4}	20
$t \ _{2014^{40}}$	Drop-cast (TIPS-pentacene/PS)/Spin-coat (c-PVA)/Inkjet (Ag)	N/A	35	Full	0.8	104	3
201441	Dispense (S1200)/Spin-coat (D207)/Inkjet (Ag)	By bank	22	Full	0.80	10^{6}	20
r 2014 ⁴²	Spin-coat (PBTTT)/Gravure (c-PVP)/Inkjet (Ag)	N/A	25	Full	0.1	10^{4}	40
a2014 ⁴³	Blade-coat (diF-TES-ADT/PTAA)/Blade-coat (Fluoro-	N/A	43	Full	0.31	105	20
t	polymer)/Inkjet (G: Ag);Blade-coat (S/D: PEDOT:PSS)						
i 201544	Inkjet (DPPT-TT)/Bar-coat (PMMA)/Inkjet (PEDOT:PSS)	Inkjet	40	N/A	0.19	10 ³	60
O 2016 ⁴⁵	Gravure (SP400)/Gravure (D320)/Gravure (Ag)	Gravure	10	Full	0.1	105	5
; 2016 ⁴⁶	Inkjet (TIPS-pentacene/PS)/Inkjet (c-PVP)/Inkjet (Ag)	Inkjet	40	Full	0.26	105	3
, modili	ty)nkjet (TIPS-pentacene)/Inkjet (c-PVP)/Inkjet (Ag)	Inkjet	9	Full	0.065	103	60
201648	Inkjet (FS0096)/Inkjet (c-PVP)/Inkjet (Ag)	Inkjet	100	Full	0.02	10 ²	30
201649	Blade-coat (TIPS-pentacene/PS)/Screen (5018)/Screen (Ag)	N/A	N/A	Full	0.308	105	60
201650	Drop-cast (TIPS-pentacene/PS)/Spin-coat (SU8)/Inkjet (Ag)	N/A	75	Full	0.4	105	5
201651	Drop-cast (TIPS-pentacene/PS)/Spin-coat (PVCN)/Inkjet (Ag)	N/A	40	Full	0.6	10^{6}	3
2017 ⁵²	Blade-coat (TIPS-pentacene/PS)/Spin-coat (PVCN)/Inkjet (Ag)	N/A	50	Full	0.37	105	5
201753	Drop-cast (TIPS-pentacene/PS)/Spin-coat (PVCN/P(VDF-TrFE-	N/A	N/A	Full	0.2	10^{6}	5
	CFE))/Inkjet (Ag)						
201754	Drop-cast (TIPS-pentacene)/Inkjet (PVP)/Inkjet (PEDOT:PSS)	N/A	114	N/A	0.95	103	0.8
201755	Inkjet (TIPS-pentacene/PS)/Inkjet (PVCN)/Inkjet (Ag)	Inkjet	20	Full	0.1	10^{6}	3
201756	Inkjet (DPP-TT)/Inkjet (c-PVP)/Inkjet (Ag)	Inkjet	0.8	Full	0.27	105	12
201757	Gravure (SP series)/Gravure (D series)/Inkjet (G: Ag);Gravure	Gravure	42.5	N/A	0.208	106	80
	(S/D: Ag)						

Table 1. Summary of OFETs fabricated by all solution-processed process/printing (Pa	tt., p	patterning
0		

2.2 Short channels

To fabricate short channels and fine line widths, several approaches based on gravure, flexography, reverse-offset were developed by pre-patterning micro-structures onto the roller or the imprinting plate.⁵⁸⁻⁶⁰ For low cost digital manufacturing, drop-on-demand inkjet printing is a preferred choice with great material saving and short design-to-product time. However, the complicated dynamics during ink droplet generation from the print head, and jetted droplets impacting the substrate surface make the normal printers difficult to achieve fine resolution patterns with narrow line width and short channels.⁶¹ With a widely used 10 picoliter (pL) print head, the achievable line width and gap distance of electrodes is normally larger than 50 μ m.⁶² Recently, by optimizing printing conditions such as the surface energy of substrates, platen temperature, and voltage wave-form for the conventional printer, direct printing of short channel lengths less than 10 um have been reported for incorporating in low-cost printable OFETs, where the details were not fully revealed.²⁶⁻²⁸ Super inkjet printing using a femtoliter (fL) printer head with high registration accuracy is developed to form narrow line width and short channel down to 1 µm for OFET fabrication.³¹ However, continuous generation and accurate control of such tiny ink droplets in high throughput manufacturing is very challenging. Therefore, several techniques on improving the printing resolution using the common inkjet printers have been developed.

Wetting-constrained printing: Based on the understanding that shorting might occur as straight rows of drops were printed in close proximity due to the presence of bugling, Tseng and co-workers proposed a unique printing process to control the ink wetting behaviour and allow the source/drain electrodes to be inkjet printed close enough to each other without shorting.³⁵ In their studies, two guiding drops were firstly placed at the beginning of the source and drain lines, off-axis and away from the channel. The contact of the early formed bulge would guide the successively printed drops away from the channel, where small spacing of 12 μ m was achieved without shorting. Fully printable scaled PBTTT OFETs were thus implemented and showed high speed operating frequencies of 18 kHz. In the work of Tang et al., by modulating the surface energy of PVA with fluoroalkylsilanes (FOTS), the wetting of Ag inks during merging process was much reduced due to the un-favorable wettability, resulting in formations of narrower electrodes with shorted channels.⁶³ It was found that the width of the narrowest uniform electrodes printed on FOTS-PVA was approximately $(35 \,\mu\text{m})$, which was two-times smaller than that on PVA, while the controllable channels of sub-20 μ m were demonstrated (Figure 2(a)). Moreover, the surface energy modulation was also exploited to facilitate the patterning of organic semiconductors through self-assembling. Thus they successfully realized fully printable 2 V-operation OFETs with 15 µm short channels based on TIPS-pentacene/PS blend channel, achieving an estimated mobility of 0.2 cm²V⁻¹s⁻¹ and high on/off ratio of 10⁴. Instead of additionally modifying the wetting properties of inks on substrate, Chu et al. reported on a direct-writing fabrication process of OFETs with short channels less than 1 µm by using the dissolving effect between ink solvents and interlayer material.⁵⁶ The key to defining an ultra-narrow channel was attributed by the ridge formed along the printed Ag line edges caused by redistribution of the uncross-linked SU8 surface during the drying process, which limited the ink spread and separated neighbouring printed lines with a minimum gap of 0.8 µm by carefully adjusting the printing parameters.

Self-aligned printing: To yield small spacing yet avoid the shorting, a self-aligned printing approach was developed by Doggart *et al.* based on the self-repelling effect against the overlapped electrodes.⁶⁴ The mechanism relied on the engineering of ink formulate with organoamine as a stabilizer for silver nanoparticles, which allowed the formation of a hydrophobic boundary around

the first printed Ag electrodes, followed by repelling and self-aligning of the ink subsequently printed in the vicinity of the original electrode s. This facile method enabled printing of very reproducible channels as short as $10 \,\mu\text{m}$ with a very narrow distribution of channel length.

In the pioneering work of Sirringhaus et al., an alternative self-aligning printing technique was developed to aggressively scale the channels and create sub-micrometer channels. It consisted of two steps, i.e., printing/evaporating a first electrode which was further treated more hydrophobic by plasma treatment and repulsive to the successively deposited inks, followed by another printing of a second electrode along the edge of the first electrode by certain overlapping, which was selfaligned off the first conductive electrode to attain sub-micrometer channels (Figure 2(b)).^{65, 66} In their subsequent work, they used PFDT self-assembled monolayers for modulating the firstly printed gold electrodes more repulsive, instead of CF₄ plasma for PEDOT:PSS, and were capable achievement of channel lengths of 100 nm scale with a surprisingly high device yield.⁶⁶ The resulting top-gate p-type F8T2 OFETs with 0.2 µm channel length exhibited field-effect mobility up to $0.005 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and high on/off ratios of 10^3 - 10^4 . This approach was also applicable to fabricate high performance n-type short channel (0.2 µm) N1400 OFETs by using low work function Ag as source electrode to enhance the charge injection at the contact.⁶⁷ Thanks to the utilization of ultra-thin cross-linked Cytop dielectric, short channel effects were nearly observed in the scaled down device with crisp current saturation for operating voltages lower than 5 V. Furthermore, lowpower organic complementary inverter was demonstrated based on high performance printed topgate TIPS-pentacene (p-type) and P(NDI2OD-T2) (n-type) OFETs sharing the same substrate, achieving noise margin values of 56% and a gain higher than 10.68

Hybrid printing: To obtain channels with higher resolution (< 10 µm) for common inks, a print-and-drag hybrid printing technique was proposed by Tseng *et al.* using micron-scale mechanically controlled tungsten probe, which acted as a pen to drag through the pad, to create a highly scaled feature (< 5 µm).⁶⁹ Combined with the early developed approach for printing source/drains to align the gate, fully-printed short channel OFET inverters were demonstrated, attaining propagation delays as low as 15 µs. Interestingly, another hybrid printing technique towards higher resolution was adopted with the help of laser ablation in a direct-written way, as reported by Bucella and coworkers.⁷⁰ The sub-micrometer channels were produced by femtosecond laser ablation of inkjet printed Ag electrodes into a pair of source/drain electrodes with high resolution (Figure 1(d)). These electrodes were successfully demonstrated in the fabrication of both p- and n-type, top-gate OFETs with sub-micron channels, showing mobilities higher than 0.1 cm²V⁻¹s⁻¹.



Figure 2. Printing of short channels. (a) Illustration of the realization of the relatively short channel length by constraining the wetting of ink on the FOTS–PVA. Reprinted with permission.⁶³ Copyright 2014, Royal Society of Chemistry. (b) Schematic of the self-aligned inkjet printing (SAP)

process. The dashed line indicates the initial position of the printed gold nanoparticle ink before dewetting from the hydrophobic surface layer on the electrode. Reprinted with permission.⁶⁵ Copyright 2007, Nature Publishing Group. (c) Schematic of the hybrid printing which consists of inkjet printing the silver ink line and then ablating the sintered silver line to form high resolution channels with femtosecond laser ablation (FLA). Reprinted with permission.⁷⁰ Copyright 2013, Elsevier.

2.3 Self-aligned structure

It is noteworthy that decrease of the contact length also contributes to the operation speed because $f_{\rm T}$ increases in proportion to the inverse sum of $L_{\rm ch}$ and $L_{\rm overlap}$. As OFETs aggressively scale down, the contact length gradually becomes comparable to the channel length, where the parasitic capacitance begins to play an important role in determining the circuit performance. Although this leads to the requirement for self-alignment of gate electrode with respect to the source/drain electrodes for printable OFETs, it still remains challenging due to the limited registration accuracy and dynamics with state-of-the-art volume printing.

To minimize the parasitic overlap capacitances, Noh *et al.* proposed a novel fabrication process for printable tog-gate OFETs with self-aligned gate architecture, which comprised four-steps, e.g., depositing a thick (1 mm) photoresist on top of the ultra-thin (30–50 nm) cross-lined PMMA gate dielectric layer; selectively irradiating the exposed channel region by UV through the back of the substrate; forming a trench structure self-aligned with respect to the edges of the source and drain electrodes by developing of the photoresist; and finally inkjet printing a wide gate electrode.⁶⁵ As a result, the developed structure consisted of a required ultra-thin gate dielectric of large capacitance right over the channel and a very thick bilayer dielectric with a minimized capacitance (Figure 3(a)). Short channel (100 ~ 400 nm) OFETs with the developed self-aligned gate configuration yielded a low parasitic overlap capacitance to values as low as 0.2–0.6 pF/mm, showing a high transition frequencies of 1.6 MHz.

The aforementioned approach depended on the UV irradiation through shadow mask, i.e., preprinted source/drain electrodes, and was thus only applicable to top-gate OFETs. With the help of patterned surface wettability-assisted alignment technique, Arai *et al.* demonstrated aligned bottomgate OFETs (Figure 3(b)).⁷¹ In their work, a photosensitive SAM was firstly applied to the gate dielectric to produce a hydrophobic surface, and then was decomposed by exposure to UV light through the back substrate. The exposed surfaces, responding to the source/drain regions, became hydrophilic with TMAH rinsing, and enabled the self-alignment of PEDOT:PSS source/drain electrodes with respect to the bottom-gate electrode. Similarly, Bonfiglio group performed the UV radiation to expose and pattern the deposited photoresist film through the back side of ultra-thin transparent parylene-C dielectric using the bottom-gate as mask, where the photoresist covering only the gate electrode enabled the successive self-aligned source/drain electrodes by the lift-off.⁷² Thanks to self-aligning, very small parasitic capacitances were evaluated of of 8 ± 2 pF and a cutoff frequency of 100 kHz was obtained, which was 3 orders of magnitude improved compared to that of non-self-aligned device.

However, these techniques used time consuming UV irradiation and development to facilitate the implement of alignment, increasing the process complexity. Subramanian group used a novel inkjet printed wetting-based roll-off process for self-aligning transistor source/drain electrodes to gates and demonstrated a self-aligned transistor by all inkjet printing exclusively.³³ It was achieved

by facilitating the roll-off of subsequent printed S/D electrodes from the previously formed mesa composed of a bottom gate and a PVP insulator, resulting in an improved overlap capacitance as small as 0.14–0.23 pF/mm (Figure 3(c)). They for the first time fabricated fully self-aligned inverters with a propagation delay as low as 0.488 ms at a fan-out of 1.



Figure 3. Realizing self-aligned structures. (a) Schematic of the process to form a self-aligned gate structure, comprising deposition of a photosensitive dielectric, UV irradiation through the back of substrate and development, and inkjet printing of gate electrode. Reprinted with permission.⁶⁵ Copyright 2007, Nature Publishing Group. (b) Main steps in the realization of the self-aligned OFETs by UV irradiation through the back of substrate using bottom-gate as mask. Reprinted with permission.⁷² Copyright 2007, Elsevier. (c) Wetting-based roll-off process with self-aligned source/drain electrodes consisting of four layers of printing.³³ Copyright 2010, Elsevier.

It should be noted that the influence of contact resistance (R_c) on f_T is implicit in equation (1) because μ_{eff} is in theory impacted by R_c :

$$\mu_{\rm eff} \approx \mu_0 \left(1 - \left(\frac{\mu_0 C_i W R_c (V_{\rm GS} - V_{\rm th})}{L + \mu_0 C_i W R_c (V_{\rm GS} - V_{\rm th})} \right)^2 \right)$$
(2)

Due to the presence of relatively large R_c , arising from the presence of injection barrier at the source/organic semiconductor, μ_{eff} will drop significantly as the channel length of the devices scales down. This means that the contact resistance should also be taken into account when the channel is printed shorter in high-resolution OFETs. Note that most printed OFETs are based on staggered-type structure (i.e., top-gate bottom-contact or bottom-gate top-contact structure) and their contact resistance is strongly dependent on the contact length.^{72, 73} Thus, there is a trade-off between the self-alignment and reasonable overlapping for aggressively downscaled high performance OFETs since the contact resistance issue cannot be well addressed at present.²⁹ For the state-of-art inkjet printed OFETs with coarse resolution on micrometer scale and relatively large contact resistance, full overlapping of gate to source/drain has thus been widely used in order to promise a high injection effectivity with reasonable convenience of manufacturing. Nevertheless, efforts have to be devoted to contact engineering in order to fabricate high performance self-aligned OFETs of high resolution.³⁴

2.4 Fine patterning

Patterning of OFETs is not only a routine to fabricate active-matrix display and integrated circuits, but also an effective means to promote device performance such as elimination of cross-talk, improvement of ON/OFF, and reduction of static power consumption. There have been a variety of subtractive and additive techniques developed to pattern the organic semiconductors (Figure 4).

2.4.1 Subtractive patterning

Dry-etching: Conventional photolithography is the most mature one to provide microscale or higher resolution patterning, benefiting from the well-established manufacturing facilities in the industry. However, such a task is extremely challenging for printable OFETs because of the chemical incompatibility of the commonly used solvents needed to process photoresist and development with the organic soluble semiconductor and the potential degradation of performance induced by UV irradiation and etching process.

To circumvent the chemical or physical damage of the underlying organic semiconductor layer, Chang *et al.* employed a perfluorinated Cytop polymer as the protective layer throughout the conventional lithographic development and plasma dry-etching processes, realizing photolithographically patterned semiconducting islands with feature size down to a micrometer (Figure 4(a)).⁷⁴ The developed patterning approach was demonstrated applicable to versatile soluble polymer semiconductors (e.g. PBTTT, P3HT, PQT, and F8T2) and compatible with all common transistor architectures with either top gate or bottom gate. The on/off ratios of patterned PBTTT and P3HT top-gate transistors were expected to considerably enhance by 2–3 orders of magnitude compared to the unpatterned devices, where the off-currents of the patterned devices was reduced to the gate leakage level on the pA scale.

Later, Tang and co-workers found that the patterned top-gate OFETs based on the state-of-art IDT-BT semiconductor, enabled by the similar dry-etching process, had enhanced on/off ratio as well but also showed deteriorated performance with poorer subthreshold behaviour and decreased mobility.⁷⁵ This was ascribed to increased interface trap density at the semiconductor/dielectric interface caused by removing the protective Cytop layer and exposing of the critical conductive channel, while using the polymer protective layer as a part of gate dielectric instead of removing it resulted in high performance. These studies indicate that the protective interlayer not only enables the patterning process for high-resolution OFET devices, but also allows the achievement of high performance.

UV irradiation: Inspired by the deleterious influence of UV irradiation during conventional photolithography, Kim *et al.* proposed a facile and general route to achieve high-resolution (subµm-scale) scalable patterning of OFETs by using highly energetic photons to directly trigger the photo-conversion of organic materials (Figure 4(b)).⁷⁶ When deep-ultraviolet (DUV) irradiation was performed with chrome-patterned quartz masks to the soft matters, they transformed from conducting/semiconducting to insulating state due to the dissociation of specific chemical bonds within molecules as well as the loss of inter-molecular ordering. It was demonstrated that the resulting patterned small molecule (C8-BTBT) and polymer (P3HT and P-29-DPPDTSE) OFETs showed no noticeable mobility degradation but an improvement of ON/OFF due to the excluding of fringing current. Thanks to the patterning, the supply current in the patterned inverter deceased by an approximately 3 orders of magnitude while gain almost maintained identical, suggesting lower power consumption. Unlike the photolithographic patterning in industries, the developed method is free of using chemical solvents related to development and cleaning, which is of great interest.

Removement and isolation: Recently, a laser ablation assisted patterning approach was for the first time used to fabricate solution-processed PDVT-8 OFET arrays without utilization of undesirable chemical solvents as well.⁷⁷ The patterning approach relied on removement of undesired materials and isolation of channels by high energy laser ablation, which significantly simplified the fabrication process (Figure 4(c)). Noteworthy, it needed careful selection of laser processing parameters and materials to produce of OFET arrays with high quality and high yield. Alternatively, Nguyen *et al.* adopted a simple transferring method to pattern TES-ADT crystals by adversely removing the undesirable parts using a PDMS mold containing 1,2 e dichloroethane (DCE) solvent and obtain high feature resolution below 1 μ m (Figure 4(d)).⁷⁸ This method simultaneously facilitated the growth of TES-ADT thin films into crystal patterns and enabled high performance OFETs with a field-effect mobility of 0.3 cm²V⁻¹s⁻¹.

2.4.2 Additive patterning

Although the aforementioned approaches provide various advantages such as high resolution, high quality semiconductor/dielectric interface, and flexibility for patterning versatile semiconductors, they rely on expensive sophisticated equipment and are time consuming. Additive processes like transfer printing and inkjet printing are more attractive to pattern printable OFETs with high yield and low cost.

Transferring from module: In the work of Ikawa *et al.*, transfer printing of polymer semiconductors (PH3T, PBTTT and PQT) was demonstrated by controlling of the PDMS stamp's sorptive nature against the organic solvent via temperature modulation. It was realized by firstly transferring organic films from one substrate, where high quality films were pre-deposited through dedicated push coating, to a pattern-moulded glass plate with a higher surface energy and then transferring the desirable patterned pattern to the device substrate (Figure 4(e)).⁷⁹ Other mass-printing technologies, such as conventional gravure, offset, flexographic, screen printing etc., have also been applied to manufacturing flexible and printed electronics, enabling roll-to-roll printed OFETs by incorporating with each other and solution coating.¹⁴ The benefits of these printing approaches for patterning printable OFETs may be high resolution and compatibility with large-area printing, however, the requirement for specific mould sacrifices the low cost and convenience provided by maskless printing.

Selective wetting: To date, inkjet printing has been extensively used to develop high performance OFETs in a drop-on-demand manufacturing way in spite of having a coarse resolution (Figure 4(f)).^{46, 55, 80} Although the channel is directly formed by inkjet printing droplets into the required regions, non-controllable edges tend to emerge in printed channels, causing serve non-uniformity issue. With the aim of obtaining uniform channel width with high accuracy, contrasting the surface wettability by modulating its surface energy has been extremely studied to confine the semiconducting film into a regular dimension.

For instance, Li *et al.* demonstrated that the selective treatment of the surfaces of the hydrophobic Cytop dielectric by O₂ plasma through a shadow mask made such surfaces hydrophilic, followed by the application of soluble ink, resulting in the patterned C8-BTBT films.⁸¹ However, for intrinsic hydrophilic polymers, wettability contrast would be very limited by using this approach, leading to the requirement for pre-modulating the surface more hydrophobic. In the work of Tang *et al.*, to achieve the patterned wettability, self-assembled monolayers (FOTS) were used to modify the hydroxyl-rich PVA more hydrophobic, followed by selectively removing those in the channel

region via ultraviolet ozone.⁶³ The solvent for TIPS-pentacene/PS blend (chlorobenzene) showed asymmetric wetting in and outside the channel regions, evident from lower contact angle of 10° in the channel region compared to 71° outside the channels (Figure 4(g)). As a result, printable low-voltage OFETs were produced on the PVA dielectric with patterned wettability.

Patterning by bank: Note that shadow masks were used to determine the selective patterning of wettability, sacrificing disadvantage of maskless manufacturing. As an alternative, using a bank to act as container for semiconductor inks is a practical means to facilitate the patterning of printable OFETs. This is because bank can be manufactured-on-demand where required by well-established process and is capable of matching with other subsequent effective printings or solution coating (Table 1). The lyophobic fluoropolymer Teflon was extremely used for constructing the bank structure (Figure 4(h)).^{82, 83} Fukuda et al. reported on the use of 200-nm-thick dispensed fluoropolymer (Teflon) bank to pattern printed OFETs, where the semiconductor inks were printed with a dispenser with an optimum concentration is 0.05 wt.%, and demonstrated high speed printed organic inverter circuits.⁸⁴ On the other hand, exceptional uniformity was obtained by bank patterning in the demonstrated short channel (< 20 µm) OFET arrays comprising 100 devices, as expected, whose mobilities were estimated up to be 0.80 6 0.23 μ m.⁴¹ In the work of Mizukami *et* al., high-resolution Teflon bank was formed by photolithographic wet-etching or dry-etching and enabled patterning of OFET pixels for flexible organic light-emitting diode displays.^{85, 86} Interestingly, higher mobilities were also achieved by either using solution-shearing instead of coarse dispensing or inkjet printing of high performance semiconductor/polymer blends. Another widely used fluoropolymer was Cytop, which facilitated the homogeneous dewetting of high performance C8-BTBT and resulted in fully-printed patterned OFETs with a high mobility and on/off ratio of the OFETs exceeded 13 cm²V⁻¹s⁻¹ and 10⁸, respectively.⁸⁷



Figure 4. Fine patterning of printable OFETs. (a) Schematic of photolithographic patterning of semiconducting polymers using Cytop layer as a protective layer. Reprinted with permission.⁷⁴ Copyright 2010, Wiley-VCH. (b) Schematic diagram of patterning of organic thin films through the deep-ultraviolet (DUV) irradiation and cross-polarized optical microscopy (CPOM) images of the resulting patterned semiconductors. Reprinted with permission.⁷⁶ Copyright 2015, Nature Publishing Group. (c) Microscopy images of patterned OFET arrays after laser ablation. Reprinted with permission.⁷⁷ Copyright 2017, American Chemical Society. (d) Schematic of semiconductor

patterning by transfer the un-desirable patterns. Reprinted with permission.⁷⁸ Copyright 2017, Elsevier. (e) Schematic of semiconductor patterning by transfer the desirable patterns. Reprinted with permission.⁷⁹ Copyright 2012, Nature Publishing Group. (f) Polarized optical micrograph of an inkjet printed OFET. Reprinted with permission.⁵⁵ Copyright 2017, Wiley-VCH. (g) The measured contact angles on wettable and unwettable surfaces using chlorobenzene as the test liquid and microscopy images of the patterned TIPS-pentacene/PS islands in channel regions. Reprinted with permission.⁶³ Copyright 2014, Royal Society of Chemistry. (h) Optical microscope image of the OFET layout and magnified image of the patterned channel with a bank. Reprinted with permission.⁸² Copyright 2017, Wiley-VCH.

3. Approaches for low voltage operation

3.1 Basic device physics

The required operation voltage for a field-effect transistor is mainly determined by the subthreshold swing (SS), a measure of how easily a transistor can be switched from the off-state to the on-state. In theory, a field-effect transistor's SS can be expressed in a simplified model as⁸⁸

$$SS = \frac{dV_{\rm GS}}{d\log I_{\rm D}} = \ln 10 \cdot \frac{k_{\rm B}T}{q} \cdot \left[1 + \frac{q}{C_{\rm diel}} \cdot \left(\sqrt{\epsilon_{\rm s} N_{\rm bulk}} + q N_{\rm int} \right) \right]$$
(3)

where both the density of deep bulk traps N_{bulk} and the density of deep interface traps N_{int} as a function of energy is constant, k_{B} is the Boltzman's constant, T the absolute temperature, q the absolute value of the electron charge, ε_{S} semiconductor dielectric constant, and C_{diel} the gate dielectric capacitance.

The equation may be simplified as

$$SS = \ln 10 \cdot \frac{k_{\rm B}T}{q} \cdot \left[1 + \frac{q^2 N_{\rm sub}}{C_{\rm diel}} \right]$$
⁽⁴⁾

where N_{sub} (per unit area and unit energy) is the subgap density of states (DOS) contributed by both the deep bulk traps and the interface traps.

Device engineering by either enlarging C_{diel} or reducing N_{sub} enables the realization of steep subthreshold swing for OFETs. The former approach, which has been extensively adopted to normally form large capacitance hundreds of nF/cm², is feasible for common organic semiconductors. A large gate capacitance is also desired to enhance the current driving capability and facilitate the scaling of OFET circuitry. The latter strategy is more dependent on the formation of high quality channel instead of the choice of dielectric materials, providing a greater degree of freedom in dielectric materials. The utilization of small gate capacitance is extremely beneficial for low power operation, given the presence of significant contact resistance and parasitic capacitance.⁵⁰ In addition to subthreshold swing, other device electrical characteristics (e.g., mobility, hysteresis, leakage) are also prone to affect by the choice of dielectric and semiconductor materials and their processing. In this regard, there is a tradeoff between performance requirements (e.g., low-voltage, high mobility, high reliability) and processability requirements (e.g., large-area printing/solution coating, high uniformity, reproducibility).¹⁷

3.2 Enlarging the gate capacitance

The idea of using ultra-thin and high-k dielectrics for enlarging the capacitance of conventional gate dielectric is straightforward according to the fundamental equation describing the capacitance. Since Dimitrakopoulos *et al.* firstly adopted sputtered high-k oxides (BZT, BST, and Si₃N₄) as gate

dielectrics to fabricate low-voltage pentacene OFETs, high-k inorganic insulators have been introduced for developing low-voltage OFETs. To this end, the metal oxides (AlOx, ZrOx, HfOx, TiO_x, TaO_x, YO_x, etc.) been extensively used due to their ready availability from inorganic fieldeffect transistor technology.⁸⁹ For examples, high-k AlO_x is one of the most reported insulators for conventional low-voltage OFETs in the previously studies, which is available from the ready vacuum deposition/oxidation, e.g., atomic layer deposition (ALD), pulsed lased deposition (PLD), e-beam evaporation, O₂ plasma oxidation, and UV-O₃ oxidation. Note that to circumvent the leakage issue and improve the semiconductor/dielectric interface, self-assembled monolayers (SAMs) such as ODPA are also mandatory to incorporate into the metal oxide (MO_x) dielectrics to form a classical hybrid structure (SAM/MO_x).^{3, 90, 91} More recently, interests in solution-processable high-k metal oxide dielectrics have arisen primarily from the requirements for inexpensive large-area fabrication processes. Low-voltage OFETs with steep subthreshold swing have been demonstrated using solution-processable MOx manufactured by sol-gel method, LbL deposition, UV-curing, anodic oxidation.⁹²⁻⁹⁷ Whereas the remaining challenges is that the resulting oxides often involve hightemperature annealing and tend to form very thin films, which is not desired to solution-coating or printing.⁸⁹ Therefore, polymer dielectrics have been widely utilized to fabricate printable OFETs (as shown in Table 2) due to high solubility in organic solvents and compatibility with solution coating/printing, which will be discussed in the following sections.

- Т
- а
- b
- 1

OSC^{a)} e Type^{b)} Dielectric^{a)} k ON/OFF SSt (nm) C_{diel} μ (cm² Year (nF/cm²) V⁻¹s⁻¹) (mV/dec) Ultra-thin polymeric dielectrics 50-70 45 N1400 TGBC 0.06 105 250 201098 c-Cytop 201399 PVP-4T PTDPPTFT4 10^{6} 3.1 50 58 BGTC 0.129 110 S c-PMMA TIPS-TPDO-BGTC 105 2016100 3.9 100 0.018 250 _ u tetraCN m **PVP:HDA** 4.2 ~22 140 TIPS-BGTC 4.2 10^{4} 380 2018101 m pentacene/PS ł High-k polymeric dielectrics r P(VDF-TrFE-CFE) 10^{6} 2012102 60 160 330 PBTTT-C16 TGBC 0.4 97 y P3HT TGBC 0.3 --P(NDI2OD-T2) TGBC 0.1 10^{4} 160 0 PVDF-HFP:PVP PSe-DPP 105 2017103 10 230 28.2 BGTC 0.191 _ f PII-2T BGTC 0.107 10^{3} _ c-PVP 7 400 15 TIPS-pentacene BGBC 0.95 10^{3} 300 201754 Low-k/high-k bilayer dielectrics e 2013104 ZrO₂-16.5 258 60 P3HT BGTC 0.08 $\sim 10^{3}$ _ V CYELP/ODPA i PVA/P(VDF-7.9/60 20/160 P(NDI2OD-T2) 10^{5} 200 2014105 TGBC 0.32 с TrFE-CFE) e

- С
- р
- e
- r

PVA/OTS	7.3	-/230	28	PVDT-10	BGTC	11	10^{4}	-	2014106
Cytop/P(VDF-	-	8/270	104	IDT-BT	TGBC	1.4	10^{6}	158	2015107
TrFE-CFE)									
BST-(P(VDF-	13.2	178/30	64.4	PDPPTT	BGBC	0.14	$\sim \! 10^3$	221	2015108
HFP)/PVP									
BST-CEC/PVP	19	378	44.5	DPPTTT	BGBC	0.6	$\sim \! 10^3$	238	2016109
			TIPS-pe	entacene/PaMS	BGBC	0.3	$\sim \! 10^3$	170	

^{a)} Deposited by solution process/printing; ^{b)} Types of OFET geometry are classified as bottom-gate and bottom-contact (BGBC), bottom-gate and top-contact (BGTC), top-gate and bottom-contact (TGBC), or top-gate and top-contact (TGTC).

3.2.1 Ultra-thin polymeric dielectrics

Because of the low dielectric permittivity for common polymeric materials, utilization of ultrathin gate dielectric is very straightforward to fabricate low-voltage printable OFETs. However, the insulating property of pristine polymeric dielectrics is also prone to sacrifice when its thickness decreases, resulting in poor electrical reliability. Therefore, cross-linking of dielectrics is desired to improve the insulating performance, which is also the requirement for orthogonal processing of other OFET functional layers on top. Examples of low-voltage OFETs using ultra-thin (< 100 nm) cross-linked dielectrics have been reported by many groups as shown in Table 2.

However, the non-conformal wet coating of dielectric films on the rough underlying surface inevitably results in poor uniformity and reproducibility at present. In addition, thinner solutioncoated or printed films always suffer a predictably higher risk of leakage through pinholes, thus resulting in low device yield.^{98, 110, 111} It is noteworthy that chemical vapor deposition (CVD) based insulating polymers such as poly(chloro-p-xylylene) (parylene-C) or poly(1,3,5-trimethyl-1,3,5trivinyl cyclotrisiloxane) (pV3D3) can be coated conformally and un-destructively onto various underlying materials (such as electrode, semiconductor, dielectric or substrate) at low process temperature, which enables to fabricate OFETs across various device configurations with remarkably high device yield and uniformity.^{112, 113} Although losing the cost and large area advantages conferred by printing, high quality dielectrics deposited by CVD deserve to be important material sets for printable OFETs and circuits with better reliability. The combination of the two techniques, namely printing and chemical vapor deposition, represents an important approach for a reliable fabrication of large area OFETs.¹¹⁴ Another advantage of using these kinds of vacuum processed insulators is that they are also very attractive to passivate the OFET devices, which not only substantially improves the reliability performance but also enables successive procedure for integration of electronic elements on top available.115

3.2.2 High-k polymeric dielectrics

It is thus mandatory to search for high-*k* polymeric dielectrics to address the contradictory selection of low-*k* ones between processing reliability (high thickness) and steep subthreshold swing (large gate capacitance). The utilization of high-*k* polymers is certainly a promising way to high capacitance gate dielectrics for steep subthreshold printable OFETs (Table 2), which remains advantages of both traditional inorganic materials (high-*k*) and polymer ones (low temperature solution processability and mechanical flexibility).

Compared to other conventional polymers, the most well-known high-k (> 20) polymeric dielectrics are ferroelectric fluoropolymer poly(vinylidene fluoride) (PVDF) based copolymer and

terpolymers.⁸⁹ However, the prominent ferroelectric behavior of P(VDF-TrFE) copolymers may cause serious current-voltage hysteresis in the fabricated OFETs, which are thus applied to memory applications. By introducing a small amount of the monomer chloro fluoroethylene (-CFE) into the backbone of P(VDF-TrFE) copolymer to disrupt ferroelectric domain formation, a terpolymer P(VDF-TrFE-CFE) relaxor is obtained with reduced ferroelectric behavior and hysteresis. Yan *et al.* firstly reported on the use of high-*k* (55 at 1 kHz) P(VDF-TrFE-CFE) with a molar ratio of 56:36.5:7.5 as gate dielectrics for solution-processed polymer OFETs (Figure 5(a)). They demonstrated low operation voltage (< 3 V) with very sharp subthreshold swing (< 100 mV/dec) and negligible hysteresis enabled even by thick dielectrics (~160 nm).¹⁰² Based on the high-*k* P(VDF-TrFE-CFE) terpolymer, low-voltage printable circuits were also realize.^{90, 116} However, the remaining challenge is that when the high-*k* gate dielectric layer is directly interfacing the channel of "face-on" molecule packing, the energetic disorder caused by the dipoles in high-*k* dielectric would tend to trap carriers from gate bias induced conduction channel. The resulted localization of charge carriers could cause not only mobility degradation, but also increased hysteresis and device instabilities.

3.2.3 Low-k/high-k polymeric dielectrics

To address the mobility degradation and instability issues of the OFETs with high-k gate dielectrics, the low-k/high-k bi-layer structure gate dielectric has been proposed with a thin low-kdielectric layer between the high-k one and the organic semiconductor channel to suppress the dipole field effect.¹¹⁷⁻¹¹⁹ Li et al. found that the electron mobilities of n-type P(NDI2OD-T2) observed in the P(VDF-TrFE-CFE) gated 3 V-operating OFET devices were only $0.11 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$, which were relatively lower than the value reported previously. By using a thin PVA (20 nm) as a buffer dielectric to form a PVA/P(VDF-TrFE-CFE) bilayer, the fabricated OFETs exhibited an improved mobility $(0.36 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1})$ with negligible hysteresis.¹⁰⁵ In a subsequent report on low-voltage stateof-the-art polymer (indacenodithiophene-benzothiadiazole, IDT-BT) OFETs, the P(VDF-TrFE-CFE) films were coated with a orthogonal low-k fluoropolymer (Cytop) to form a tuned organic semiconductor/dielectric interface, which finally enabled higher mobility with a small SS of 150 mV/dec.107 It is noteworthy that the stability under prolonged bias was extremely improved compared to single Cytop or P(VDF-TrFE-CFE) dielectric gated OFETs, where threshold voltage changed less than 0.08 V after 3600 s negative bias stressing (Figure 5(b)).¹²⁰ The performance enhancement could be explained by the neutralization of the charge trapping effect at the IDT-BT/Cytop interface and remnant polarization effect of relaxor P(VDF-TrFE-CFE) under gate bias. Based on the identical Cytop/P(VDF-TrFE-CFE) dielectric, Pecunia and coworkers demonstrated high performance low-voltage IDT-BT/F4-TCNQ blend OFETs with near-ideal behaviors, showing small contact resistance, overlapped linear and saturation mobilities, and poor independence of mobilities on gate-source voltage.¹²¹ Instead of Cytop, another fluoropolymer Teflon was used by Ng et al. for the thin low-k capping layer, the Teflon/P(VDF-TrFE-CFE) bilayers, which were coated to form thick gate dielectrics (800 ~ 900 nm), facilitated the fabrication of stable printed OFETs with high performance (Figure 5(c)).¹²² Furthermore, high performance printed circuits have also been demonstrated, pulsed voltage multiplier, NAND and NOR gates, ring oscillators, and single-OFET gain stage with latch.^{118, 122, 123}



Figure 5. Low-voltage OFETs with high-*k* polymeric P(VDF-TrFE-CFE). (a) Schematic diagram of the molecular structure of solution processable relaxor P(VDF-TrFE-CFE). Dielectric constant and loss of P(VDF-TrFE-CFE) 56/36.5/7.5 mol% terpolymer film as functions of measurement frequency at room temperature. Reprinted with permission.¹⁰² Copyright 2012, Wiley-VCH. (b) Transfer curves measured at different time under negative bias stress (NBS) for the IDT-BT OFET with a Cytop/P(VDF-TrFE-CFE) bilayer dielectric, showing high biasing stress stability. Reprinted with permission.¹²⁰ Copyright 2017, IEEE. (c) Transfer characteristics of a typical printed OFET using Teflon/P(VDF-TrFE-CFE) bilayer as gate dielectric before and after 5-min bias stress. Reprinted with permission.¹²² Copyright 2016, IEEE.

3.3 Reducing sub-gap density of states

Another way to steep subthreshold swing by reducing the subgap DOS at the channel seems very promising for solution-processed low-voltage OFETs as very thick gate dielectrics are also available in this case, which can thus be reliably coated with high reproducibility. Low-voltage OFETs with small subgap DOS ($N_{sub} < 10^{12} \text{ cm}^{-2} \text{eV}^{-1}$) have been reported without utilization of large gate capacitance but with engineered small molecule/polymer blends or high crystalline small molecule semiconductors (Table 3).

developed	developed low-voltage printable OFE is using thick gate dielectrics of small gate capacitances.								
Structure	Semiconductor	Dielectric	t	C_{diel}	SS	$N_{ m sub}$	Year		
	(Blend ratio wt.%)		(nm)	(nF/cm ²)	(mV/dec)	$(\mathrm{cm}^{-2}\mathrm{eV}^{-1})$			
BGTC	TES-ADT	c-PDMSS	400	N/A	190	N/A	2010124		
BGTC	TES-ADT	PS/SiO ₂	-/300	10-11	200	1.5×10 ¹¹	2014125		
BGBC	Ph-BTBT-10	PS/SiO ₂	30/300	25	79	5×10 ¹⁰	2016 ¹²⁶		
BGBC	diF-TES ADT	SiO ₂	200	17.3	430	6.8×10 ¹¹	2013127		
BGBC	DTBDT-C ₆	Parylene-C	560	N/A	170	N/A	2015113		

Table 3. Summary of device performance (SS, subthreshold swing; N_{sub} , sub-gap density of states) and material processes (t, gate dielectric thickness; C_{diel} , gate dielectric capacitance) for the recently developed low-voltage printable OFETs using thick gate dielectrics of small gate capacitances.

BGBC	TIPS-pen/PS(3:1)	PVA	407	12.2	100	5.2×10 ¹¹	2013128
BGBC	TIPS-pen/PS(3:1)	SU8	1160	2.97	250	5.8×10 ¹⁰	201650
BGBC	TIPS-pen/PS(3:1)	PVCN	295	10.2	100	3.9×10 ¹⁰	201651
BGBC	DTBDT-C ₆ /PS(4:1)	Parylene-C	350	6.3	100	2.7×10^{10}	201683
BGBC	DTBDT-C ₆ /PS(3:1)	Parylene-C	150	24	100	1×10^{11}	201782
BGBC	TIPS-pen/PS(3:1)	PVCN	N/A	N/A	116	7.78×10 ¹⁰	201755

3.3.1 Small molecule/polymer blend channel



Figure 6. Printable low-voltage OFETs realized by reducing N_{sub} and fabricated in bottom-gate bottom-contact (BGBC) structure. (a) Small molecule/polymer blend (TIPS-pentacene/PS) OFET with a 1.1 µm thick SU8 gate dielectric (2.9 nF/cm²). Reprinted with permission.⁵⁰ Copyright 2016, Wiley-VCH. (b) TIPS-pentacene/PS OFET with a P(VDF-TrFE-CFE)/PVCN bilayer gate dielectric (46.3 nF/cm²). Reprinted with permission.⁵³ Copyright 2016, IEEE.

The blending of small molecule semiconducting materials with amorphous polymers was originally introduced to combine the good semiconducting properties of the former with the ease of processing and film uniformity of the latter.¹²⁹ A particularly successful group of blend systems involved acene-based semiconductor blended with semiconducting or insulating polymers. It was found that dependent of the processing parameters, a bilayer or trilayer stratification may be induced by the vertical phase-separation phenomenon.¹³⁰ However, the trilayer stratification with a buried thin layer of highly crystallized acene formed at the semiconductor–dielectric interface was more preferred to yield higher performances. In general, OFETs made of this kind of semiconducting material sets with the proper stratification have been demonstrated to exhibit higher mobility and better uniformity, compared to those with neat semiconductors.¹³¹⁻¹³⁵

Interestingly, this blending strategy has also been shown to be very efficient for reducing the N_{sub} of TIPS-pentacene by utilizing PS as the other component, providing a feasible way to improve

the OFET's subtreshold swing performance.¹³⁶ As demonstrated by Guo's group, the developed TIPS-pentacene/PS (3:1, wt.%) blends OFETs based on a thick low-*k* polyvinyl alcohol (PVA) dielectric (407 nm, $k \sim 5.6$) not only presented a predictable high mobility of 1 cm²Vs⁻¹, but also realized a very small subtreshold swing value of about 100 mV/dec.^{128, 137} Note that the low-voltage operation (< 2 V) was achieved relying on relatively small gate capacitance as low as 12.2 nF/cm². The utilization of thick PVA dielectrics was beneficial for effectively eliminating the possible influence of intermixing of printed Ag inks with the dielectric layer, and thus enabled the implement of low-voltage all-solution processed OFETs and inverters.^{40, 63, 138} Because hydroxyl groups are richly contained in the polar PVA film, which easily absorbs water, the developed low-voltage OFET devices with PVA dielectric present much poorer operational and storage stabilities.⁵¹ In the following work, the authors further developed and used less polar cross-linkable polymer dielectrics, such as PS, poly(methylmethacrylate) (PMMA), poly(iso-butylmethacrylate) (PiBMA) and poly(4-methylstyrene) (PMS), poly(vinyl cinnamate) (PVCN), to replace the PVA dielectric and build OFETs with improved stability.^{51, 139-141}

In despite of various dielectrics, the developed OFETs based on TIPS-pentacene/PS semiconducting blends exhibited low voltage operation (< 5 V) experimentally, confirming the feasibility of reduced DOS related strategy for reducing the subthreshold swing. Recently, based on TIPS-pentacene/PS blends (3:1 wt.%), low-voltage printable OFETs (< 5 V) using SU8 dielectric with the thickness over 1 µm was firstly demonstrated by W. Tang et al., where the employed gate capacitance (2.9 nF/cm²) was the smallest among the reported works (Figure 6(a)).⁵⁰ It is also noteworthy that the developed low-voltage OFETs based on reduced- N_{sub} organic semiconducting layer using very 1.1 µm SU8 gate dielectrics can also sustain high voltage operation. The gate leakage current of low-voltage printed TIPS-pentacene/PS blends OFETs kept around 1 pA (seven orders of magnitude lower than the drain current) with the gate voltage changing from 20 to -40V.50 This hybrid low/high voltage operatable device technology was considered promising for developing flexible display systems, which comprised both relatively high voltage pixel driving circuits and low voltage logic circuits in the peripheral drivers.¹⁴² Attributed to the formed highquality semiconductor/dielectric interface and the very low gate field (< 0.05 MV/cm) across the thick gate dielectric layer, the probability of charge trapping into localized states was significantly reduced and excellent operational stability achieved.25

Despite the idea of introducing reduced-DOS semiconducting layer to obtain small *SS*, combination of employment of high capacitance dielectrics would help efficiently to control the accumulation of carriers in channel for extremely smaller *SS*. On the other hand, using high-*k* dielectric is mandatory in aggressively down scaled OFETs to inhibit short channel effects. With the help of the large gate capacitance (46.3 nF/cm²) of PVDF-terpolymer/PVCN bilayer gate dielectric and reduced N_{sub} of TIPS-pentacene/PS semiconducting blends, Zhao *et al.* demonstrated that the best extracted SS value for the optimized OFETs reached as low as 64 mV/dec, which was close to the room-temperature theoretic limit of 59.6 mV/dec (Figure 6(b)).⁵³ Not surprisingly, the developed low-voltage OFETs appeared to be more compatible with printing/solution coating process and show excellent bias stress stability.¹⁴³

3.3.2 Neat small molecule channel



Figure 7. Printable low-voltage OFETs realized by reducing N_{sub} neat small molecule channel. (a) Neat small molecule (Ph-BTBT-10) OFET in bottom-gate bottom-contact (BGBC) structure. Reprinted with permission.¹²⁶ Copyright 2016, IEEE. (c) Neat small molecule (TES-ADT) OFET in bottom-gate top-contact (BGTC) structure. Reprinted with permission.¹²⁵ Copyright 2017, Wiley-VCH.

High-quality channel with ultra-low trap density could also be processed from neat organic semiconducting materials, where similar small SS is expected to present in the implemented OFETs. The previously reported solution-processed low-voltage OFETs were mostly fabricated based on acene-based small molecules (Table 3). As reported by Kim et al., when TES-ADT films were spincast onto the smooth PDMSS/PMFA blend dielectrics, the resulting OFETs could be operated in the voltage ranging from 2 to -5 V due to a notably low SS of 140 mV/dec.¹²⁴ In a subsequent work, Jang et al. also demonstrated that by exposing the deposited TES-ADT film mildly to vaporized 1,2-dichloroethane (DCE) solvent, the developed TES-ADT OFET could operate at low voltages (< 5 V) with a small SS of 200 mV/dec (Figure 7(a)).¹²⁵ They ascribed this good performance to significantly reduced trap density in channel composed of large crystals whose sizes were up to several thousand micrometers. In the work of Diemer et al., diF-TES ADT crystalline order induced during film growth was significantly improved by a newly developed vibration assisted crystallization (VAC) method that involved vibrating the substrate in the crystal growth chamber at a controlled direction, amplitude, and frequency. As a result, the estimated subthreshold swing (430 mV/dec) performance for VAC diF-TES ADT OFETs was twofold improved compared to that of the solvent-assisted crystallized devices (1 V/dec).

The search for high-quality solution processable organic semiconductor to build low-voltage high performance OFETs has stimulated the advance of research activities. Recently, new kinds of organic semiconductors with extremely high crystalline quality have been demonstrated available for fabricating low-voltage OFETs without relying on large gate capacitance. In the work of Kunii *et al.*, a new kind of polycrystalline semiconductor (2-decyl-7-pehnl-[1] benzothieno[3,2-b][1] benzothiophene, Ph-BTBT-10) with highly ordered smectic E liquid crystalline phase was successfully used for realizing low-voltage (< 2 V) OFETs, where the *SS* was as low as 79 mV/dec close to the theoretical limit (Figure 7(b)).¹²⁶ In the work of Fukuda *et al.*, it was found that the printed DTBDT-C₆ OFETs exhibited low operation voltage (< 2 V) with a nearly ideal threshold

voltage (-0.16 V) and quite low subthreshold swing (170 mV/dec) despite of using a thick low-*k* parylene-C gate dielectric (560 nm).¹¹³ However, the printed OFET devices used inkjet-printed silver source/drain electrodes and exhibited high contact resistance and low carrier mobility. The authors went a step further to address the contact issue by blending DTBDT-C₆ with PS insulators. Compared to the neat DTBDT-C₆ OFET, the contact resistance was significantly reduced from 238 k Ω •cm to 20 k Ω •cm while the mobility was improved from 0.22 ± 0.06 cm²V⁻¹s⁻¹ up to 1.0 ± 0.2 cm²V⁻¹s⁻¹ for DTBDT-C₆/PS blend OFET at a short channel length of 9 µm.⁸³

3.3.3 Structure dependence

It should be pointed out that most of the presented low-voltage OFETs enabled by reducing the N_{sub} instead of enlarging the gate capacitance were constructed in co-planar structure as discussed above. However, this approach would be problematic for OFETs implemented in staggered structures if semiconductor/polymer blends were used for the semiconducting layers. As the vertical phase-separation finally results in an insulating polymer-rich layer in the blend channel, a dielectric-like layer is then formed essentially, which also contributes an additional capacitance. It is not difficult to see that this additional capacitance in the channel layer is in series with the capacitance of gate dielectric. Therefore, the resulted effective gate capacitance should be greatly reduced whatever bilayer or trilayer stratification is finally formed. In this case, the choice of gate dielectric turns out to be vital for achieving steep OFET swing and low operation voltage.

In the work of Tiwari *et al.*, though the TIPS-pentacene/PS blend (3:1 wt. %) OFET of staggered structure showed a smaller subthreshold swing (1.4 V/dec) than that of neat TIPS-pentacene OFET (4.1 V/dev), it was yet too large to operate the devices with low voltages.¹⁴⁴ The measured gate capacitances, which were obtained from maximum capacitance values in accumulation region according to C-V characteristics of metal-insulator-semiconductor structures, were in fact much smaller than that of neat TIPS-pentacene OFET or the calculated values of sole dielectric.^{145, 146} Moreover, with increase of the TIPS-pentacene/PS ratio, the estimated gate capacitance changed from 200 nF/cm² for neat TIPS-pentacene OFET to 21 nF/cm² for TIPS-pentacene/PS blend (1:3 wt. %) device.¹⁴⁷ These results were evident that the contained insulating polymeric materials in the blend channel also played an important role in determining the subthreshold swing behavior for staggered OFETs. This may be the reason why it was challenging to use high performance small molecule semiconductor/polymer blends to fabricate low-voltage OFETs in staggered structure (i.e. bottom-gate top-contact structure).¹⁴⁸

On the other hand, the aforementioned rule didn't apply to low-voltage OFET devices using highly-crystallized neat semiconducting channel since no insulating polymer matrix was used. As presented by Jang *et al.*, they demonstrated that by significantly lowing trap density in the TES-ADT-only channel, which exhibited large crystal sizes of up to several thousand micrometers, and a face-to-face, π -overlapped structure, the resulting OFET in a staggered configuration could also operate at low voltages (< 5 V) with a small SS of 200 mV/dec.¹²⁵ In the work of Kunii *et al.*, the Ph-BTBT-10 film with highly ordered smectic E liquid crystalline phase had also been demonstrated available for building bottom-gate top-contact low-voltage (< 2 V) OFETs, where the *SS* was as low as 79 mV/dec close to the theoretical limit.¹²⁶ Therefore, this approach of reducing *N*_{sub} is feasible to fabricate low-voltage printable OFETs with proper matching of semiconducting material sets and various device configurations.

4. Printable OFET biochemical sensors and sensing system

As OFETs' functional layers and interfaces among them could be conceived to engineer, they are promising to function as core elements for developing a broad range of biochemical sensing devices, as shown in Table 4. More niche biochemical applications (e.g., skin-inspired electronics, imperceptible, implantable, or wearable electronics) were demonstrated by OFET technology.^{4, 94, 149} Here, an illustration of recent efforts in OFET-based biochemical sensors as well as sensory systems is given with emphasis on low-voltage devices that are fully (or partly in some case) printed.

Structure	OSC	Sensitive interface	Membrane	Analyte	$ V_{\rm GS} ({ m V})$	Performance
BGBC ¹⁵⁰	D _{3A} oligomer	OSC/Analyte	D _{3A} oligomer	NO _x	40	LOD: 250 ppb
BGTC ¹⁵¹	P3HT/PS	OSC/Analyte	P3HT/PS	NH ₃	40	<i>R</i> : 5-50 ppm
BGBC ⁵¹	TIPS-pentacene/PS	OSC/Analyte	TIPS-pentacene/PS	NH ₃	5	<i>R</i> : 5-25 ppm
BGTC ¹⁵²	DPP2T-TT	OSC/Analyte	DPP2T-TT	NH ₃	5	LOD: < 1 ppb
BGBC ¹⁵³	P3HT/SXFA	OSC/Analyte	P3HT/SXFA	TNT	40	LOD: 0.5 ppb
BGTC ¹⁵⁴	PSFDTBT	OSC/Analyte	PSFDTBT	H_2S	30	LOD: 1 ppb
BGTC ¹⁵⁵	PDPP3T1	OSC/Analyte	PDPP3T1	Ethaol	60	LOD: 1 ppb
BGTC ¹⁵⁶	PBIBDF-BT	OSC/Analyte	PBIBDF-BT	Humidity	100	<i>R</i> : 32%-69%
BGTC ¹⁵⁷	P3HT-azide/C[8]A	OSC/Electrolyte	P3HT-azide/C[8]A	Toxic solvents	0.5	-
BGBC ¹⁵⁸	pII2T-Si	OSC/ Electrolyte	Abs/pII2T-Si	Tyrosine kinase	2	LOD: 2.5 ng/mL
BGBC ¹⁵⁹	pII2T-Si	OSC/Electrolyte	DNA-Au/pII2T-Si	Hg^{2+}	1	LOD: 10 µM
BGBC ¹⁶⁰	РЗНТ	Electrode/OSC	Au/P3HT	DNA	40	-
BGTC ¹⁶¹	РЗНТ	OSC/Dielectric	PL/P3HT	Diethyl ether	100	<i>R</i> : 0.6–3 wt. %
BGTC ¹⁶²	РЗНТ	OSC/Dielectric	SA/P3HT	Biotin	100	LOD: 15 pM
TGBC ¹⁶³	РЗНТ	OSC/Dielectric	PVP/P3HT	Glucose	2	<i>R</i> : 8 µM-30 mM
ISOFET ¹⁶⁴	РЗНТ	Electrolyte/dielectric	Ta_2O_5	\mathbf{K}^+	5	S: 29 A/mM
ISOFET ¹⁶⁵	РЗНТ	Electrolyte/dielectric	Ta_2O_5	Glucose	1	LOD: 10 mM
EGOFET ¹⁶⁶	TIPS-pentacene/PS	Electrolyte/electrode	ITO	H^{+}	5	S: 51.5 mV/pH
EGOFET ¹⁶⁷	PBTTT	Electrolyte/electrode	PBA/Au	Glucose	3	LOD: 5 mM
EGOFET ¹⁶⁸	PBTTT	Electrolyte/electrode	Streptavidin/Au	Protein (IgG)	3	LOD: 8 nM
EGOFET ¹⁶⁹	PBTTT	Electrolyte/electrode	Streptavidin/Au	Protein (IgG)	3	LOD: 4 nM
EGOFET ¹⁷⁰	PBTTT	Electrolyte/electrode	Zn ^{II} -DPA/Au	Protein (α-caseir	n) 1	LOD: 0.22 ppm
EGOFET	PBTTT	Electrolyte/electrode	Ni ^{II} -nta/Au	Protein (BSA)	1	LOD: 0.6 pM
EGOFET ¹⁹	PBTTT	Electrolyte/electrode	DPA/Au	Hg^{2+}	1	LOD: 9.9 ppb
EGOFET ²⁰	PBTTT	Electrolyte/electrode	HPOP/Au	Lactate	3	LOD: 66 nM
EGOFET ²¹	PBTTT	Electrolyte/electrode	Nitrate	NO ₃ -	3	LOD: 45 ppb
			reductase/Au			
OCMT ¹⁷¹	TIPS-pentacene	Electrolyte/electrode	ss-DNA/Au	DNA	2	<i>R</i> : 0.1-1000 nM
OCMT ²²	TIPS-pentacene	Electrolyte/electrode	ss-DNA/Au	DNA	2	LOD: 155 fM
OCMT ²³	TIPS-pentacene	Electrolyte/electrode	Parylene C	H^{+}	1	<i>S</i> : 1.4 V/pH

Table 4. Summary of printable OFET-based biochemical sensors.

NOTE: V_{GS} , Gate-source voltage; BGBC, Bottom-gate bottom-contact; BGTC, Bottom-gate top-contact; TGBC, Top-gate bottomcontact; ISOFET, Ion-sensitive OFET; EGOFET, Extended-gate OFET; OSC, Organic semiconductor; LOD, Limit of detection; R, Detection range; S, Sensitivity.

4.1 Solution processed/printable OFET sensors

There have been various possible transducing mechanisms proposed to develop OFET-based chemical and biological sensors, however, what is unequivocal from the reported work is that bottom-gate structure has been extensively adopted with the exposed channel as the sensing area for relatively high sensitivities as shown in Table 4. In this case, the sensing process relies on the interaction of target species either directly with the organic semiconducting layer or with the biological receptors modified upon, which finally affects the field-effect mobility of carriers in channel as well as the threshold voltage.¹⁷²



Figure 8. Representative low-voltage OFET biochemical sensors. (a) Conventional OFET sensor using sensitive channel for detecting Hg²⁺ in seawater (1 mM). Reprinted with permission.¹⁵⁹ Copyright 2016, Nature Publishing Group. (b) An extended-gate OFET with immobilization of streptavidin on the surface of Au electrode for IgG detection. Reprinted with permission.¹⁶⁸ Copyright 2014, American Institute of Physics. (c) An organic charge-modulated field-effect transistor (OCMT) for pH sensing. Reprinted with permission.²³ Copyright 2017, Elsevier.

It is challenging for the prominent OFET-based biochemical sensors to directly measure ions or molecules in aqueous electrolytes because most organic semiconductors cannot survive the conventional chemical modification and measurement processes. To circumvent this limitations, Shen and co-workers used stable poly-(diketopyrrolopyrrole-terthiophene) (PDPP3T) and chemically modified it with NCCL by using a plasma-assisted in situ microdamage interfacial grafting approach.²⁴ The fabricated low-voltage (< 5 V) bottom-gate OFETs with immobilized receptors could function as the sensing antenna for selective detection of adenosine triphosphate (ATP) with a low detection limit of 0.1 nM. As discussed above, there is increasing concern associated with bottom-gate OFET sensors that long time stability and durability may be

problematic during prolonged detection times, suggesting the use of organic films with excellent chemical solvent-resistance and electrical stability. Moreover, low-voltage operation is a crucial issue since high operating voltage limits the sensing reliability and reproducibility.^{173, 174} In this respect, solvent-resistant cross-linked P3HT-azide co-polymer was utilized by Lee et al. to develop low-voltage ($V_{DS} = -0.6$ V, $V_{GS} = -0.5$ V) OFET sensors, which demonstrated the direct sensing of liquid analytes for various liquid-phase toxic solvents and pH solutions.¹⁵⁷ Recently, important advances have been also made on the synthesis of novel organic semiconductors. As proposed by the Bao's group, isoindigo-based conjugated polymer with solubilizing siloxane-terminated side chains (PII2T-Si) was successfully employed to fabricate low-voltage (< 4 V) flexible solutionprocessable OFETs, which presented unexpected and remarkably stable electrical performance, not only under ambient conditions but also in direct contact with aqueous media (Figure 8(a)).¹⁵⁹ By incorporating DNA-functionalized gold nanoparticles (AuNPs) on the organic semiconductor's surface, the fabricated OFET can thus be stably operated to reproducibly and selectively detect Hg^{2+} contamination in the harshest seawater environments, allowing a detection limit down to 10 µM. Another example of OFET biosensor was carried out by the same group in which the biomarker (sFlt1) was successfully detected by inkjet printed large-area arrays of PII2T-Si OFETs.¹⁵⁸

With the aim to improving the sensing reliability, alternatively, there have been many attempts to employ interesting OFET structures irrespective of the use of strictly limited organic semiconductors. For instances, the OFET-based extended-gate structures have been often presented in many researches with the sensing area separated from the transistor itself. In this case, the operation mechanism of extended-gate-type OFET (EGOFET) sensors can be explained by the threshold voltage shift resulting from either an interfacial potential shift at the gate/electrolyte interface or charge coupling by the terminal portion.^{175, 176} In chemical/biological sensors, different extended gates or utilization of different receptors to modify on them would yield different potentiometric sensing systems.^{164, 177} For examples, T. Minami and co-workers developed a series of high performance chemical and biological sensors based on extended gate OFETs, which were solution processed and could operate at low voltages (< 3 V) by using a hybrid dielectric composed of very thin AlO_x (< 10 nm) and C₁₄-PA SAMs (Figure 8(b)).^{19-21, 168, 169, 178-180} The authors reported on the demonstration of antibody detection (biotinylated immunoglobulin G, IgG), α -casein protein, bovine serum albumin (BSA), saccharide, mercury (II) ions (Hg^{2+}), and nitrate ion (NO_3^{-}). When the H⁺ sensitive ITO electrode was used as the extended gate in a low-voltage all additive printing/coating processed TIPS-pentacene/PS blend OFET, J. Zhao demonstrated that the ionsensitive OFET sensor could detect pH variation less than 0.1 pH when it operated in the highly sensitive subthreshold regime (SS < 83 mV/dec).¹⁴³

The conventional types of extended-gate OFET sensors have shown improved stability, however, the previously mentioned devices with this architecture suffer from disadvantages of bringing an additional degree of complication due to the requirement for reference electrodes in the solution sensing area. In this regard, Bonfiglio's group made an advancement by proposing a new concept of organic charge-modulated field-effect transistor (OCMT) free of the external reference electrode, which introduces a remote floating gate to detect charged analytes through capacitive coupling.¹⁸¹ Charge variations on the floating gate may be exploited for realizing detections of pH and DNA in liquid media and presumably the electrical activity of cells.¹⁸² Based on a hybrid AlO_x/Parylene-C (6 nm/25 nm) gate dielectric and TIPS-pentacene semiconductor layer, the OFET core of the structure could be operated at ultra-low voltage (< 2 V) and realized DNA hybridization

detection even with a single nucleotide polymorphism.¹⁷¹ It is worth to note that during the sensing process, the organic semiconductor was not exposed to the liquids where DNA was hosted thanks to the extended floating Au gate. In subsequent work, the authors could tailor the OCMT biosensor's performance by optimizing the layout and obtained record performance for direct DNA hybridization detection with an extrapolated detection limit of 155 fM.²² As an alternative to conventional ISFET, OCMT had recently been adapted for pH sensors by using a plasma activated parylene-C sensing layer.²³ The OFET pH sensor with an optimized geometry was reported to present an unexpected sensitivity of 1.4 V/pH, which overcame the typical sensitivity (limited to 20 mV/pH) of untreated parylene C and exceeded the Nernst limit (Figure 8(c)).

4.2 Printed low-voltage OFET sensing systems

Although printable OFETs are very promising to develop many physical and chemical sensors for the fabrication of custom sensor systems, currently a series of high-level functionality more useful for stand-alone systems such as accurate analog-to-digital conversion, complex signal processing, power management and wireless communication to address these sensors cannot be realized by the entirely printed OFET technology. For the envisioned applications, a hybrid technology is thus proposed to combine organic functional devices with silicon chips in order to retain the benefits of print manufacturing without sacrificing performance, representing the future development direction in this field.^{183, 184} For instance, Li *et al.* developed a hybrid pH sensing system by integrating the plastic pH sensing tag, which comprised the ITO-gated low-voltage OFET and a solid Ag/AgCl/PVB thin film reference electrode, into Si-chips in a battery powered handheld system, demonstrating reliable pH monitoring (Figure 9(a)).¹⁶⁶

Nevertheless, there is a remaining window for printable OFETs to realize interface circuits and process local signals. In this sense, OFET amplifiers are crucial to improve the sensitivity and reliability (especially the signal-to-noise ratio) and enable the front-end organic sensors to interface with peripheral readout systems.¹⁴⁹ Based on low-voltage printed OFET inverters and amplifiers, a few fully-printable sensory systems for biochemical detection have been demonstrated. A simplest zero- V_{GS} inverter based amplifier composed of an extended-gate pH-sensitive OFET and a load OFET was developed by Tang *et al.* on PEN plastics, based on the printable low-voltage TIPS-pentacene/PS blend OFETs with very excellent bias stressing stability. This sensing tag interfaced with a 3.3 V battery-powered readout circuit board, which communicated with a mobile phone through NFC, and showed a good linearity over a wide pH range from 2 to 12 (Figure 9(b)).²⁵

To suppress background noise and improve the sensitivity of the protein-sensors, K. Fukuda fabricated a differential amplifier with an extended Au-gate functionalized with streptavidin based on the printed low-voltage DTBDT-C₆ OFETs with uniform electrical performance.¹¹³ They used the developed sensing system to detect small amounts of unlabeled immunoglobulin (IgG) and found a good linear relationship between the target concentration and the differential signal of output voltage at concentrations of less than 15 μ g/mL. Recently, in a novel potentiometric electrochemical K⁺ sensing system (Figure 9(c)), Shiwaku *et al.* employed a printed OFET-based amplification unit with negative-feedback to improve the sensitivity.¹⁸⁵ The amplifier was designed with a pseudo-CMOS structure and configured only by low-voltage p-type OFETs using DTBDT-C₆/PS blends. It was observed that a tunable gain of 3.1–8.3 with a high linearity endowed by the developed amplification system enabled the ion concentration sensitivity of the sensor to amplify from 34 mV/dec to 160 mV/dec.



Figure 9. Printed low-voltage OFET sensory systems. (a) Hybrid pH sensing system consisting of integrated extended-gate ion-sensitive OFET (EGOFET) and Si-chip readout circuit board. Reprinted with permission.¹⁶⁶ Copyright 2018, IEEE. (b) Flexible pH sensitive OFET inverter powered by a 3.3 V readout circuit board, which communicates with a smart phone through near field communication (NFC). Reprinted with permission.²⁵ Copyright 2016, IEEE. (c) Printed low-voltage pseudo-CMOS amplifier based K⁺ sensing system. Reprinted with permission.¹⁸⁵ Copyright 2018, Nature Publishing Group.

5. Conclusions and future outlook

In summary, printable OFETs assist the new development of niche electronics where otherwise silicon technologies are not applicable. Among the emerging applications biochemical sensing and low-end signal processing are good candidate for printable OFETs. With the aim of developing low-power printable sensory system on one chip, progress of finer resolution for high performance OFETs and strategies of material engineering for achieving steep subthreshold swing have been summarized. High-resolution printable OFETs have been widely studied and demonstrated capable of fast operation speed of higher than 1 MHz, which is high enough for monitoring the biochemical response and building OFET circuits to interface the sensors. Based on the printable low-voltage OFETs, various biochemical sensors have been reported, showing the flexible suitability of OFET sensing platform by modulating device configurations and engineering specific functional layers. It is noticeable that steep subthreshold swing is desirable for both OFET sensing devices and interface circuits, enabling them to be low-voltage powered and improve reliability. Up to date, it is feasible

to achieve steep subthreshold swing through printing process by either using high-k polymeric dielectrics or reducing the channel subgap density of states via material engineering. By combination of the two means, subthreshold swing is expected to approach the theoretical limit.

Further works in this field could be devoted to the following studies: (i) As OFETs are printed with finer resolution, the negative influence of relatively high contact resistances becomes an additional challenge. Thus, reduction of injection barrier to approach ohmic contact should be performed by various contact engineering; (ii) Fully-printable low-voltage OFETs have been realized by using organic channels of sub-gap DOS for p-type organic semiconductors while few reported for n-type ones. It is urgent to exploit the latter ones to fabricate low-voltage CMOS-like inverters for building high performance printed amplifiers towards low-power biochemical sensing applications; (iii) Last but not the least, OFET biochemical sensors are mostly reported to detect single analyte, sacrificing the array potential for printed OFET technology. Therefore, multiplexing arrays capable of mapping single analyte distribution or realizing multi-detection at the same time would be more meaningful.

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