# A General Strategy to Achieve Colossal Permittivity and Low Dielectric Loss Through Constructing Insulator/Semiconductor/Insulator Multilayer Structures

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Abstract:

In the heavily reduced rutile $TiO_2$ ceramics annealed in $Ar/H_2$ hybrid atmosphere, the maximum dielectric permittivity (~$3.0\times10^4$) obtained is about 100 times higher than that (~300) of the unannealed $TiO_2$ ceramic. The measured dielectric losses of most samples are below 0.07 over most of the measured frequency range ($10^2$-$10^6$ Hz). The minimum dielectric loss is 0.03 (at $10^4$-$10^5$ Hz). Furthermore, such colossal permittivity (CP) is almost independent of the frequency (100-$10^6$ Hz) and the temperature (20K-350K). We suggest that the colossal permittivity is attributed to the large carrier (Oxygen vacancies and freedom electrons) concentration of the inner semi-conductor and the low dielectric loss is due to the presentation of the insulator layer in the surface. A new mechanism of the insulator/semi-conductor/insulator (ISI) sandwich structure for the colossal permittivity is proposed, which is confirmed by the experiment using the typical silicon (Si) semi-conductor plate deposited with top and bottom insulator layer $Ga_2O_3$, successfully, both CP and low dielectric loss are also achieved at the same time in $Ga_2O_3/Si/Ga_2O_3$ structure.

## Introduction

In recent years, intensive research is being conducted in the area of alternative dielectric materials with colossal permittivity (CP), low loss and relatively weak dependence of frequency- and temperature for potential applications in advanced microelectronics and high-energy-density storage applications. Nowadays, several mechanisms used to explain colossal permittivity (CP>$10^3$) have been proposed, resulting in the discovery of new CP materials[1-5], such as $BaTiO_3$-doped perovskites[1], $CaCu_3Ti_4O_{12}$ (CCTO[2,6]), NiO[3], $La_{2x}Sr_xNiO_4$[4] (x=1/3 or 1/8) and co-doped $TiO_2$[5]. A high-performance dielectric material should exhibit temperature- and frequency-stable, high permittivity as well as low dielectric loss (<$10^{-1}$). Nevertheless, achieving CP meanwhile getting low dielectric loss in a single material is still an extremely challenging task, comparatively, the latter is far harder than the former. According to the mechanisms of CP materials mentioned above, such as barrier layer capacitance (BLC[1,6]), nano-scale disorder[7], Mott-variable-range-hopping (Mott-VRH[8]), electron-pinned, defect-dipole[5], etc., a low dielectric loss may be obtained only if the charges polarized by an external electric field can be localized in a microcosmic range, for examples, the domains, the grain boundaries or the interfaces between the materials and the electrodes.

As we known, there is another mechanism relating to thermally activated carrier hopping associated with substitutional defect states could lead to CP, however, the dielectric loss must necessarily also be high due to the Kramers-Kronig relation[8,9]. If these carriers hopping can be replaced by localized lattice defect states[10,11], a CP, an acceptable dielectric loss and a less frequency/temperature dependence can be obtained simultaneously. Furthermore, carrier hopping could be confined/localized by extrinsic defect states, leading to both CP and low dielectric loss[5], although there have been some debatable issues about the electron-pinned, defect-dipole, till now. In principle, when these localized carriers (including positive charges and negative ones) are applied by an external electric field, the positive charges and the negative ones are separated, oriented and alternate. Therefore, there are no any net charges in the inner of CP materials, but only in the top and bottom surface. It is conceivable that both CP and low dielectric loss can also be achieved if the movable carriers can be confined in the top and bottom surface, which may be possible to be realized easily.

In this work, we present the experimental results and theory calculations to confirm the above hypothesis. In the heavily reduced $TiO_2$ ceramics, there is hugely difference in the carrier concentrations between in the surface and in the inner. In the inner of heavily reduced $TiO_2$ ceramics, there is a great deal of oxygen vacancies (one oxygen vacancy with one or two positive charges) and freedom electrons (negative charges), which is similar to an n-type doped semiconductor. However, in the top and bottom surface of heavily reduced $TiO_2$ ceramics, there is an almost absolute insulator thin layer, where no obvious carriers can be detected. Both CP and low dielectric loss are achieved at the same time in the heavily reduced $TiO_2$ ceramics. Similarly, in the typical silicon (Si) semi-conductor plate deposited with top and bottom insulator layer $Ga_2O_3$, CP with low dielectric loss is also observed. A new mechanism of CP is proposed to explain the CP in the insulator/semi-conductor/insulator (ISI) sandwich structure.

## 1. Experiments

Raw materials used in this work are rutile $TiO_2$ (99.99%, Aldrich). Pure rutile $TiO_2$ ceramics were prepared by a conventional solid-state method and the optimized sintering condition is 1400 $^oC$ in air for 10h with a rising rate of 3 $^oC\ min^{-1}$. Then, $TiO_2$ ceramics were annealed at 1150 $^oC$ in Ar (with 0.1% $H_2$) for 1h, 2h, 5h, 10h and 20h, respectively.

The crystal structures of rutile $TiO_2$ ceramics were evaluated by measuring x-ray diffraction (XRD) spectra with Ni filtered $CuK_\alpha$ radiation. The surface morphologies of rutile $TiO_2$ ceramics were investigated using a scanning electron microscope (SEM) image checked by Hitachi S-570. Frequency (or temperature) dependence of the dielectric properties and complex impedance were measured by HP4294. X-ray photoelectron spectroscopy (XPS, Escalab 250 XI) was also collected of rutile $TiO_2$ ceramics for checking the valance states of Ti ions and evaluating roughly the content of O ions (or Oxygen vacancies).

## 2. Results and discussions

Both XRD patterns (Supplementary Fig. S1) and surface SEM pictures (Supplementary Fig. S2) of all pure rutile $TiO_2$ ceramics suggest that the reduced annealing process cannot change the microstructure of $TiO_2$ ceramic, compared with that of the unannealed $TiO_2$ ceramic. However, the colors of all annealed $TiO_2$ ceramics are blacker than that of unannealed $TiO_2$ ceramic (Supplementary Fig. S1), which indicates that oxygen vacancies are presented in $TiO_2$ ceramic annealed in reducing gas or inactive gas.

Figure 1:

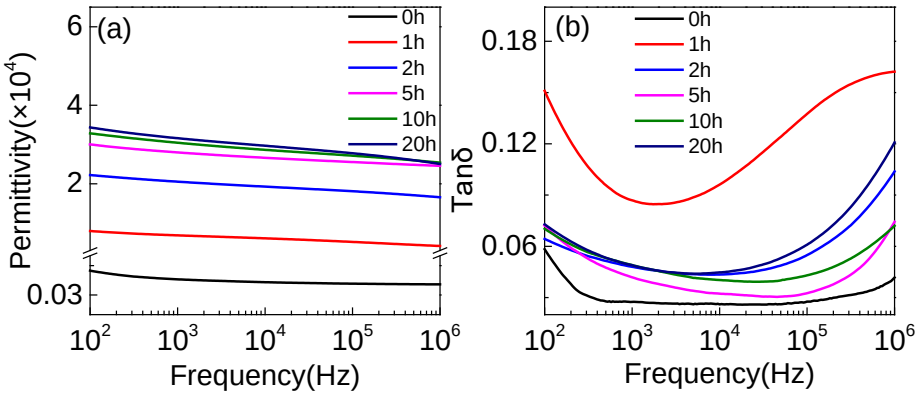


Figure 1 Frequency dependence of the dielectric properties at room temperature. Dielectric permittivity (a) and dielectric loss (b) of pure rutile $TiO_2$ ceramics annealed at 1150 $^oC$ in Ar (with 0.1% $H_2$) for 1h, 2h, 5h, 10h and 20h, respectively. Before annealed, $TiO_2$ ceramics were sintered at 1400 $^oC$ in air for 10h. As compared, dielectric properties of the unannealed $TiO_2$ ceramic were also shown here, labeled as "0h".

Figure 1 shows dielectric permittivity and dielectric loss of pure rutile $TiO_2$ ceramics annealed for various times in Ar (with 0.1% $H_2$) atmosphere. Compared with that of the unannealed $TiO_2$ ceramic, dielectric permittivity of all annealed $TiO_2$ ceramics are enhanced greatly at the expense of increasing dielectric loss slightly. The dielectric permittivity of $TiO_2$ ceramics increases with the increasing of annealing times (Supplementary Fig. S3). The maximum dielectric permittivity (~$3.0\times10^4$) obtained in $TiO_2$ ceramic annealed for 20h is about 100 times higher than that (~300) of the unannealed $TiO_2$ ceramic. Furthermore, such colossal permittivity (CP) is almost independent of the frequency (100-$10^6$ Hz). The measured dielectric losses of all samples (except

the sample annealed for 1h) are below 0.07 over most of the measured frequency range. The minimum dielectric loss is 0.03 (at $10^4$-$10^5$ Hz) in $TiO_2$ ceramic annealed for 5 h, meanwhile, dielectric permittivity of this sample is up to ~$2.7\times10^4$.

Figure 2:

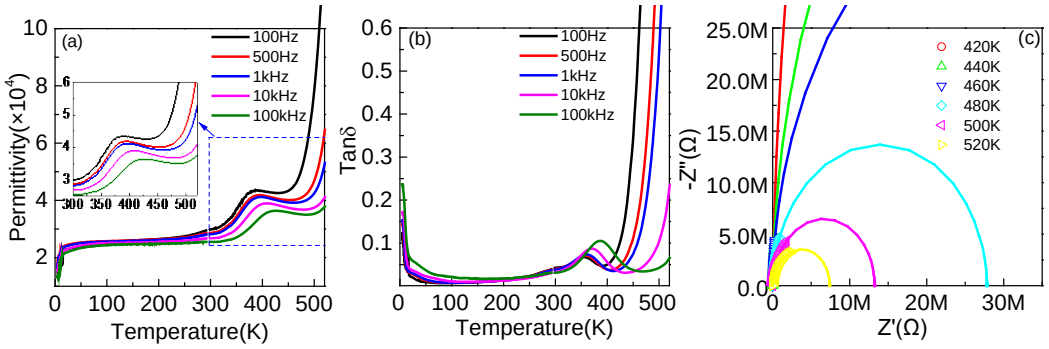


Figure 2 Temperature dependence of the dielectric properties of $TiO_2$ ceramic annealed for 5 h were measured from 5K to 520K. (a) Dielectric permittivity. (b) Dielectric loss. (c) Complex impedance plots [Z'(ω)-Z''(ω)](open dots) of $TiO_2$ ceramic annealed for 5h measured from 420 to 520 K, and corresponding fitting results (solid lines) using a Cole–Cole model. The inset in Fig. 2 (a) is the enlargement of temperature dependence of CP from 300 to 520 K, which data were extracted from the correspondence of Fig. 2(a).

It is signification that both CP and low dielectric loss of the annealed $TiO_2$ ceramics are almost independent of temperature over a wide temperature range, from 20 K up to 350 K, as shown in Figure 2 (a) and (b). Within the whole measured temperature range, from 5 K up to 520 K, there are three dielectric relaxations, which occur at about 20, 350, and 450 K, respectively. At even lower temperature (5 K), the dielectric permittivity decreases quickly from $2.5\times10^4$ to $1.5\times10^4$, which is still much higher than that (~100) of pure rutile $TiO_2$ single crystal.[12] Li[13]reported that the hydrogen-reduced rutile $TiO_2$ crystal with oxygen vacancies and $Ti^{3+}$ ions exhibited CP (~$10^4$) at room temperature, which was thought to be associated with the weak-binding electrons generated from the oxygen vacancies. In the hydrogen-reduced rutile $TiO_2$ crystal, a dielectric relaxation occurred at about 30 K, and the dielectric permittivity from ~$10^4$ down to ~$10^3$ (at 10 K). Meanwhile, in hydrogen-reduced rutile $TiO_2$ crystal, CP due to the weak-binding electrons was not independent of the frequency, where CP significantly dropped to ~100 at $10^6$ Hz accompanied by the increasing of dielectric loss (over 100%).[13] Obviously, CP associated with the weak-binding electrons is not suitable for the mechanism of CP in our annealed $TiO_2$ ceramics. The dielectric relaxations observed in the cases of CCTO[14] and doped NiO[3] lead to the permittivity rapidly falling from the CP level down to the level of one hundred at temperatures below 200 K and large frequency/temperature dispersion over a broad temperature range, which are usually attributed to BLC effect, including both IBLC (internal barrier layer capacitance) and SBLC (surface barrier layer capacitance). IBLC exists at the grain boundaries and SBLC is in the interface between the materials and the electrodes. Either IBLC or SBLC is attributed solely to Maxwell-Wagner interfacial polarization, where the complex impedance is suitable for using a Cole-Cole model. In our annealed $TiO_2$ ceramic, however, the fitting results of the complex impedance at both 5 K and 350 K are not accordant with a Cole-Cole model at all, where all fitting results can be drew as the straight lines (Supplementary Fig. S4). Actually, only the higher-temperature dielectric relaxation observed above 450 K, shown in Figure

2(c), can be attributed to Maxwell-Wagner interfacial polarization. It is due to grain boundary polarization mechanism, and an activation energy ($E_a$) deviated from the Arrhenius form was 0.88 eV (Supplementary Fig. S5) for the $TiO_2$ ceramic annealed for 5 h, which is close to that in (In,Nb) co-doped $TiO_2$ ceramics.[5]Obviously, within the temperature range from 5 to 450 K, a new mechanism behind the CP of our annealed $TiO_2$ ceramics should be brought to light. Although there is a great deal of oxygen vacancies in the annealed $TiO_2$ ceramics, which is similar to the co-doped $TiO_2$ ceramics[5,15-17], the electron-pinned defect-dipoles theory cannot be used to explain the CP of our annealed $TiO_2$ ceramics because no any foreign ion was doped designedly into $TiO_2$ ceramics. With increasing temperature above 20 K, the permittivity slightly increases, at which state positive temperature coefficient of permittivity implies thermally activated processes dominate, accompanied with a slightly increasing dielectric loss (Fig. 2 (b)). Note that the annealed $TiO_2$ samples exhibit a relatively small negative temperature coefficient of permittivity, between the second dielectric relaxation and the third one, as shown in the inset of Fig. 2 (a), which is contrary to that of permittivity below 350 K. Negative temperature coefficient of permittivity can be explained as a result of the dominant ionic polarization mechanism similar to that impure rutile $TiO_2$ crystal.[18]

Figure 3

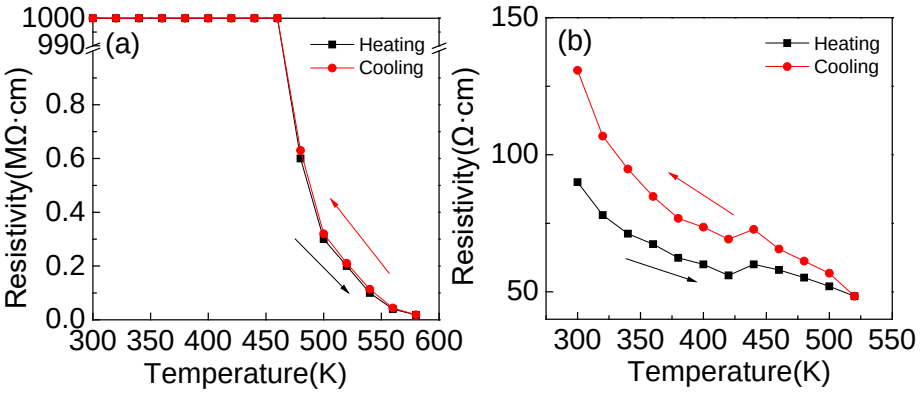


Figure 3 Temperature dependence of the resistivity of $TiO_2$ ceramic annealed for 5 h measured from 300 to 580K. (a) Surface resistivity. (b) Internal resistivity. Resistivity measurements were carried out two times. One is recorded with the temperature increasing (black line), and the other is recorded with the temperature decreasing (red line).

When we tried to measure the carrier concentrations of the annealed $TiO_2$ ceramics by Hall Effect, we found that, at room temperature, the surface resistivity of all $TiO_2$ ceramics, including the unannealed one, were far above $10^9$ Ω·cm (upper limit of our instrument). It implies that there is an insulator layer on the surface of the annealed $TiO_2$ ceramics, which is conflicting with the universal acknowledge reported in many documents[13,19-21], i.e. oxygen vacancies are certainly presented in $TiO_2$ materials when exposed in inactive or reduced gas at high temperature. Temperature dependence of the resistivity of $TiO_2$ ceramic annealed for 5 h was measured from 300 to 580 K, as shown in Fig. 3 (a). It suggests that the high resistivity state of the surface is not destroyed until the temperature increases above 460 K. At 580 K, the surface resistivity of $TiO_2$ ceramic annealed for 5 h drops ~$10^4$Ω·cm. When the temperature decreases from the measured maximum temperature (580 K), the surface resistivity can recovery completely, which means breakdown does not occur in the annealed $TiO_2$ ceramic. Surprisingly, the internal resistivity of the

annealed $TiO_2$ ceramics is as low as the level ~$10^2$ Ω·cm at room temperature, for example, that of $TiO_2$ ceramic annealed for 5 h is 91Ω·cm, as shown in Fig. 3 (b), which suggests a great number of carrier concentrations due to oxygen vacancies. When the temperature increases, the internal resistivity of the annealed $TiO_2$ ceramic only decreases a little. During the temperature decreasing process, the internal resistivity at every measured temperature point is higher a little than that of the corresponding one during the temperature increasing process. It maybe some oxygen vacancies were replaced by the extra oxygen absorbed from the air during the high temperature. The Hall Effect measurement results at room temperature show that, in the inner of $TiO_2$ ceramic annealed for 5 h, the carrier concentration is about $8.6x10^{18}$ $cm^{-3}$ , which is higher an order than that ($4.8x10^{17}$ $cm^{-3}$) of $TiO_2$ ceramic annealed for 1 h. Compared with the unannealed $TiO_2$ ceramic, each annealed $TiO_2$ ceramic appears a poor inner resistivity.

Here, we can conclude that, below 350 K, the CP accompanied by a low dielectric loss of the annealed $TiO_2$ ceramic is attributed to the very insulating surface layer and the much conductive inner part due to the heavily oxygen-deficiency. It should be questioned why the surface oxygen vacancies in annealed $TiO_2$ ceramics do disappear, after all, the extra oxygen cannot be supplied at all in an inactive or reduced gas during the annealing process. A vital detail is worthwhile to ponder, that the color of the $TiO_2$ ceramic sintered at 1400 °C in air became darken while it was just moved from the furnace (Supplementary Mov. S1). When the $TiO_2$ ceramic with dark color was heated again above 170 °C (440 K), the surface color can be recovered as a light yellow, which is the same as that of the $TiO_2$ ceramic just moved from the furnace. This surface color did change whether the $TiO_2$ ceramic is exposed to pure $O_2$ or $N_2$(Supplementary Mov. S2). After the temperature decreased to room temperature, deep brown color of the surface was present again (Supplementary Fig. S6 and Supplementary Mov. S3). Note that this surface color change does not occur when the sintering temperature of $TiO_2$ ceramic is below 1100 °C, which surface color keeps white (Supplementary Fig. S6). XPS analysis shows that there is a great amount of water in the surface of the $TiO_2$ ceramic sintered at 1400 °C (Supplementary Fig. S7). Comparatively, there is less water in the surface of the $TiO_2$ ceramic sintered below 1100 °C. The surface XPS data of Ti 2p for $TiO_2$ ceramics shows that almost all Ti ions in the surface of $TiO_2$ ceramics have +4 valance, and $Ti^{3+}$ (or $Ti^{2+}$) ions are not obviously detected (Supplementary Fig. S8). It implies that the vast majority of surface oxygen vacancies ($V_o^{\bullet\bullet}$) in $TiO_2$ ceramics cannot lost one or two electrons, therefore, the surface resistivity is very high. Therefore, we suggest that the very insulating surface layer of the annealed $TiO_2$ ceramic could be related to the water in the surface of $TiO_2$ ceramic. This surface water may be the absorption water from the air, which occurs in the unannealed $TiO_2$ ceramics. In the annealed $TiO_2$ ceramics, the surface water could be major attributed to the chemical reaction between the oxygen from the $TiO_2$ ceramic and the hydrogen from the $H_2$/Ar atmosphere. This judgment is major due to the experiment phenomena that the color of annealed $TiO_2$ ceramic is already dark before it is moved from the annealed furnace.

Figure 4：

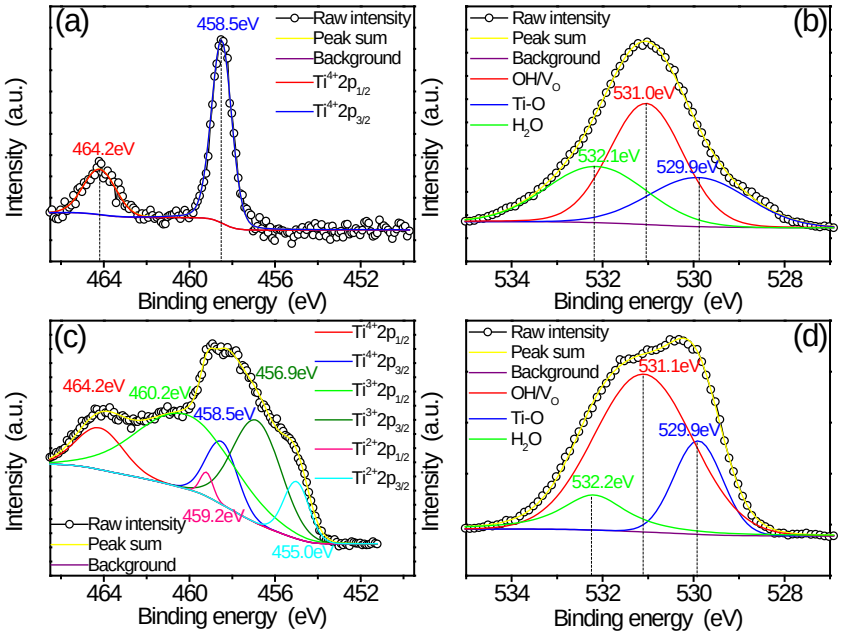


Figure 4 XPS data (open circles) and corresponding fitting results (solid lines) of Ti 2p and O 1s electrons for $TiO_2$ ceramic annealed at 1150 °C in Ar (with 0.1% $H_2$) for 5 h. Before annealed, $TiO_2$ ceramics were sintered at 1400 °C in air for 5 h. (a) and (b) are the surface XPS data of Ti 2p and O 1s , respectively. (c) and (d) are XPS data below the surface of Ti 2p and O 1s , respectively, which were measured after the Ar ion etching process was executed for 2 min by the power of 1kW (Etching rate was about 15 nm/min).

In order to check the valance state of Ti and O elements in the annealed $TiO_2$ ceramic, we measured the XPS data of both the surface and the inner by the Ar ion etching process. Figure 4 shows XPS data (open circles) and corresponding fitting results (solid lines) of Ti 2p and O 1s electrons for $TiO_2$ ceramic annealed at 1150 °C in Ar (with 0.1% $H_2$) for 5 h. As shown in Fig. 4 (a), the position of the Ti 2p doublet with $2p_{3/2}$ and $2p_{1/2}$ binding energies of 458.5 eV and 464.2 eV, respectively, is clearly present, corresponding to that of pure rutile $TiO_2$[22], in addition, noticeable $Ti^{3+}$ (or $Ti^{2+}$) signals are not obviously detected. It is similar to that in unannealed $TiO_2$ ceramic sintered at 1400 °C, that almost all Ti ions are +4 valances in the surface and no obvious $Ti^{3+}$ or $Ti^{2+}$ can be detected (Supplementary Fig. S9). However, in the inner away from the surface about 30 nm, there is obviously $Ti^{3+}$ and $Ti^{2+}$ ions, which were verified by the presentation of $Ti^{3+}$ (Peaks 460.2 and 456.9 eV) ions and $Ti^{2+}$ (Peaks 459.2 and 455.0 eV) ions, an shown in Fig. 4 (c). It is well known that $Ti^{3+}$ (or $Ti^{2+}$) ions comes from $Ti^{4+}$ ions, which is reduced by getting one electron ( two electrons for $Ti^{2+}$ ions) while one oxygen vacancy may release one or two freedom electrons. However, both in the surface and in the inner, the strong peak of $V_o^{\bullet\bullet}$/OH (Peaks 531.0 eV) was detected as shown in Fig. 4 (b) and (d), respectively. The peak of $V_o^{\bullet\bullet}$/OH is even stronger than that of Ti-O (Peaks 529.9 eV), which indicates a great deal of oxygen vacancies are produced in both the surface and the inner of $TiO_2$ ceramic annealed in $Ar/H_2$ atmosphere. In the inner of $TiO_2$ ceramic, one oxygen vacancy can releases one (or two) electron, which may be captured by $Ti^{4+}$ ion, as a result, $Ti^{3+}$ (even $Ti^{2+}$) ion is presented. However, in the surface of $TiO_2$ ceramic, there are a great amount of $H_2O$ molecules, which can be decomposed into H and OH group by catalysis of $TiO_2$ materials[23]. As we known, OH

group have great oxidizability due to the unstable electron structure with seven electrons, which is usually prior to form the steady electron structure with eight electrons by the covalent bond. The author[24,25] reported that, in the surface of $TiO_2$, one oxygen vacancy can be filled two OH groups by the covalent bond to form $TiO\text{-}(OH)_2$ dimerics. When all of freedom electrons from the oxygen vacancies are restrained by OH groups by the covalent bond, an insulting layer is presented in the surface of annealed $TiO_2$ ceramic. Note that, the thickness of the absolute insulting layer is thinner than 30 nm, which is verified by the XPS analysis after Ar ion etching process is executed for 40 s and 80 s (Supplementary Fig. S10), respectively, by the same power of 1kW.By the way, there is a little freedom electrons in the surface of annealed $TiO_2$ ceramic if the annealing time is not long enough in $Ar/H_2$ atmosphere, such as the $TiO_2$ ceramic annealed for 1h (Supplementary Fig. S11), which leads to a large dielectric loss as shown in Fig.1b (red line).

Figure 5

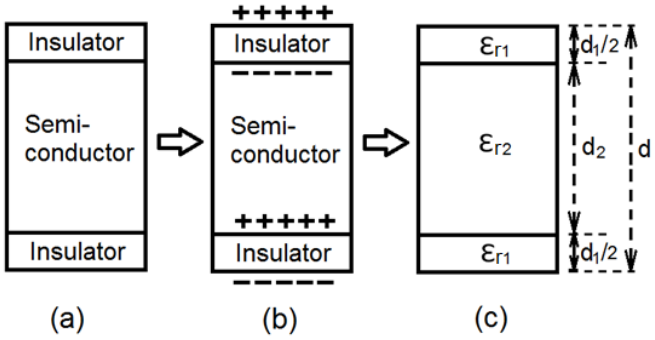


Figure 5 Sketch map of colossal permittivity based on the $TiO_2$ ceramic annealed in $Ar/H_2$ atmosphere. (a) Insulator/semi-conductor/insulator sandwich structure. (b) Sandwich structure applied by an external electrical field. (c) Dielectric constant and thickness of each part in the sandwich structure. $\varepsilon_{r1}$ ($\varepsilon_{r2}$) and $d_1$ ($d_2$) are dielectric constant and thickness of the insulator (semi-conductor), respectively. The total thickness of the sandwich structure is labeled as d, which is the sum of $d_1$ and $d_2$ ($d_2 >> d_1$).

Figure 5 shows the sketch map of colossal permittivity based on the $TiO_2$ ceramic annealed in $Ar/H_2$ atmosphere. This is a simplified Insulator/semi-conductor/insulator sandwich (ISI) model because three points are idealized. The first, in the actual $TiO_2$ ceramic, the so-called 'insulator' layer is not absolutely insulating; the second, the thickness of top insulator is reckoned as that of bottom insulator; the third, the interface between the insulator and the semi-conductor is not clear, where the component should be gradual.[15]When an external electric field was applied on the heavily reduced $TiO_2$ ceramics, oxygen vacancies and freedom electrons were transported to top or bottom surface, respectively, which cannot arrive at the external circuit to form current (resulting in a large dielectric loss) and can be confined beneath the top or bottom surface due to the top or bottom absolute insulator layer. According to the theory of series capacitor, the total capacitor 'C' of the sandwich structure is expressed as:

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_1} = \frac{2}{C_1} + \frac{1}{C_2}$$

Here, $C_1$ and $C_2$ are the capacitor of the insulator and the semi-conductor layer, respectively. Both the insulator and the semi-conductor layer are reckoned as a plate capacitor, and the total

capacitor 'C' of the sandwich structure, the capacitor '$C_1$' of the insulator layer, and the capacitor '$C_2$' of the semi-conductor are:

$$C = \varepsilon_0 \varepsilon_r s/d;\ C_1 = 2\varepsilon_0 \varepsilon_{r1} s/d_1;\ C_2 = \varepsilon_0 \varepsilon_{r2} s/d_2$$

respectively. Here, $\varepsilon_0$ is the absolute dielectric constant and $s$ is the surface area of the sandwich structure; $\varepsilon_{r1}$ ($\varepsilon_{r2}$) and $d_1$ ($d_2$) are dielectric constant and thickness of the insulator (semi-conductor), respectively. The total thickness of the sandwich structure is labeled as $d$, which is the sum of $d_1$ and $d_2$ ($d_2 \gg d_1$, $d \approx d_2$). The dielectric constant $\varepsilon_r$ of the sandwich structure is derived as (Supplementary Formula. S1):

$$\varepsilon_r = \frac{d_2 \varepsilon_{r1} \varepsilon_{r2}}{d_1 \varepsilon_{r2} + d_2 \varepsilon_{r1}} = \frac{\varepsilon_{r2}}{\frac{d_1 \varepsilon_{r2}}{d_2 \varepsilon_{r1}} + 1}$$

Here, this formula can be expressed as three sub-formulas:

$$\varepsilon_r = \begin{cases} \frac{\varepsilon_{r2}}{2}; & \frac{d_1 \varepsilon_{r2}}{d_2 \varepsilon_{r1}} = 1 \\ \varepsilon_{r2}; & \frac{d_1 \varepsilon_{r2}}{d_2 \varepsilon_{r1}} \ll 1 \\ \frac{d_2}{d_1} \varepsilon_{r1}; & \frac{d_1 \varepsilon_{r2}}{d_2 \varepsilon_{r1}} \gg 1 \end{cases}$$

The above three sub-formulas show that $\varepsilon_r$ of the sandwich structure is dependent of $\varepsilon_{r2}$ (dielectric constant of the semi-conductor) and $d_2/d_1$ (the ratio of the thickness between the semi-conductor and the insulator). Only if both $\varepsilon_{r2}$ and $d_2/d_1$ are large enough, a relative great valve of $\varepsilon_r$ can be obtained.

In this ISI sandwich structure, a large ratio of $d_2/d_1$ is easy to be achieved. A large $\varepsilon_{r2}$, i.e. dielectric constant of the semi-conductor layer, seems to be beyond comprehension, after all, the intrinsic dielectric constant of $TiO_2$ materials is about 100. In typical polarization theory, there are three major polarizing mechanisms, including electron polarization, ion polarization, and electric dipole orientation polarization[26-28]. Electron polarization is due to the distortion of the electron cloud around the atomic nucleus. Ion polarization is attributed to the separation between the positive charge center and the negative charge one in a crystal cell. Electric dipole orientation polarization is reckoned as that the random and disorganized electric dipoles are arrayed regularly. These three polarizations have the same characteristic as that the charges of polarization due to the applied external electric field are local, which are restricted within an atom or a crystal cell, and cannot produce a macroscopic current in the external circuit. In a real material, actually, there are some space charges that can be also re-arrayed applied an external field. However, these space charges usually cannot be restrained within the material but participate in the current of the external circuit. In a dielectric material, therefore, space charges are usually diminished as far as possible because they result in a great dielectric loss due to leakage current. However, in a poly-crystalline material, such as CCTO[29,30], space charges can be restricted in the grain boundary or the interface between the CCTO and the electrode, which can lead to a colossal permittivity due to the IBLC [29](the former) or SBLC[30] (the later) mechanism. In our ISI sandwich structure, such as $TiO_2$ ceramic annealed in $Ar/H_2$ atmosphere, there are a great amount of oxygen vacancies with positive charges and freedom electrons with negative charges, which can be separated by the applied external electric field and restricted beneath the surface insulator layers. Therefore, a great deal of space charges can lead to a great polarization ($\varepsilon_{r2}$) without a large dielectric loss.

According to the mechanism of the colossal permittivity In the ISI sandwich structure, $TiO_2$ ceramic is not a unique candidate for colossal permittivity. Only if a semiconductor have both top and bottom insulator layers, it can certainly have a colossal permittivity accompany with a low dielectric loss. In order to verify this assumption, two single-crystalline silicon plates (n type, thickness 0.7 mm) were selected as the semi-conductor layer (Supplementary Fig. S12). The resistivity of one plate is 0.001 Ω·cm, and that of the other is 1 Ω·cm for a comparing object with a relative low carrier concentration. The same $Ga_2O_3$ layers with about 300 nm thickness deposited on the top and bottom surface of silicon plate, respectively, were used as the insulator layers. Note that, here, $Ga_2O_3$ layer is selected because it has a large band gap (4.8eV[31]) and much low carrier concentration due to the intrinsic excitation. It is exciting that a colossal permittivity (~$5\times10^4$) is achieved and the minimum dielectric loss is about 3.4% in silicon plate with a resistivity 0.001 Ω·cm. In another silicon plate with a resistivity 1 Ω·cm, the dielectric constant is about $4\times10^4$, and the minimum dielectric is almost same as that of the silicon plate with a resistivity 0.001 Ω·cm. This experiment data suggest, again, that the colossal permittivity is attributed to the large carrier concentration in the semi-conductor layer, and the low dielectric loss is due to the insulator layer in the ISI sandwich structure. Interestingly, when the silicon plate was replaced by other semi-conductor materials, such as ZnO, ITO etc., the same order of CP with a low dielectric loss can be obtained.

## 3. Conclusions

In conclusion, in this paper, a new model of the ISI sandwich structure for the colossal permittivity based on the $TiO_2$ ceramics annealed in $Ar/H_2$ hybrid atmosphere. There is a great amount of oxygen vacancies in the inner of the annealed $TiO_2$ ceramic; fortunately, there is also an insulator layer due to OH groups in the surface of the annealed $TiO_2$ ceramic. We suggest that the colossal permittivity is attributed to the large carrier concentration of the semi-conductor, and the low dielectric loss is due to the presentation of the insulator layer in the surface. Note that this CP model of the ISI sandwich structure is not limited in annealed $TiO_2$ ceramics. In the typical silicon semi-conductor plate with top and bottom insulator layer $Ga_2O_3$, successfully, both CP and low dielectric loss are achieved at the same time. By the way, if the thickness of semi-conductor layer is as thin as the level of several micron or even thinner, it is much vital for CP with a low dielectric loss that a very thin insulator layer (several or dozens nanometers) must be prepared successfully. It is worthwhile that enormous efforts will be spent in the following works on the new CP systems based on the ISI sandwich structure.

## Acknowledgements

This work was supported by the National Natural Science Foundation of China (Grant No. 51272166), a Project Funded by the Priority Academic Program Development of Jiangsu Higher Education Institutions (PAPD), and J. Hao acknowledges financial support from the grant Research Grants Council of Hong Kong (GRF No. PolyU 153004/14P).

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