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This is the peer reviewed version of the following article: Li, M., Zheng, J., Xu, H., Wang, Z., Wu, Q., Huang, B., Zhou, H., Liu, C., Precise Patterning of Large-Scale TFT Arrays Based on Solution-Processed Oxide Semiconductors: A Comparative Study of Additive and Subtractive Approaches, Adv. Mater. Interfaces 2018, 5, 1700981. , which has been published in final form at https://doi.org/10.1002/admi.201700981. This article may be used for non-commercial purposes in accordance with Wiley Terms and Conditions for Use of Self-Archived Versions. This article may not be enhanced, enriched or otherwise transformed into a derivative work, without express permission from Wiley or by statutory rights under applicable legislation. Copyright notices must not be removed, obscured or modified. The article must be linked to Wiley's version of record on Wiley Online Library and any embedding, framing or otherwise making available the article or pages thereof by third parties from platforms, services and websites other than Wiley Online Library must be prohibited.

Precise patterning of solution-processed InGaZnO/InZnO TFT arrays: A comparative study of additive and subtractive approaches

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Abstract: Wafer-scale thin film transistor (TFT) arrays are demonstrated by using the additive or subtractive patterning method, which employs a hydrophobic polymer to form surface patterns or photolithography with wet-etching processes, respectively. With either of the two methods, 1600 TFT devices are precisely fabricated on a 4 cm×4 cm substrate, using solution-cast indium gallium zinc oxide (IGZO) and indium zinc oxide (IZO) as the active channel layers for their amorphous morphology to allow good uniformity. The devices fabricated by the two methods are systematically compared by using electrical characterizations, photo-electronic spectroscopy, device simulations, and reliability tests. When using the additive method, the IZO (or IGZO) TFT shows a field-effect mobility up to 8.0 $cm^2V^{-1}s^{-1}$ (or 5.2 $cm^2V^{-1}s^{-1}$), whereas when using the subtractive method, the IZO and IGZO TFT show the mobility values up to 24.2 $cm^2V^{-1}s^{-1}$ and 13.7 $cm^2V^{-1}s^{-1}$, respectively. Combining the X-ray photo-electronic spectroscopy (XPS) studies and the device simulations, we suggest that compared with the additive method, the subtractive method with proper post-annealing lead to smaller amount of oxygen vacancies and less acceptor-like sub-gap states, which could be reasons for higher current levels, larger field-effect mobility, and better reliability under negative bias-stressing with illumination. To demonstrate the potential for circuit applications, an NMOS inverter is fabricated by the solution-processed patterning method and show a full swing output transfer characteristic and a voltage gain of 33.8.

KEYWORDS: solution process, additive/subtractive patterning, metal oxide semiconductor, thin film transistor array

1. Introduction

Metal oxide-based thin film transistors (TFTs) have demonstrated considerable potentials for applications in sensors [1, 2], solar cells [3], nonvolatile memory devices [4], and flat panel displays in ultrahigh resolution [5]. Compared with amorphous silicon and organic semiconductors, metal oxide semiconductors (MOS) exhibit the advantages of high electron mobility (more than 10 $cm^2V^{-1}s^{-1}$), high transparency, and large-area uniformity [1, 2, 6-10]. In general, indium (In) and tin (Sn) elements are often employed as the key components in high mobility compounds for their heavy metal cations with (n-1)$d^{10}ns^0$ electronic configurations, which provide fast conduction pathways for the free carriers [6, 9, 11]. For the films that are grown by vacuum-assisted techniques, such as sputtering [12] or pulsed laser material ablation [13], the element stoichiometric ratio needs to be critically controlled by considering the different evaporation rate of target materials [14]. To realize cost-effective, large-scale, and high throughput fabrication, solution-based techniques (usually based on sol-gels) have also attracted significant interests, including spin-coating [9, 10], spray pyrolysis [11], blade coating [8], etc. Despite large success in printed oxide TFTS, there is relatively less research on patterning solution-process oxide thin-film transistor arrays.

For patterning functional films, there have been two main strategies: the additive and subtractive approaches. The additive approach is usually to chemically pattern the surface into different areas with distinct surface free energies, by using self-assembly monolayers (SAMs) or polymers with low surface tensions. Consequently, the solution cast on the surface naturally de-wet from the lyophobic areas and concentrate onto the lyophilic areas, followed by drying to form isolate solid islands [15, 16]. This method based on self-assembly process has been applied to biological or organic functional materials to obtain selective growth or deposition of DNA, organic crystals, or polymer films [15, 17]. In comparison, the subtractive approach is often to firstly spin-coat or print a uniform film, and then to define the sacrificial layer (e.g. photo-resist) patterns followed by wet etching with solvents or acids [18]. This method has been widely used in fabricating metal electrodes and sometimes for oxide semiconductors. The subtractive method has the advantage in being fully compatible with conventional semiconductor industry, while the additive method may benefit in avoiding corruptions of

films in etching and effectively utilizing materials; both methods can be of high resolution down to several microns [16, 19] And yet there has rarely been research on using these methods to fabricate wafer-scale oxide TFT arrays and the direct and quantitative comparisons of the two types techniques are still lacking.

In this study, we explore the two scalable and cost-effective solution-processed patterning strategies to precisely fabricated high-quality oxide thin film arrays, employing InGaZnO and InZnO as the active channel layers. In the additive approach, patterns were firstly formed by a hydrophobic polymer CYTOP followed by blade coating. With either of the approaches, array of 1600 TFTs were fabricated on a 4 cm × 4 cm substrate with only several microliter precursor solutions and the maximum processing temperature is 350 ℃. The highest field-effect mobility is up to 24.2 $cm^2V^{-1}s^{-1}$ and 13.7 $cm^2V^{-1}s^{-1}$ for IZO and IGZO TFTs, respectively. The different performances in devices made from subtractive and additive methods are attributed to the different sub-gap states, as revealed by the systematic studies in photo-electron spectroscopy and quantitative device simulations. Furthermore, the reliability and uniformity of TFT arrays were examined and an NMOS inverter was fabricated to show the full swing output transfer characteristics, which demonstrate the potentials in solution-processed circuit applications.

2. Patterning TFT arrays

The additive approach is to coat the MOS films on pre-patterned substrates, as shown in **Figure 1a-d**. At first, photoresist (PR) was spin-coated and patterned on Si/SiO_2 substrate by photolithography. Then CYTOP solution (solution: solvent = 1: 2) was spin-coated on the substrate at 5000 rpm for 45 s, followed by annealing at 100 ℃ for 10 min in ambient to form hydrophobic films. The sample was soaked in acetone for 10 min to lift off photoresist and the CYTOP pattern was left as the bank surrounding the channel region. After UV treatment for 3 min, the contact angle θ of the bare Si/SiO_2 substrates and CYTOP pattern for DI water were measured to be 18.6° and 111.2° by contact angle meter, as shown in **figure 1**. Then the 0.1M IGZO or IZO solution was sheared across the CYTOP-patterned substrate by a glass rod, which lead to formation of isolated IGZO or IZO islands. The samples were annealed at 100 ℃ for 5 min in a saturated water vapor atmosphere and 350 ℃ for 60 min in ambient, followed by

deposition of electrodes. Optical images of the TFT arrays fabricated with the additive patterning method are shown in **Figure 1e-g**.

The subtractive approach is to pattern the MOS films by wet etching and recovering process, as shown in **Figure 1i-l**. Firstly, 0.1M IGZO/IZO solution was spin-coated onto clean Si/SiO_2 substrate, followed by 100 ℃ water vapor annealing for 5 min and 350 ℃ annealing for 60 min, sequentially. Then photoresist (PR) was coated and patterned on the IGZO/IZO films to define channel regions by photolithography. After etching in hydrochloric acid solution (38% hydrochloric acid: deionized water=1 ml: 150 ml) and removing the residual PR, the isolated IGZO/IZO patterns were obtained. To recover the semiconductor films from damage by acid, two post-treatments were used before depositing electrodes, including 350 ℃ annealing or UV treatment (PL17-110, $15mW/cm^2$) in ambient. Optical images of the TFT arrays fabricated with the subtractive patterning method are shown in **Figure 1m-o**.

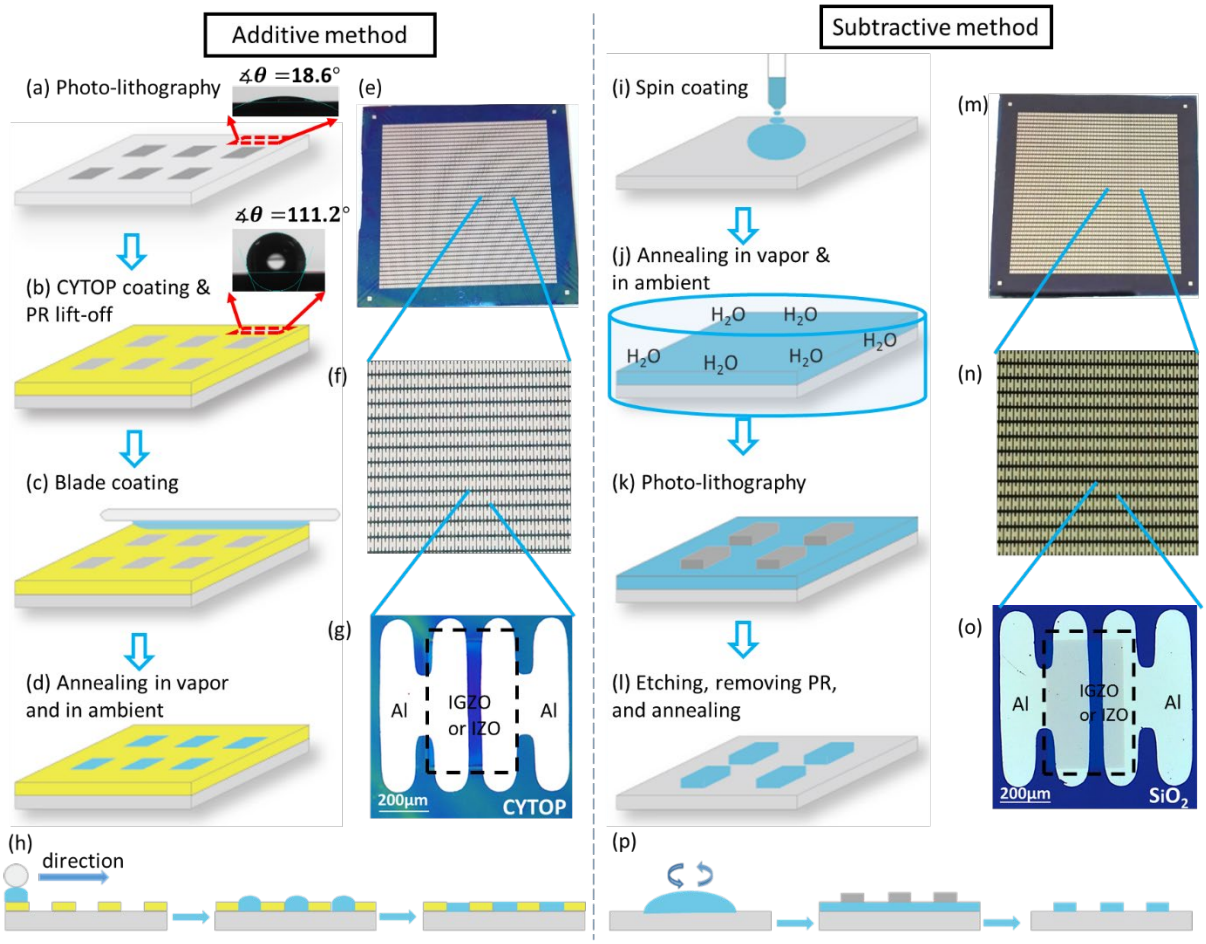

Figure 1 (a)-(d) Schematic process flow of the additive patterning approach: (a) Using photolithography to define photo-resist; (b) Spin-coating CYTOP and lift-off to form CYTOP banks; (c) Using rod to coat oxide solutions; (d) Annealing the film in water vapor and then in ambient conditions. The inserted figure shows the contact angle θ of cleaned Si/SiO_2 wafer (18.6°) and CYTOP film (111.2°). The optical images of TFTs arrays are shown in (e)-(g). (h) The schematic representation of film formation in additive patterning. (i)-(l) Schematic process flow of the subtractive patterning approach: (i) Spin-coating the oxide semiconductor films; (j) Annealing in water vapor and ambient conditions; (k) Using photolithography to define the channel area; (l) Removing photo-resist and doing post-treatment of the films. The optical images of TFTs arrays are shown in (l)-(n). (p) The schematic representation of film formation in subtractive patterning.

The differences in the film formation during the two approaches mainly are: in the additive method, the IGZO/IZO precursor solution self-assembled into small droplets during the coating due to the differences in surface free energy, and then naturally dried to form isolated domain films (see Fig. 1h). In comparison, in the subtractive method, the precursor solution form uniform thin film first and then etched into discrete patterns (see Fig. 1p). Therefore, in the additive method the patterns of MOS directly formed without destruction, whereas in the subtractive patterning methods the films need recovery from acid-etching by post-treatment. The resulting differences in device performance will be investigated below.

3. Device performance

The electrical properties of typical IZO or IGZO TFTs fabricated with the additive ("Add") or subtractive patterning method ("Sub") are shown in **Figure 2**. In the subtractive method, the as-etched oxide semiconductor exhibits poor performance due to the large amount of impurities or defects (Figure S1) and was recovered by post-treatment such as thermal annealing at 350 ℃ or UV treatment. For the recovery process, thermal annealing treatment is more effective than UV treatment in enhancing current and increasing mobility (data shown in Figure S2) in the current study. It is probably because high-temperature annealing assists denser structural frameworks in the oxide semiconductor films, which eliminated the

impurities and provided fast conduction pathways for free carriers [6, 9, 11]. The extracted parameters of the typical devices are summarized in **Table 1** (the statistics data will be given later). The TFT mobility was extracted from the transfer curve by the equation $\mu = \frac{2L}{WC_i}(\frac{\partial\sqrt{I_d}}{\partial V_g})^2$ in the saturation region when $V_d > V_g - V_{TH}$ or by $\mu = \frac{L}{WC_iV_d}\frac{\partial I_d}{\partial V_g}$ in the liner region when $V_d << V_g - V_{TH}$. Here I_d represents for the drain current, μ represents for the mobility, V_d represents for the drain voltage, V_g represents for the gate voltage, V_{TH} represents for the threshold voltage, W and L is the width and length of the TFTs, respectively, and C_i is the capacitance of the gate dielectric.

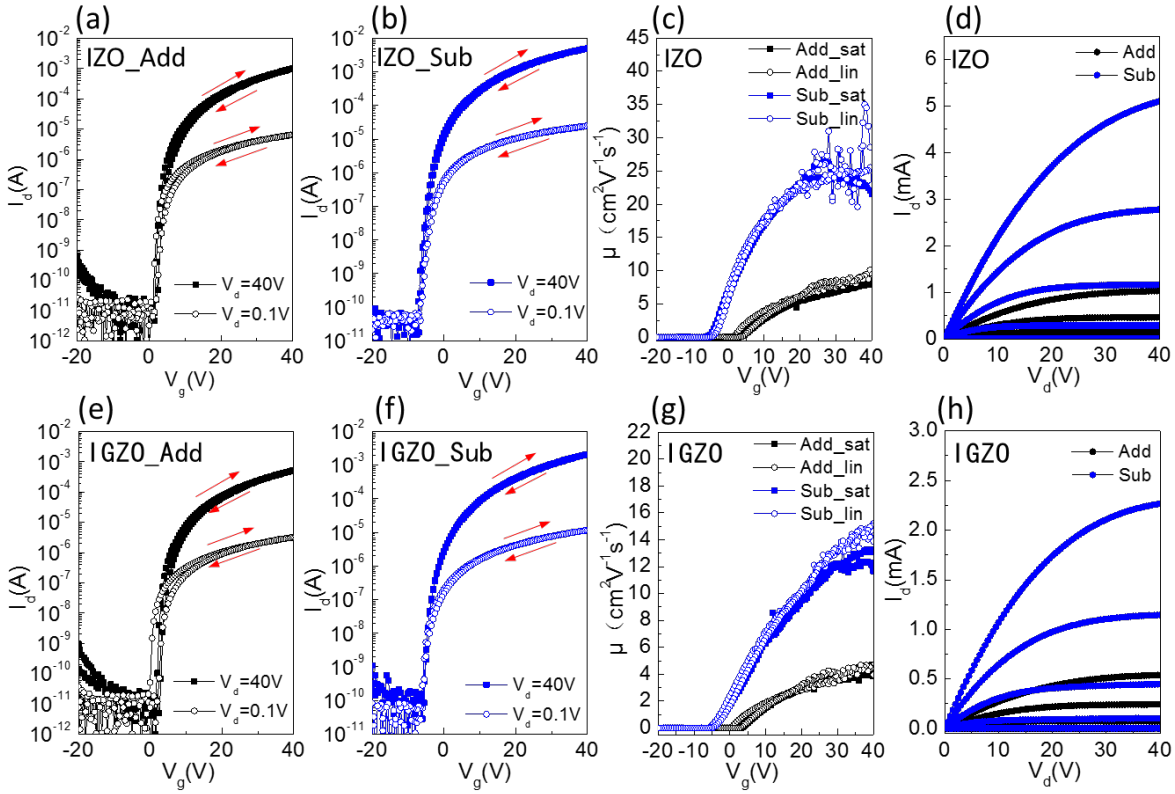

Figure 2 Current-voltage characteristics for IZO (a-d) or IGZO (e-h) TFTs, which were fabricated with additive ("Add") or subtractive patterning approach ("Sub"). For IZO TFTs, transfer curves are shown in (a, b), where the dual scans (forward and backward) were performed in the saturated or linear regime, field-effect mobility as a function of V_G is shown in (c), and output characteristic are shown in (d). The same characteristics of IGZO TFTs are shown in (e-h).

Table 1. Extracted parameters of TFTs fabricated.

Patterning method	Post-treatment	Semiconductor	μ_{sat}	V_{TH}	I_{on}/I_{off}	S.S
			[$cm^2V^{-1}s^{-1}$]	[V]	\	[V/dec]
Additive	\	IZO	8.0	5.7	2.2×10^9	0.4
		IGZO	5.2	6.5	2.2×10^9	0.5
Subtractive	350 ℃/30 min	IZO	24.2	1.3	4.2×10^8	0.7
		IGZO	13.7	2.4	5.3×10^7	0.4
	UV/30 min	IZO	6.3	8.2	9.8×10^7	0.6
		IGZO	0.9	14.7	2.5×10^7	1.3
	\	IZO	2.3	9.2	5.7×10^7	0.6
		IGZO	0.2	11.3	1.2×10^6	2.3

The TFTs fabricated with the subtractive patterning method with post-annealing exhibited the highest mobility. The IZO TFT fabricated with this method shows a saturation mobility of ~24.23 $cm^2V^{-1}s^{-1}$ and the IGZO TFT shows a saturation mobility of ~13.71 $cm^2V^{-1}s^{-1}$, respectively. The mobility of IGZO TFTs is lower than the mobility of IZO TFTs, because gallium with higher oxygen affinity plays a role of an oxygen-retaining agent, which decreases the oxygen vacancy concentration and thus decreases the mobile carrier density [9]. The mobility as a function of gate voltage of IZO or IGZO TFT in the saturation region is shown in **Figure 2c** and **Figure 2g**. Generally, the mobility increased with V_g and reached the maximum value; in IZO TFTs, the mobility slightly decreased after the maximum. This feature is in good accordance with the percolation model, in which the heights of random potential barriers are lowered for carrier transport to form better path when the Fermi-level is raised by the gate-field [ref##5]. The slight decrease in IZO TFTs at the large gate field is probably due to the surface or Columbic scattering at a high carrier concentration [ref##6].

Compared with the subtractive methods, the additive patterning method result in the TFTs fabricated with lower mobility values, i.e. 8.0 $cm^2V^{-1}s^{-1}$ for IZO and 5.2 $cm^2V^{-1}s^{-1}$ for IGZO TFTs, respectively. The oxide semiconductor films were coated by spin coating at high speed to form a large-area, thin film in subtractive patterning method, whereas the films were coated by blade coating at a very low speed to form discrete solution micro-droplets in additive patterning

method. In the next section, the films were subjected to the XPS analysis for detailed investigations.

To examine the uniformity in performance of TFT arrays, the devices were randomly selected in 4 cm×4 cm Si/SiO_2 wafers to test. The devices fabricated in the same batches (on the same wafer) were randomly selected to be measured as shown in **Figures 3a-d**, showing generally good uniformity. The devices fabricated in different wavers (different batches) are statistically analyzed as shown in in **Figures 3e-h**, giving some variations in saturation mobility values. From the figures, we observe that: (1) the TFTs fabricated with the additive or subtractive patterning method shows the same off-state leakage current below $\sim 10^{-10}$ A, because all the semiconducting layers were patterned in isolated domains; (2) for materials, the IGZO TFTs exhibits lower values but smaller variations in mobility, as compared with the IZO TFTs; (3) for processing methods, the subtractive methods generally give higher mobility than the additive methods. The extracted field-effect mobility of the devices fabricated in different batches are as below: the average saturated mobility of 53 IZO TFTs from the subtractive patterning is 9.5 ± 3.09 $cm^2V^{-1}s^{-1}$ while the average value for 80 IZO TFTs from the additive patterning is 6.3 ± 1.48 $cm^2V^{-1}s^{-1}$; the average saturated mobility of 55 IGZO TFTs from the subtractive patterning is 4.9 ± 1.17 $cm^2V^{-1}s^{-1}$ while the average value for 50 IGZO TFTs from the additive patterning is 3.1 ± 0.61 $cm^2V^{-1}s^{-1}$.

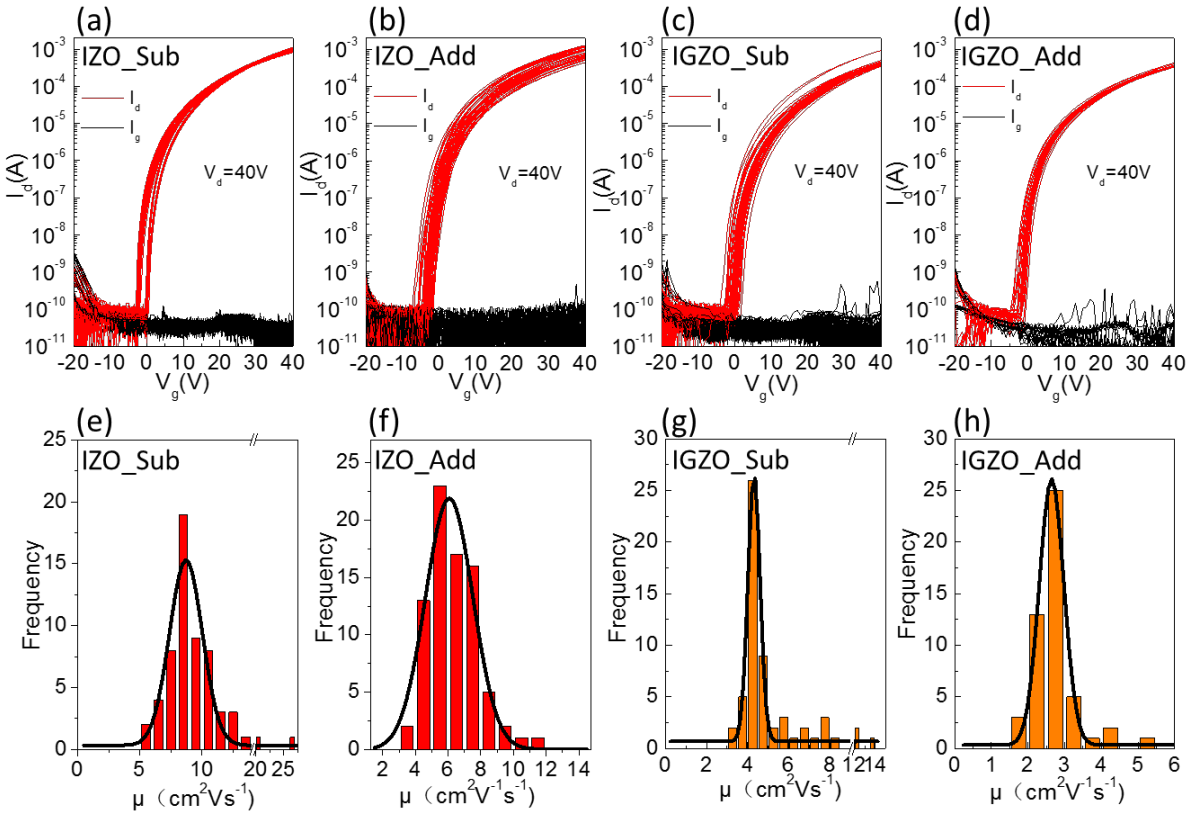

Figure 3 For the devices on the same wafers (the same batch), the transfer characteristics in saturation region (V_d=40V) were measured for randomly selected TFTs: (a) IZO TFTs (40 devices) from the subtractive patterning; (b) IZO TFTs (27 devices) from the additive patterning; (c) IGZO TFTs (40 devices) from the subtractive patterning; (d) IGZO TFTs (40 devices) from the additive patterning. For the devices on the different wafers (different batches), the extracted saturation mobility for randomly selected devices: (e) IZO TFTs (53 devices) from the subtractive patterning; (f) IZO TFTs (80 devices) from the additive patterning; (g) IGZO TFTs (55 devices) from the subtractive patterning; (h) IGZO TFTs (50 devices) from the subtractive patterning.

4. Charge transport properties

The mechanisms for charge transport are analyzed with photo-electron spectroscopy and device simulations. **Figure 4** illustrates the X-ray photoelectron spectroscopy (XPS) data of O 1s peaks for the IZO and IGZO films fabricated with additive and subtractive method. The signals of O 1s peaks are deconvoluted into two components: metal oxide (M-O, ~529.9 eV) and oxygen vacancy (V_O, ~531.5 eV) [9, 20, 21]. In both IZO and IGZO films, the films fabricated

with subtractive patterning method (**Figure 4b,e**) exhibits larger ratio of M-O bonding as compared with those made by the additive patterning method (**Figure 4a,d**). The M-O bonding is believed to provide fast conduction pathways for electrons [6, 9], while the meaning of V_O are complicated in forming various sub-gap states, which are shown in **Figure 5.** On the one hand, some oxygen vacancies have small vacancy sizes (type-I V_O), and so they do not trap electrons but incline to provide free carriers with small gate-field and mainly act as a shallow donor-like states. On the other hand, some oxygen vacancies have larger vacancy sizes to trap electrons (type-II V_O), and so they can trap two electrons until illumination and mainly work as electron traps deep in the band gap [22, 23]. To quantify the sub-gap states coming from microstructures, device simulations are performed to combine with the XPS studies as discussed below.

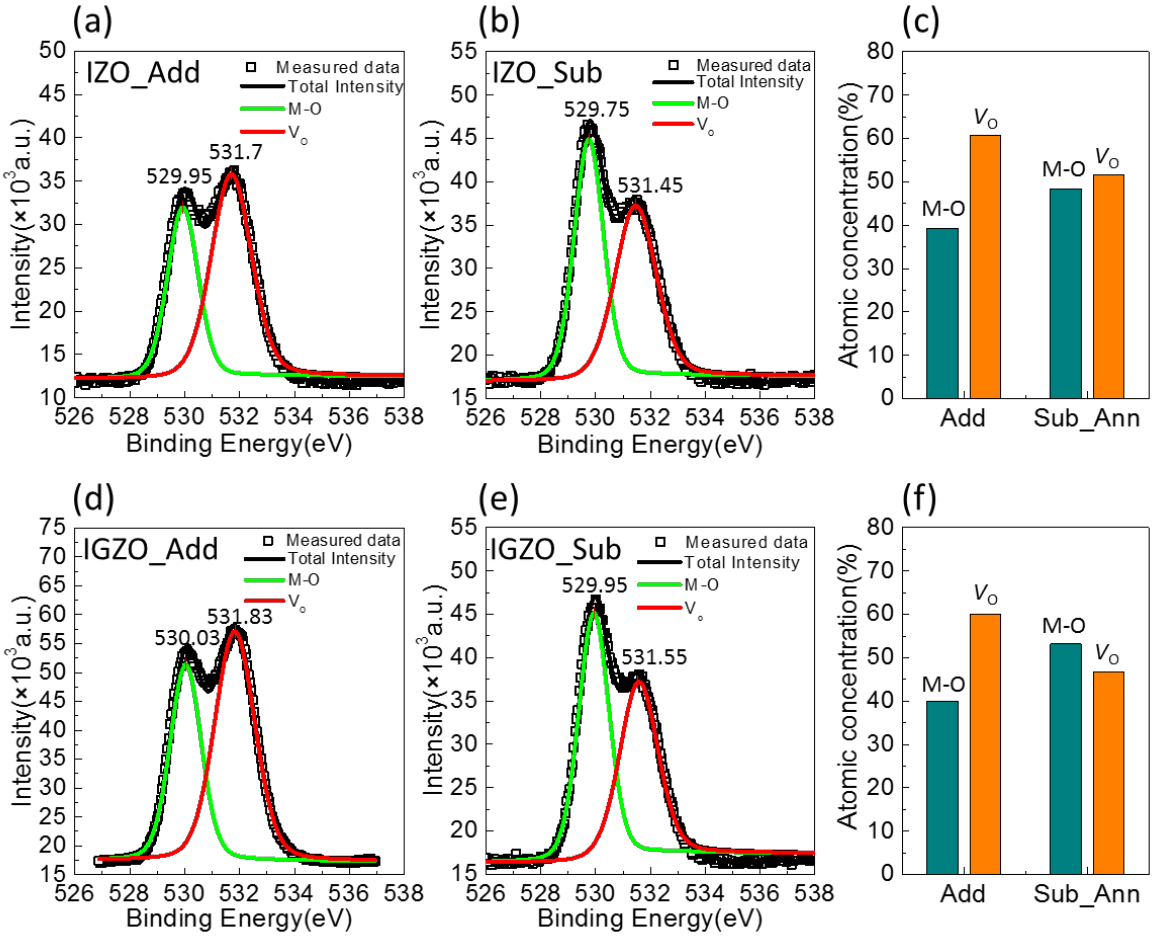

Figure 4. X-ray photoelectron spectroscopy (XPS) data of O 1s peaks: the IZO films fabricated

with additive ("Add") (a) or subtractive ("Sub") (b) patterning method. The extracted atomic concentration of the M-O and Oxygen vacancy is shown in (c). The IGZO films fabricated with additive ("Add") (d) or subtractive ("Sub") (e) patterning method. The extracted atomic concentration of the M-O and Oxygen vacancy is shown in (f).

The sub-gap states in MOS include contributions from acceptor-like states [$g_A(E)$] and donor-like states [$g_D(E)$] [24], as shown in the below equations and **Figure 5e**. The relationship between ion-bonding, DOS, and *I-V* curves were summarized in **Table 2**. The total density of $g_A(E)$ is composed of the density of acceptor-like tail states near conduction band minimum [$g_{TA}(E)$] and the density of acceptor-like deep states [$g_{DA}(E)$]. The former $g_{TA}(E)$ originate from the disorder of metal cation *s*-band and is supposed to be shallow traps [22, 23, 25], while $g_{DA}(E)$ is supposed to be related with the weakly bonded oxygen and to act as deep traps [26]. The total density of $g_D(E)$ is a combination of the density of shallow donor-like states near the conduction band minimum [$g_{DD}(E)$] and the density of donor-like tail states near the valence band maximum [$g_{TD}(E)$]. The shallow donor states $g_{DD}(E)$ originate from the type-I V_O defects and act as donors for free carriers, whereas the deep donor states $g_{TD}(E)$ is related to the type-II V_O defects and lead to instability during the negative bias stressing or photo-illumination [27]. The latter merely affects the static electronic characteristic and so $g_{TD}(E)$ cannot be directly extracted from the measured *I-V* characteristics in this work. In the following, $g_A(E)$ and $g_{DD}(E)$ were extracted by fitting the *I-V* data in saturation region by TCAD simulations.

$$g_D(E) = g_{TD}(E) + g_{DD}(E) = N_{TD} \times \exp\left(\frac{E_V - E}{kT_{TD}}\right) + N_{OV} \times \exp\left[-\left(\frac{E_{OV} - E}{kT_{OV}}\right)^2\right]$$

$$g_A(E) = g_{DA}(E) + g_{TA}(E) = N_{DA} \times \exp\left(\frac{E - E_C}{kT_{DA}}\right) + N_{TA} \times \exp\left(\frac{E - E_C}{kT_{TA}}\right)$$

Table 2 Relationship between microscopic ion-bonding, DOS, and *I-V* curves.

Ion-bonding	**Metal-oxygen bonding (M-O)**		**Oxygen vacancies (V_O)**	
DOS	g_{TA}	g_{DA}	g_{DD}	g_{TD}

Origins	Metal cation s-band (disorder or vacancy)	Weakly bonded oxygen	V_O defects with a small vacancy size (type I)	V_O defects with a large vacancy size (type II)
Defect types	Shallow traps	Deep traps	Shallow donors (provide e- under gate-field)	Deep donors (provide e- under illumination)
Effect on *I-V* curves	Reduce on-current	Reduce on-current; increase V_{th} ; increase S.S	Increase on-current; reduce V_{th}; increase S.S	Reduce reliability in stressing (bias/illumination)

The fitting results are depicted by lines in **Figure 5b** for IZO and **Figure 5f** for IGZO, respectively. The corresponding concentrations of shallow donor-like states [i.e. $g_{DD}(E)$] are shown in **Figure 5c,g**, where are at about 0.1 eV below conduction band minimums (E_C) and mainly provide thermally activated carriers to the conduction levels. Furthermore, the corresponding acceptor-like states [$g_A(E)$] is shown in **Figure 5d,h** and mainly act as trapping sites for the carriers. For both IZO and IGZO TFTs, the devices fabricated with the subtractive patterning method shows a larger number of donor-like states $g_{DD}(E)$ and smaller number of accepter-like states $g_A(E)$. Especially, there are fewer deep acceptor-like states $g_{DA}(E)$ (related with the weakly bonded oxygen) in the device made from the subtractive patterning method, which corresponds well to stronger M-O bonding in the same films found by XPS.

Therefore, by combing the XPS studies and device simulations, we propose that the subtractive methods give generally more M-O bonding that form conduction paths, more donor-like states [$g_{DD}(E)$] that provide free electrons, and less acceptor-like states [$g_A(E)$] that trap free electrons, as compared with the additive methods. Especially, the oxygen vacancies found in the films fabricated by the subtractive methods are supposed to be mainly from the type-I V_O, whereas the films made by additive methods are then attributed to be mainly the deep donor level from the type-II V_O.

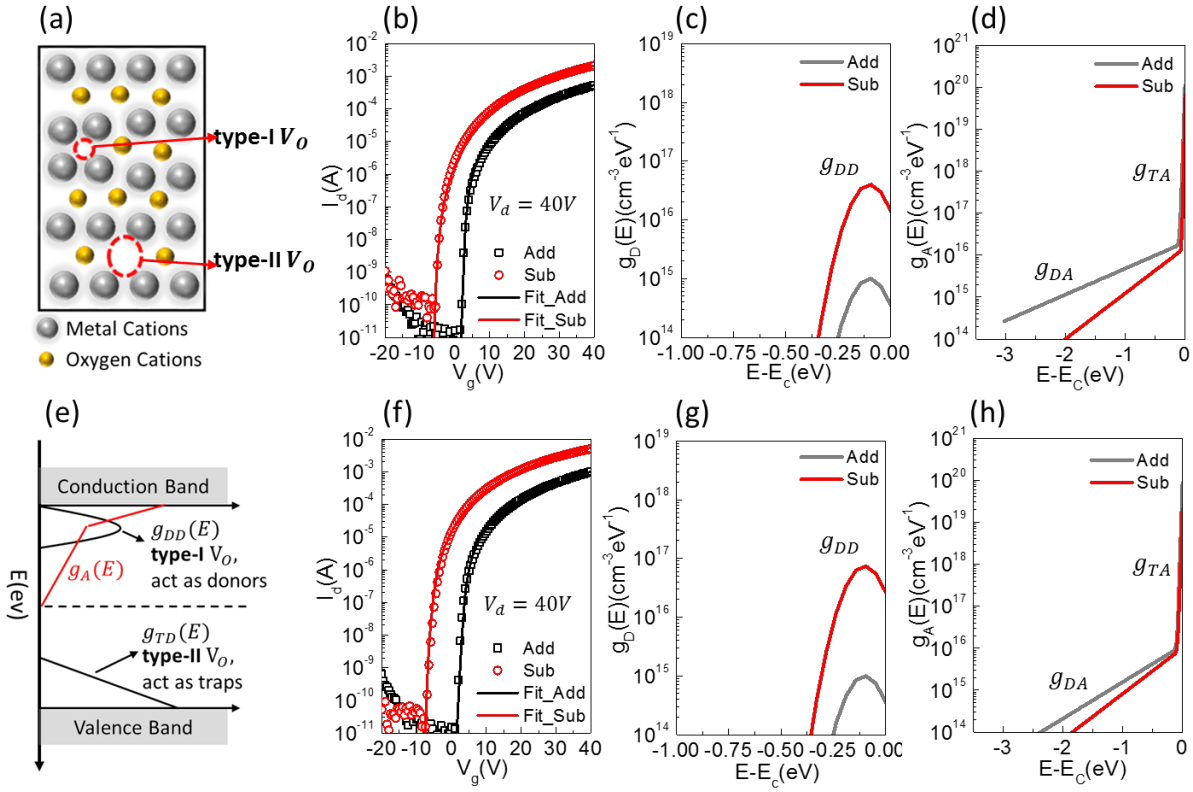

Figure 5 Two states of Oxygen Vacancy(V_O) (a) and their distribution in the band gap(e),refer to[22, 24]. Transfer curves in saturation region (V_d=40V) of the IZO TFT (b) and IGZO TFT (f), where the experimentally measured data are in open dots and the simulated data are in lines. The extracted donor-like states (c,g) and acceptor-like states (d,h) are displayed as a function of energy.

To further investigate the evolutions in M-O and V_O, the subtractive method with different post-treatment is analyzed. The XPS studies for IGZO films fabricated from subtractive methods are presented in **Figure 6** and **Figure S4**, including the films fabricated by without or with post treatment (thermal annealing or UV treatment). The atomic concentration of the M-O and V_O shows that post-treatment increases the ratio of M-O bonding and decreases the V_O bonding. Also, the post-treatment of thermal annealing gives the highest ratio of M-O bonding. This is consistent with the higher values of the mobility of TFTs fabricated by thermal-annealing, as shown in **table 1**, indicating it is effective in film recovery from the solvent etching in this study. It is expected that further optimizations of UV treatment may lead to better device performances.

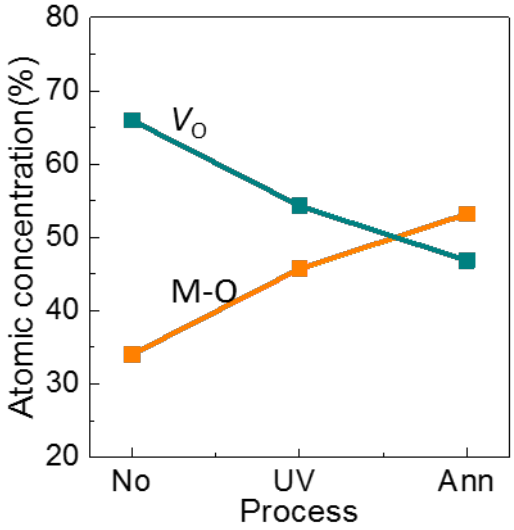

Figure 6. Atomic concentration of the M-O and Oxygen Vacancy extracted from X-ray photoelectron spectroscopy (XPS) data of O 1s peaks for the IGZO films fabricated without post-treatment ("Sub_No") or with post-treatment by thermal annealing ("Sub_Ann") or UV treatment ("Sub_UV").

5. Reliability and inverter demonstration

For applications in display panels, reliability is important for long-time operations and the device performance under negative gate-bias with illumination (NBLS) is investigated here. The resulting transfer curves and V_{TH} shift (V_{TH}-V_{TH0}) of different devices are shown in **Figure 7**, where the current was normalized to the values at the beginning (t = 0 s) for comparison. The NBLS were measured by applying a negative bias (-20V) with a white light on. After NBLS for 3600s, the mobility of all devices slightly increased and the V_{TH} of all device shifted towards negative, as shown in **figure 7c,d**. As mentioned above, the deep donor states near E_V [g_{TD}(E)] is dominant in the reliability test of bias and illumination. According to the shallow donor state-creation model proposed by Kim et. al [27], during negative bias stress, the conduction band edge levels as well as levels of sub-gap states is bent upwards. Because the defect levels become upper than the quasi-Fermi levels, the defect levels become more possible to be un-occupied, i.e. part of the electrons trapped in defect levels will be released to the conduction levels. Besides, the band gap of the IGZO/IZO films is about 3.0 eV, and so the carriers from the deep states may be excited to the conduction levels by the absorption below 400 nm under the

illumination [2, 3]. Consequently, the overall mobile carrier number increases and V_{TH} shifts towards negative.

When comparing the two processing methods, the TFTs fabricated with the additive patterning generally show relatively larger shift of V_{TH}, which is affected by deep donor states. As revealed by the XPS studies and device simulations, the oxygen vacancies found in the films fabricated by the subtractive methods are supposed to be mainly from the type-I V_O, whereas the films made by additive methods are then attributed to be mainly the deep donor level from the type-II V_O. In other words, the type-II V_O is larger in the films fabricated with the additive patterning method and it also explain the larger shift of V_{TH} in the devices. When comparing the two materials IZO and IGZO, it can be seen that the IGZO TFTs exhibits better reliability in NBLS test. This is because the more stable framework ought the stronger M-O bonding of Ga and smaller oxygen vacancy formation energies of In and Zn compared to Ga [9]. Actually, when using UV treatment in the subtractive method, the IGZO TFTs show even better stability with a V_{TH} shift of only 0.66V (see the data in **Figure S3**), which indicate that the shallow traps in the IGZO films may be efficiently passivated by the oxygen ions supplied by the UV treatment.

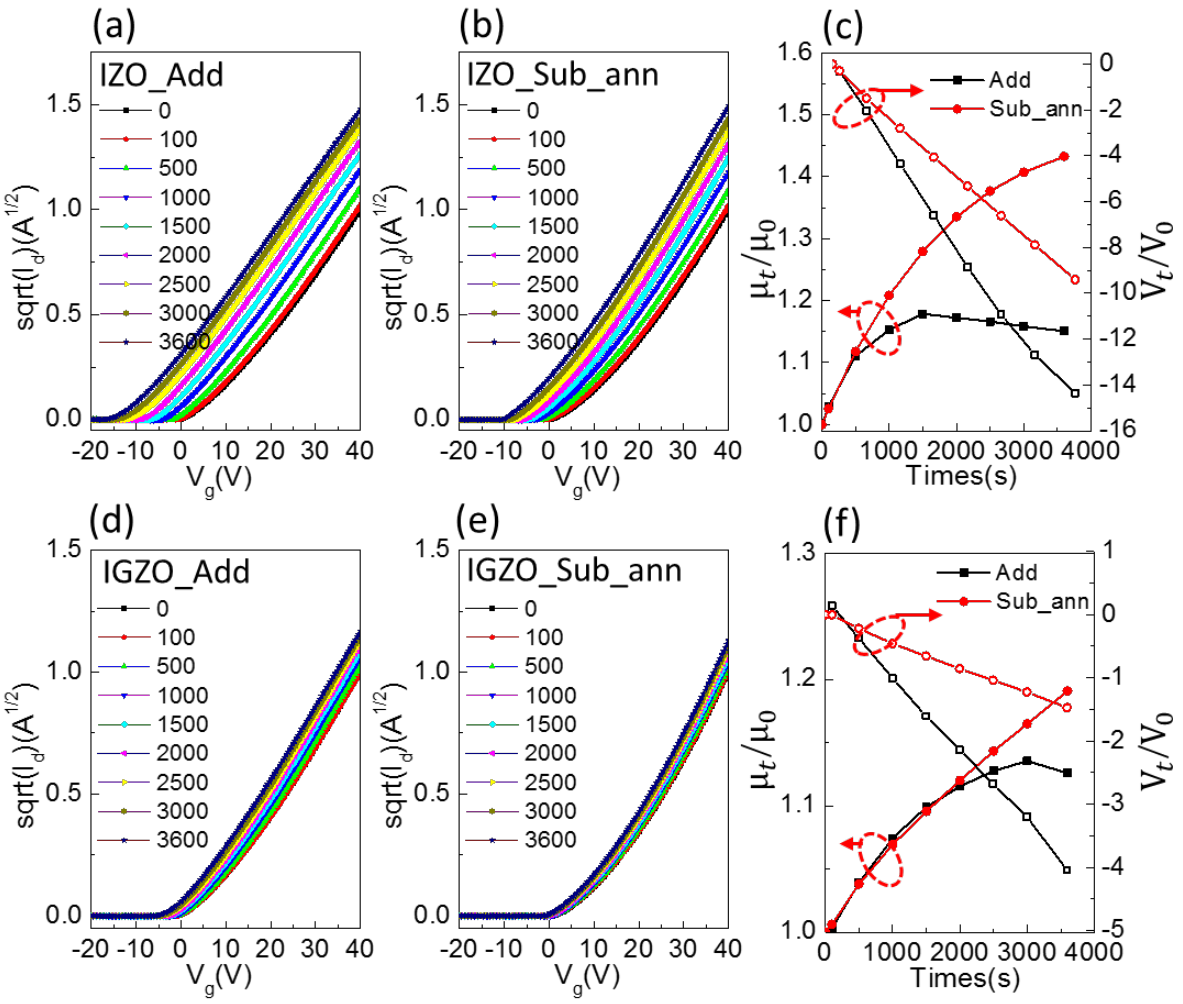

Figure 7 The negative bias-stressing with illumination (NBLS) tests of IGZO or IZO TFTs, of which the current levels are normalized by setting the maximum at 0 s as the unity. The resulting transfer curves of IZO TFTs were fabricated with additive method (a) or with subtractive method (b). The V_{TH} shift (V_{TH}- V_{TH0}) are shown in (c). The resulting transfer curves of IGZO TFTs were fabricated with additive method (d) or with subtractive method (e). The V_{TH} shift (V_{TH}- V_{TH0}) are shown in (f).

To demonstrate the potentials of the solution-patterning methods in circuit fabrication and applications, negative-channel metal oxide semiconductor (NMOS) inverters were fabricated as shown in **Figure 8**. The NMOS inverters were fabricated on the glass substrate with the subtractive patterning method. The cross-sectional structure of the NMOS inverters was shown in **Figure 8a** and the optical images are shown in **Figure 8c**, which is consisted of a driver TFT and a load TFT. In the load TFT, the gate and drain electrodes were intentionally connected. For

the driver TFT, the W/L ratio is 80 /20 μm and for the load TFT the W/L ratio is 160 /25 μm. **Figure 8d** shows the voltage transfer characteristics (VTCs), where the input voltage (V_{IN}) was swept between −10 and 10 V, the supply voltage (V_{DD}) was set at 10V, and the ground voltage (GND) was kept at 0 V. A full-swing rectangle shape VTCs was achieved under this test and the transition voltage (V_M) is 1.19 V. The output voltage (V_{OUT}) equals to V_{DD} until V_{IN} reaches V_M, and it decreases rapidly to 0 V once V_{IN} exceeds V_M. The gain values for NMOS inverters were calculated from the negative slope ($-\mathrm{d}V_{OUT}/\mathrm{d}V_{IN}$) in the VTCs, as shown in **Figure 8e**. The maximum value of gain is 33.83, which is comparable to some NMOS inverters fabricated by sputtering [28].

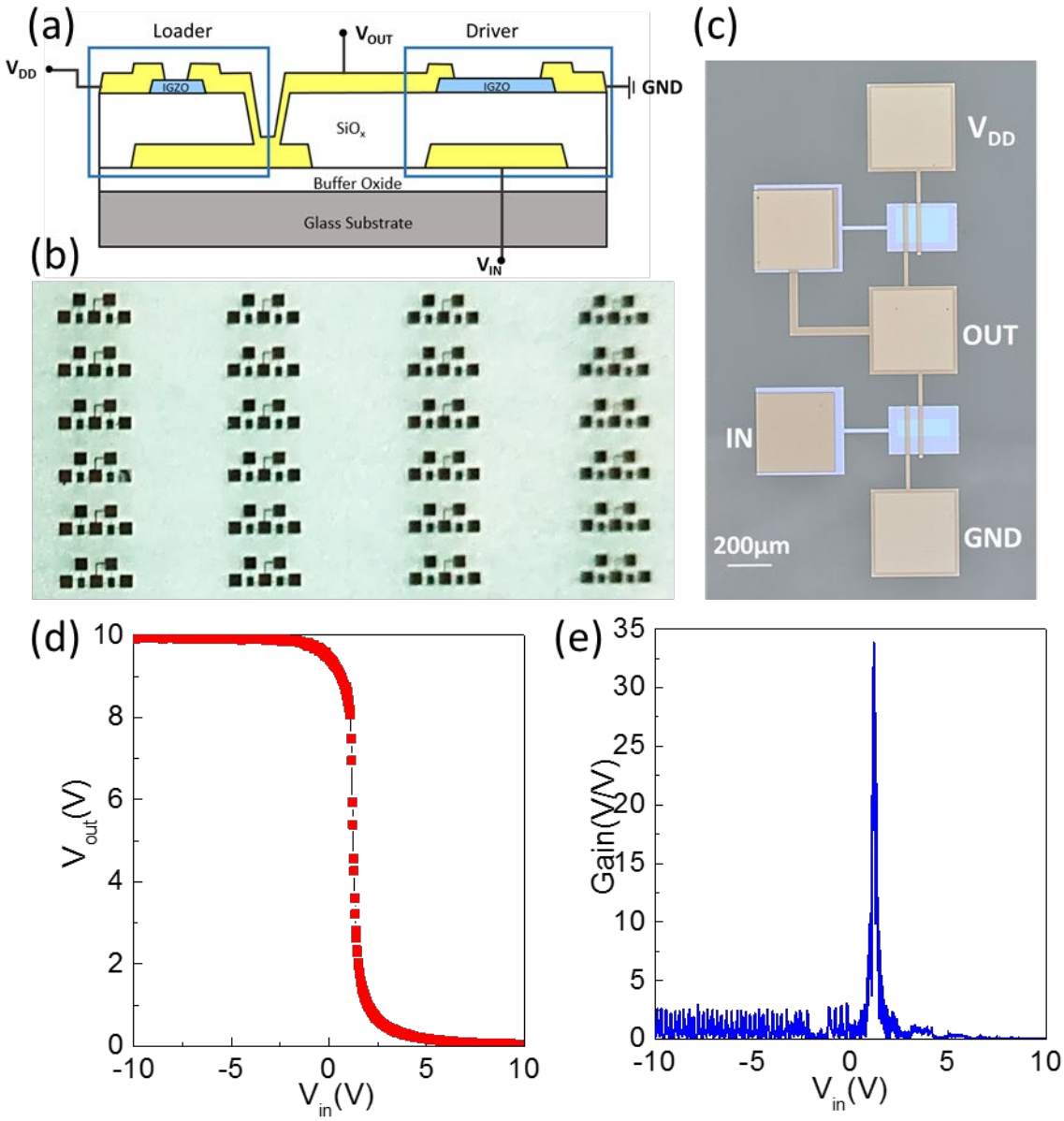

Figure 8 (a) Schematic representation of cross-sectional structure of the NMOS inverter fabricated by solution process. (b) Optical images of the NMOS inverter arrays and a zoom-in view in (c). (d) Voltage transfer characteristics (VTCs) of the NMOS inverter. (e) Gain values of the inverter.

6. Conclusions

Wafer-scale TFTs arrays of InZnO or InGaZnO semiconductor were fabricated by solution processes including the additive patterning and subtractive patterning strategy. The chemical bonding in the film and the current-voltage characteristics in devices were systematically compared. Especially, for the subtractive method, post-treatment by thermal annealing or UV

treatments were employed after etching to repair the damage of the oxide semiconductor films. The device fabricated by subtractive-patterning exhibits the field-effect mobility reaching 24.2 $cm^2V^{-1}s^{-1}$ for IZO TFTs and 13.7 $cm^2V^{-1}s^{-1}$ for IGZO TFTs, whereas the device fabricated by additive-patterning shows the mobility of 8.0 $cm^2V^{-1}s^{-1}$ for IZO and 5.2 $cm^2V^{-1}s^{-1}$ for IGZO TFTs. By combining the XPS studies of the films and numerical simulation of the devices, the better performance in the subtractive-patterning is attributed to the denser structural framework of the M-O bonding and the less oxygen vacancies that act as acceptor-like states. The patterning method was employed to fabricate NOMS inverter to demonstrate the potentials in realizing solution-processed, transparent circuits with high performance.

7. Experimental

Sol-gel solution preparation. The IZO and IGZO precursor solutions were prepared from indium(III) nitrate hydrate (99.9% trace metals basis), zinc nitrate hydrate (99.999% trace metals basis), gallium(III) nitrate hydrate (crystalline, 99.9% trace metals basis), and 2-methoxyethanol (anhydrous, 99.8%), purchased from Sigma-Aldrich. Then 0.1M In, Ga, or Zn precursor was prepared by dissolving the specific metal nitrate in 2-methoxyethanol, respectively, and stirred for 2 h before use. The IZO precursor was prepared by a mixture of 0.1 M In and Zn precursor solution, and the mole ratio of In:Zn was fixed at 1:1. The IGZO precursor was prepared by a mixture of 0.1 M In, Zn, and Ga precursor solution and the mole ratio of In:Zn:Ga was fixed at 6:3:1. All reagents were used without further purification and the solutions were stirred for 2 h before use.

Film Characterizations. For the samples tested in XPS, the films were prepared with the 0.1M IGZO/IZO precursor solution on n-doped silicon substrates. The obtained metal-oxide semiconductor (MOS) thin films on a bare silicon wafer was characterized by X-ray photoelectron spectroscopy (XPS; Thermo-VG Scientific, ESCALAB 250) using a monochromatic Al Kα(hν=1486.6 eV) source in an ultrahigh-vacuum chamber (2×10^{-10} mbar). The binding energy shift was corrected using C 1s peak. The surface contact angle of different surfaces were measured by Dataphysics, OCA15.

Device fabrication and characterizations. The InGaZnO and InZnO TFT arrays (40×40 devices)

were fabricated on 4 cm × 4 cm Si/SiO_2 wafers. All the transistors were in the bottom-gate, top-contact structure. The substrates were ultrasonically cleaned in acetone, ethanol, and deionized water for 15 min, sequentially, and dried by nitrogen blowing. The pre-cleaned substrates were activated by UV treatment (PL17-110, 15mW/cm^2) for 10 min before use. After patterning the MOS films, source and drain electrodes of 40 nm thick Al were deposited by thermal evaporation *via* shadow mask. The channel width and length are 500 μm and 60 μm, respectively. All the devices(without passivation layer) were electrically characterized by a semiconductor parameter analyzer (Agilent, B1500A) under ambient and dark conditions at room temperature unless stated otherwise. And negative gate-bias with illumination stress stability (NBLS) was carried out by a semiconductor parameter analyzer (Agilent, B1500A) with a white light on.

Acknowledgements

The authors gratefully acknowledge the financial support of the project from Guangdong Provincial Department of Science and Technology (2015B090924001) and the Guangdong Natural Science Funds for Distinguished Young Scholars under Grant 2016A030306046.

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