J. Liu, W. Xu, K. W. Chan, M. Liu, X. Zhang and N. H. L. Chan, "A Three-Phase Single-Stage AC–DC Wireless-Power-Transfer Converter With Power Factor Correction and Bus Voltage Control," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 2, pp. 1782-1800, June 2020 is available at https://doi.org/10.1109/JESTPE.2019.2916258

A Three-Phase Single-Stage AC-DC Wireless-Power-Transfer Converter with Power Factor Correction and Bus Voltage Control

Junwei Liu, Wenzheng Xu, Ka Wing Chan, *Member, IEEE*, Ming Liu, Xian Zhang, and Nelson Hon Lung Chan

***Abstract*—Wireless power transfer technology has been a research and industrial hotspot with applications in many areas, such as wireless electric vehicle charging system which requires high power, high efficiency and high power factor. Usually, the power is drawn from 50/60 Hz single-phase or three-phase AC power source. For a high power application, a three-phase AC source is commonly used. In this paper, a three-phase single-stage wireless-power-transfer resonant converter with power factor correction and bus voltage control is proposed to improve efficiency and power quality of three-phase input, and reduce production cost and complexity for high power wireless-power-transfer system. A T-type topology is applied as the common part to perform both the power-factor-correction and DC-DC wireless-power-transfer functionalities simultaneously. The proposed converter is much more advantageous than conventional three-phase two-stage wireless-power-transfer converter with individual power factor corrector. Besides, three-phase single-stage topologies have better power quality than single-phase single-stage topologies because zero-sequence components can be naturally eliminated.**

***Index Terms*—wireless power transfer, three-phase, single-stage, power factor correction**

I. Introduction

Wireless Power Transfer (WPT) is taking up more and more roles in the industrial community. WPT technology has a variety of applications with power levels ranged from several milliwatts to tens of kilowatts, including charging portable telephone [1], supplying power for biomedical implants [2] – [4], electric vehicle (EVs) battery charging [5], [6], and roadway powering moving EVs [7], [8]. Compared to conventional wired power transmission, WPT technology is much more advantageous: convenient, safe, and reliable. Inductive coupling method [1], [2], [6] – [15], as a traditional WPT technology, has been researched for a long time and is a very efficient way to deliver power wirelessly within a short distance. However, power and efficiency drop severely if transfer distance extends or there is a misalignment between transmitter and receiver. Another efficient WPT technology for mid-range transfer, magnetic resonant coupling approach [16] – [21], proposed and demonstrated by MIT in 2007 [22], attracts much interest from researchers in recent years, due to its high efficiency and relatively longer transfer distance. This approach utilizes resonance characteristic of coupled primary and secondary resonant tanks under a specific frequency to achieve WPT efficiently.

For a three-phase isolated AC-DC converter, if power factor and THD of input current are not considered, usually a three-phase diode-bridge rectifier followed by an isolated DC-DC converter will be used, as shown in Fig. 1. However, a modern three-phase AC-DC switching-mode power supply (SMPS) is required to maintain a good power quality of input source and consists of two power conversion stages: a front-end three-phase AC-DC power-factor-correction (PFC) rectifier as the first stage, and an isolated DC-DC converter as the second stage, as shown in Fig. 2. Usually three-phase six-switch PFC rectifier [23], [24], Vienna rectifier [25], TAIPEI rectifier [26], or other type of three-phase PFC rectifier [27] – [29] is used as the first stage while the second stage can be many kinds of isolated DC-DC converters, including flyback, forward, full-bridge, half-bridge, phase-shift, and LLC resonant converters. The SMPS with such two-stage configuration is called as three-phase two-stage AC-DC topology, each stage of which has their independent active switches and control schemes. Generally, a three-phase two-stage topology needs two control strategies for both stages, which obviously increases the control complexity of the system. What’s more, such two-stage topology cannot achieve its highest efficiency due to more power losses in the two-stage conversion. Moreover, it is not with the lowest cost because two-stage conversion means more components.

In recent years, three-phase single-stage AC-DC topologies [30] – [37] that integrate both AC-DC PFC rectifier and DC-DC conversion into only one power conversion stage have been proposed to overcome the drawbacks mentioned above. Such single-stage topology utilizes common active switches

Manuscript received August 2, 2018; revised February 3, 2019 and April 2, 2019; accepted April 27, 2019. This work was supported by the Department of Electrical Engineering, The Hong Kong Polytechnic University. *(Corresponding author: Xian Zhang)*.
J. Liu, W. Xu, K. W. Chan, M. Liu, X. Zhang, and N. H. L. Chan are with the Department of Electrical Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong (e-mail: liujunwei_hust@hotmail.com; xuwenzheng2012@gmail.com; eekwchan@polyu.edu.hk; leo.m.liu@connect.polyu.hk; eexianzhang@outlook.com; nelson06@gmail.com).
Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

and control scheme to realize PFC and isolated DC-DC conversion functionalities simultaneously, as shown in Fig. 3 (a), and Fig. 3 (b) shows one type of three-phase single-stage AC-DC topology, the single-stage TAIPEI rectifier, proposed in [37], where active switches Q_1 and Q_2 are commonly used for both PFC rectification and isolated DC-DC conversion simultaneously. Because of using common active switches and one control scheme, both characteristics of PFC rectifier and isolated DC-DC converter need to be investigated in depth. Not all the PFC rectifiers and isolated DC-DC converters can be randomly integrated into a single-stage topology. In Fig. 3 (b), since the TAIPEI rectifier requires varying-frequency control scheme, the operation frequency of the full-bridge DC-DC converter is also varying in a wide range.

Most of the state-of-the-art single-stage topologies are focused on transformer-based isolated power conversion while there is few for WPT application. Two three-phase single-stage AC-AC matrix converters were proposed for WPT application [38], [39]. However, they utilized 7 and 8 active switches respectively, and their power qualities are not good enough. Also, a single-phase AC-AC matrix converter was proposed for WPT application [40], but 12 active switches are used. A single-phase single-stage AC-DC WPT converter was proposed in [41], however, since its single-phase topology, its power quality is not as good as that of three-phase single-stage topology and its bus voltage is too high at low load condition. The reason that three-phase topology exhibits much better performance of PFC than the single-phase topology is that the former can naturally eliminate zero-sequence harmonics of input current by using an artificial neutral point of the input filter [32], especially for third-order harmonic. As shown in Fig. 3 (c), there is no path for the zero-sequence components to flow into the three-phase source. Instead, such components circulate through the capacitors of the input filter. Furthermore, single-phase topologies are not as suitable as three-phase topologies when high power WPT system is required.

In this paper, the concept of three-phase single-stage AC-DC topology is newly proposed to apply in WPT system: a three-phase single-stage AC-DC WPT resonant converter with PFC, as shown in Fig. 3 (c), where three-level T-type topology is simultaneously used for PFC rectification and DC-DC WPT conversion. Compared with the single-stage TAIPEI AC-DC converter in Fig. 3 (b) and the two-stage TAIPEI and half-bridge AC-DC converter in Fig. 2 (c), although the counts of active switches are the same, the proposed three-phase single-stage AC-DC WPT resonant converter with PFC is much more advantageous. Firstly, the topologies in Fig. 2 (c) and Fig. 3 (b) make the input EMI filter hard to design and its

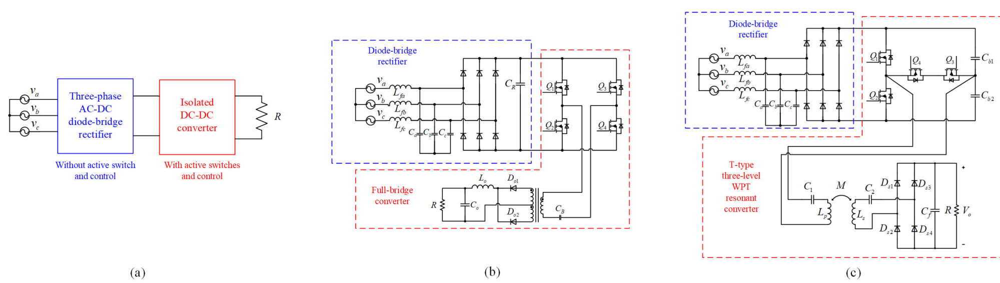


Fig. 1. Three-phase AC-DC converters without PFC. (a) Schematic diagram; (b) The three-phase diode-bridge rectifier is followed by a full-bridge converter; (c) The three-phase diode-bridge rectifier is followed by a T-type three-level WPT resonant converter.

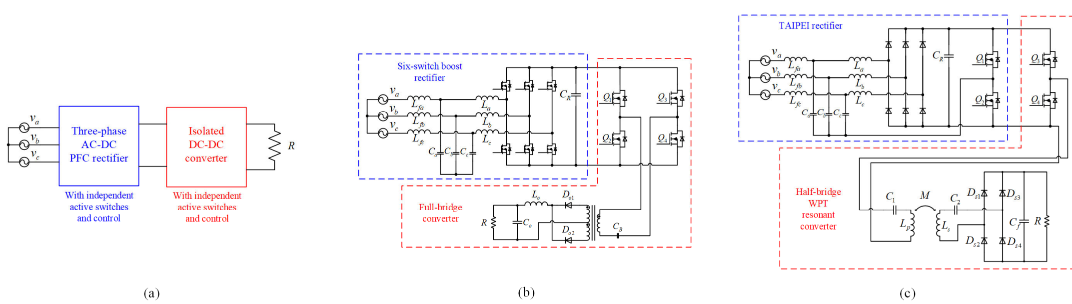


Fig. 2. Three-phase two-stage AC-DC converters with PFC. (a) Schematic diagram; (b) The first stage is a three-phase six-switch boost PFC rectifier [23], [24] and the second stage is a full-bridge converter; (c) The first stage is a TAIPEI rectifier [26] and the second stage is a half-bridge WPT resonant converter.

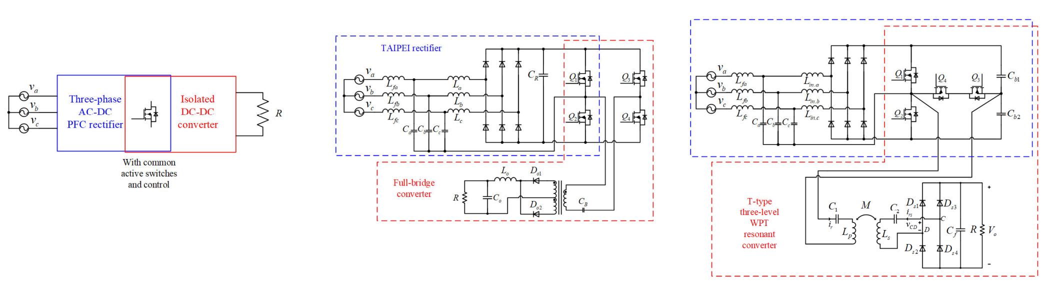


Fig. 3. Three-phase single-stage AC-DC converters with PFC. (a) Schematic diagram; (b) The single-stage TAIPEI rectifier [37]; (c) Proposed three-phase single-stage AC-DC WPT resonant converter with PFC.

volume large because of wide-range varying-frequency operation. Secondly, the second-stage half-bridge converter in Fig. 2 (c) is not so suitable for the WPT system because it generates asymmetric two-level square wave into the WPT resonant tank when the duty cycle is regulated, which brings about the even-order harmonics, increases the total harmonics and causes severer EMI problem. Thirdly, the varying-frequency control scheme of the single-stage TAIPEI topology in Fig. 3 (b) cannot be applied to the WPT system since the efficiency of the WPT system is sensitive to operation frequency and will drop dramatically when operation frequency deviates from its resonant frequency. Fourthly, voltage stresses of the two middle-side switches of the proposed topology are only half of the bus voltage, and therefore the cost of switches can be reduced significantly compared with the two topologies in Fig. 2 (c) and Fig. 3 (b).

Compared with the topology without PFC in Fig. 1 (c), the proposed topology only requires three more input inductors and one line to connect the artificial neutral point with the middle point of switches Q_1 and Q_2. The advantages and contributions of the proposed converter are summarized as follows:

(a) This work is the first time to apply three-phase single-stage AC-DC PFC topology in WPT application. Compared with two-stage topologies for WPT, the proposed converter utilizes a minimum count of power semiconductor devices and exhibits higher efficiency.
(b) The bus voltage is reduced and controlled constantly, which is very important because the bus voltage will not be excessively large and the effect of PFC can be optimized.
(c) Its operating frequency is within a small range of variation (around 6% variation during full load range), so that it can be considered as quasi-constant frequency operation, which is suitable for WPT applications and make input EMI filter design easier and with a smaller volume.
(d) T-type topology is used as the three-level converter, which is capable of simultaneously performing the functionalities of the AC-DC PFC rectification and the DC-DC WPT conversion. Compared with three-level NPC converter, two diodes and one flying capacitor are eliminated, and less isolated driver power supplies are used. Also, it is capable of generating a three-level symmetric square wave for the WPT resonant tank and reducing the higher-order harmonics.

In this paper, topology description and analysis, power factor (PF) and total harmonics distortion (THD) analysis, ZVS conditions, power loss analysis, control method and circuit operation of the proposed converter are presented. Then, the design procedure and example are proposed. Finally, an experimental prototype is implemented to verify the analysis and design.

II. Proposed Topology

A. Topology description

Fig. 3 (c) shows the proposed novel topology. Firstly, a three-wire three-phase voltage source connects with an input filter for filtering the high-frequency components and zero-sequence components of three-phase currents. Followed by the input filter are three input inductors (with the same values), three diode-legs (6 diodes), and a T-type inverter (four switches and two bus capacitors), which are formed together to perform the three-phase PFC functionality. The T-type inverter also connects a resonant tank (resonant capacitors and inductors of primary and secondary side), a secondary-side diode rectifier bridge, an output filtering capacitor, and a load resistor, to perform DC-DC WPT conversion functionality.

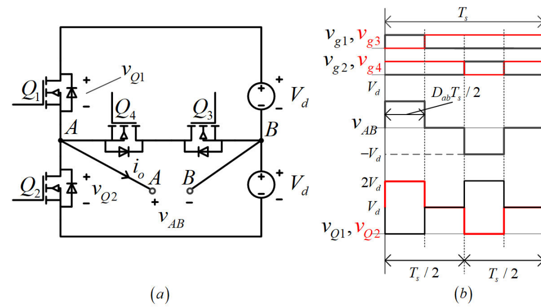


Fig. 4. (a) T-type three-level high frequency inverter; (b) Modulation waveforms of the T-type inverter, where V_d is equivalent DC voltage source. v_{Q1} and v_{Q2} are drain-source voltages of Q_1 and Q_2, respectively.

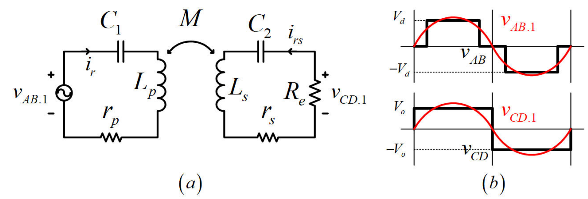


Fig. 5. (a) Equivalent circuit of series-series WPT topology; (b) input voltage and output voltage (v_{AB} and v_{CD}) of the resonant tank and their fundamental components ($v_{AB.1}$ and $v_{CD.1}$).

B. Wireless-power-transfer conversion stage

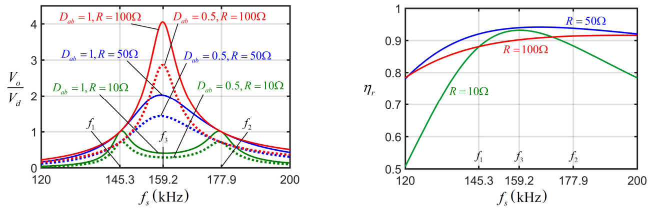
1) T-type three-level high-frequency inverter

Fig. 4 (a) shows the T-type three-level high-frequency inverter, with high-side MOSFET Q_1, low-side MOSFET Q_2, middle-side MOSFETs Q_3 and Q_4. The output voltage of this converter, v_{AB}, can be configured to be a three-level waveform. By the modulation method shown in Fig. 4 (b), the duty ratio of v_{AB}, D_{ab} (ratio of non-zero voltage in a switching period T_s) is adjustable and output current i_o commutates naturally despite its direction [42]. Compared to full bridge inverter, voltage stress of Q_3 and Q_4 reduces to half of the bus voltage while conduction loss when v_{AB} is positive or negative also reduces significantly. Compared to three-level NPC inverter, simpler modulation method, less semiconductor number, less conduction loss, and less isolated driver power supplies are the significant advantages of the T-type inverter [42].

2) Analysis of the DC/DC WPT converter stage

A T-type three-level inverter, a series-series resonant tank, a secondary-side bridge rectifier, a filtering capacitor C_f, and load resistor R are connected to form a DC/DC WPT converter. The resonant tank includes primary inductor L_p and capacitor C_1, secondary inductor L_s and capacitor C_2. M is the mutual inductance of L_p and L_s. Fig. 5 (a) shows the equivalent circuit of the DC/DC WPT converter for theoretical analysis, and r_p is total equivalent series resistance (ESR) of C_1 and L_p, and r_s is that of C_2 and L_s. To analyze the DC characteristics, First Harmonic Approximation (FHA) method [41], [43], assuming the voltage and current of the resonant tanks to be their fundamental components, is applied:

$$v_{AB} \approx v_{AB.1} = (4/\pi)\cdot V_d \sin(D_{ab}\cdot\pi/2)\cdot\sin(\omega_s t+\alpha), \quad (1)$$



(a) (b)

Fig. 6. (a) DC transfer gain vs f_s at different conditions; (b) Efficiency (η_r) vs f_s at different load conditions. The specifications are: L_p=100 μH, L_s=100 μH, M=20 μH, C_1=10 nF, C_2=10 nF, r_p=0.5 Ω, r_s=0.5 Ω.

$$v_{CD} \approx v_{CD.1} = (4/\pi)\cdot V_o \sin(\omega_s t+\beta), \quad (2)$$

$$i_r \approx I_{rp} \sin(\omega_s t+\theta), \quad (3)$$

$$i_{rs} \approx I_{rsp} \sin(\omega_s t+\delta). \quad (4)$$

Here V_d is half of the DC bus voltage, and D_{ab} is duty ratio of v_{AB}, as elaborated in the last section. V_o is the output voltage of the proposed topology. I_{rp} and I_{rsp} are peak values of currents through primary and secondary resonant tanks, respectively. α, β, θ, and δ are phase angles. ω_s is operating frequency in radian. Applying Kirchhoff's Voltage Law to the simplified equivalent circuit as shown in Fig. 5 (a), the following equations are obtained:

$$v_{AB} = \left[1/(j\omega_s C_1) + j\omega_s L_p + r_p\right]\cdot i_r + j\omega_s M\cdot i_{rs}, \quad (5)$$

$$0 = j\omega_s M\cdot i_r + \left[1/(j\omega_s C_2) + j\omega_s L_s + r_s\right]\cdot i_{rs} + R_e\cdot i_{rs}, \quad (6)$$

$$v_{CD} = -i_{rs}\cdot R_e, \quad (7)$$

where R_e is equivalent resistor:

$$R_e = (8/\pi^2)\cdot R. \quad (8)$$

Because r_p and r_s are very small compared to other impedances of the resonant tank, they can be neglected when calculating voltage transfer gain of the DC/DC WPT converter. The voltage transfer gain is calculated by (9) and (10):

$$\left|\frac{v_{AB}}{v_{CD}}\right| = \sqrt{\left(\frac{L_p}{M}-\frac{1}{\omega_s^2 C_1 M}\right)^2 + \left(\frac{\omega_s^2 L_p L_s - \frac{L_s}{C_1} - \frac{L_p}{C_2} + \frac{1}{\omega_s^2 C_1 C_2}}{R_e \omega_s M} - \frac{\omega_s M}{R_e}\right)^2}, \quad (9)$$

$$\frac{V_o}{V_d} = \sin\left(D_{ab}\cdot\frac{\pi}{2}\right)\Big/\left|\frac{v_{AB}}{v_{CD}}\right|. \quad (10)$$

Fig. 6 (a) shows the DC voltage transfer gain of the DC/DC WPT converter vs. operation frequency f_s at different conditions. Usually, the series-series resonant tank is designed assuming $L_s=L_p*k^2$ and $C_2=C_1/k^2$, where k is the resonant inductance ratio. There are three resonant frequencies of the series-series resonant tank:

$$f_1 = 1\Big/\left(2\pi\sqrt{(L_p+M/k)C_1}\right) = 1\Big/\left(2\pi\sqrt{(L_s+M\cdot k)C_2}\right), \quad (11)$$

$$f_2 = 1\Big/\left(2\pi\sqrt{(L_p-M/k)C_1}\right) = 1\Big/\left(2\pi\sqrt{(L_s-M\cdot k)C_2}\right), \quad (12)$$

$$f_3 = 1\Big/\left(2\pi\sqrt{L_p C_1}\right) = 1\Big/\left(2\pi\sqrt{L_s C_2}\right). \quad (13)$$

The efficiency of the resonant tank, η_r, can be obtained as (14), its maximum point occurs at $\omega_s=\omega_{\max}$. $\omega_{\max}$ can be calculated from (15). Fig. 6 (b) shows η_r vs. f_s at different load conditions.

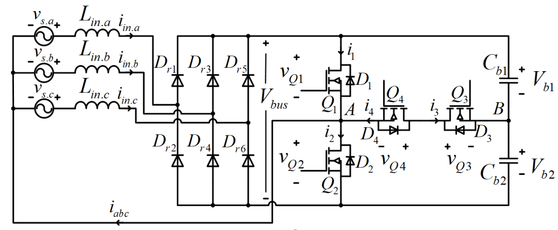


Fig. 7. Proposed three-phase PFC converter stage with equivalent three-phase voltage sources $v_{s.a}$, $v_{s.b}$, and $v_{s.c}$.

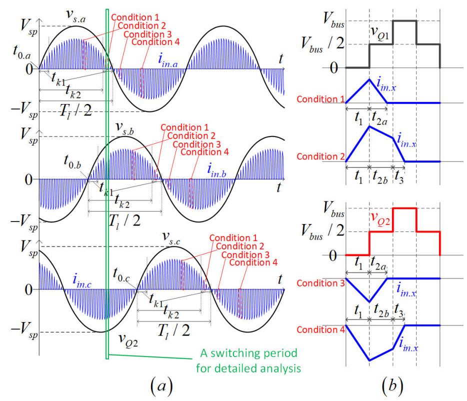


Fig. 8. Waveforms of $v_{s.x}$ and $i_{in.x}$ (x=a, b, and c): (a) low frequency profile; (b) high frequency profile.

$$\eta_r = \frac{R_e}{R_e + r_s + \left(\left(\frac{1-\omega_s^2 L_s C_2}{\omega_s^2 M C_2}\right)^2 + \left(\frac{r_s+R_e}{\omega_s M}\right)^2\right)\cdot r_p}. \quad (14)$$

$$\omega_{\max} = \left(L_s C_2 - (r_s+R_e)^2 C_2^2/2\right)^{-1/2}. \quad (15)$$

C. Three-phase power-factor-correction stage

1) Working principle and analysis

Fig. 7 shows the three-phase PFC converter stage with equivalent three-phase voltage source (voltage after input filter), $v_{s.a}$, $v_{s.b}$, and $v_{s.c}$. The three-phase PFC converter stage consists of three input inductors, six low-frequency diodes, two series-connected bus capacitors, and a T-type converter. $L_{in.a}$, $L_{in.b}$, and $L_{in.c}$ are three phase input inductors with the same inductance L_{in}. $i_{in.a}$, $i_{in.b}$, and $i_{in.c}$ are currents flowing through $L_{in.a}$, $L_{in.b}$, and $L_{in.c}$, respectively. i_{abc} is the sum of $i_{in.a}$, $i_{in.b}$, and $i_{in.c}$. D_{r1}, D_{r2}, D_{r3}, D_{r4}, D_{r5}, and D_{r6} are low-frequency diodes. V_{bus} is bus voltage of two bus capacitors C_{b1} and C_{b2} in series together. V_{b1} and V_{b2} are voltages of C_{b1} and C_{b2}, respectively, and V_{b1}=V_{b2}=$V_{bus}/2$=V_d. Fig. 8 (b) gives the operation waveforms of three-phase currents $i_{in.a}$, $i_{in.b}$, and $i_{in.c}$. Their operation principle is the same. In the following analysis, $v_{s.x}$ refers to $v_{s.a}$, $v_{s.b}$, or $v_{s.c}$ and $i_{in.x}$ refers to $i_{in.a}$, $i_{in.b}$ or $i_{in.c}$.

When $v_{s.x}$ is at its positive cycle, $i_{in.x}$ can behave as condition 1 or 2, where voltage across $L_{in.x}$ is $v_{s.x}$-v_{Q1}; when $v_{s.x}$ is at its negative cycle, $i_{in.x}$ can behave as condition 3 or 4, where voltage across $L_{in.x}$ is $v_{s.x}$+v_{Q2}, as shown in Fig. 8 (b). $i_{in.x}$ as conditions 1, 2, 3, and 4 are all working in discontinuous current mode (DCM), which is capable of reducing higher harmonics and performing PFC functionality. Firstly, $v_{s.x}$ is expressed as:

$$v_{s.x} = v_x = V_{sp}\sin(\omega_l t - \varphi_x), x = a, b, c, \quad (16)$$

where V_{sp} is peak value, ω_l is line frequency in radian, and φ_x is the initial phase (φ_a=0, φ_b=2π/3, φ_c=4π/3). The limitation of $i_{in.x}$ working in DCM is:

$$V_{sp} \le V_{bus}/2. \tag{17}$$

Note V_{sp}/V_{bus} as m, and the limitation is:

$$m \le 0.5. \tag{18}$$

When $i_{in.x}$ working in condition 1, current increases from zero to peak value during t_1 and then decreases from the peak value to zero during t_{2a}. Therefore,

$$\frac{v_{s.x}}{L_{in}} \cdot t_1 + \frac{v_{s.x} - V_{bus}/2}{L_{in}} \cdot t_{2a} = 0. \tag{19}$$

When in condition 2, current increases from zero to peak value during t_1 and then decreases from the peak value to zero during t_{2b} and t_3 with two different slopes. Therefore,

$$\frac{v_{s.x}}{L_{in}} \cdot t_1 + \frac{v_{s.x} - V_{bus}/2}{L_{in}} \cdot t_{2b} + \frac{v_{s.x} - V_{bus}}{L_{in}} \cdot t_3 = 0. \tag{20}$$

When in condition 3, current decreases from zero to negative peak value during t_1 and then increases from the negative peak value to zero during t_{2a}. Therefore,

$$\frac{v_{s.x}}{L_{in}} \cdot t_1 + \frac{v_{s.x} + V_{bus}/2}{L_{in}} \cdot t_{2a} = 0. \tag{21}$$

When in condition 4, current decreases from zero to negative peak value during t_1 and then increases from the negative peak value to zero during t_{2b} and t_3 with two different slopes. Therefore,

$$\frac{v_{s.x}}{L_{in}} \cdot t_1 + \frac{v_{s.x} + V_{bus}/2}{L_{in}} \cdot t_{2b} + \frac{v_{s.x} + V_{bus}}{L_{in}} \cdot t_3 = 0, \tag{22}$$

where t_1 and t_{2b} are determined by D_{ab}:

$$t_1 = D_{ab} T_s/2, \quad t_{2b} = (1 - D_{ab}) T_s/2. \tag{23}$$

The boundary of condition 1 and 2 is $v_{s.x}$=V_{bus}(1-D_{ab})/2 and the boundary of condition 3 and 4 is $v_{s.x}$=-V_{bus}(1-D_{ab})/2. From (16) – (22), the average value of $i_{in.x}$, $i_{avg.x}$ is expressed as:

$$i_{avg.x} = \begin{cases} \dfrac{V_{sp}T_s}{L_{in}} \cdot \dfrac{D_{ab}{}^2 \sin(\omega_l t - \varphi_x)}{8(1 - 2m\sin(\omega_l t - \varphi_x))}, & 0 \le \sin(\omega_l t - \varphi_x) \le \dfrac{(1 - D_{ab})}{2m} \\ \dfrac{V_{sp}T_s}{L_{in}} \cdot \dfrac{-(1/m)(1 - D_{ab})^2 + 2(1 + D_{ab}{}^2)\sin(\omega_l t - \varphi_x)}{32(1 - m\sin(\omega_l t - \varphi_x))}, & \sin(\omega_l t - \varphi_x) > \dfrac{(1 - D_{ab})}{2m} \\ \dfrac{V_{sp}T_s}{L_{in}} \cdot \dfrac{D_{ab}{}^2 \sin(\omega_l t - \varphi_x)}{8(1 + 2m\sin(\omega_l t - \varphi_x))}, & 0 > \sin(\omega_l t - \varphi_x) \ge -\dfrac{(1 - D_{ab})}{2m} \\ \dfrac{V_{sp}T_s}{L_{in}} \cdot \dfrac{(1/m)(1 - D_{ab})^2 + 2(1 + D_{ab}{}^2)\sin(\omega_l t - \varphi_x)}{32(1 + m\sin(\omega_l t - \varphi_x))}, & \sin(\omega_l t - \varphi_x) < -\dfrac{(1 - D_{ab})}{2m} \end{cases}. \tag{24}$$

If m≤(1-D_{ab})/2, $i_{in.x}$ always works in condition 1 or 3. Because of the symmetrical characteristic of $i_{in.x}$ when $v_{s.x}$ in the positive or negative cycle, the input power of a phase can be calculated by average power in half a line period (T_l/2):

$$P_{in.x} = \frac{2}{T_l} \int_{t_{0.x}}^{t_{0.x}+T_l/2} i_{avg1.x} \cdot v_{s.x} dt. \tag{25}$$

If m>(1-D_{ab})/2, $i_{in.x}$ works in all condition 1, 2, 3, and 4. Because of the symmetrical characteristic of $i_{in.x}$ when $v_{s.x}$ in the positive or negative cycle, the input power of a phase can be calculated by average power in half a line period (T_l/2):

$$P_{in.x} = \frac{2}{T_l} \left[\int_{t_{0.x}}^{t_{0.x}+t_{k1}} i_{avg1.x} v_{s.x} dt + \int_{t_{0.x}+t_{k1}}^{t_{0.x}+t_{k2}} i_{avg2x} v_{s.x} dt + \int_{t_{0.x}+t_{k2}}^{t_{0.x}+T_l/2} i_{avg1.x} v_{s.x} dt \right], \tag{26}$$

where $t_{0.x}$=φ_x/ω_l (x=a, b, or c) and

$$t_{k1} = \frac{1}{\omega_l} \arcsin\left(\frac{V_{bus}}{2V_{sp}} (1 - D_{ab}) \right), \tag{27}$$

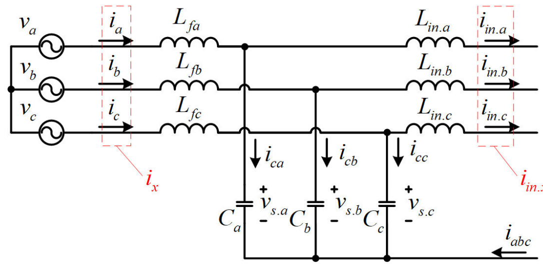


Fig. 9. Input filter and input inductor of the proposed converter

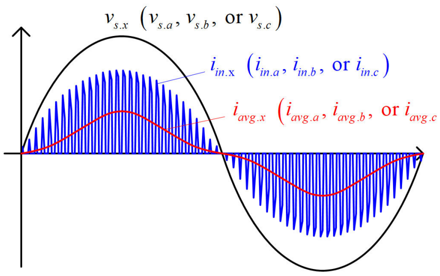
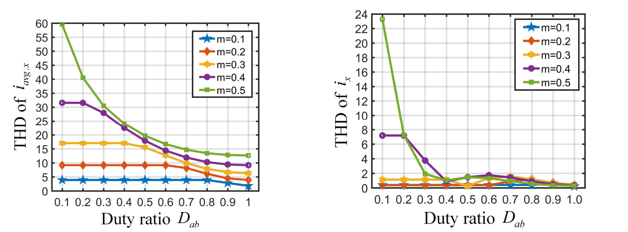


Fig. 10. Waveforms of $v_{s.x}$, $i_{in.x}$, $i_{avg.x}$.



(a) (b)

Fig. 11. THD (%) under different m conditions: (a) THD of $i_{avg.x}$; (b) THD of i_x.

$$t_{k2} = \frac{1}{\omega_l} \left[\pi - \arcsin\left(\frac{V_{bus}}{2V_{sp}} (1 - D_{ab}) \right) \right]. \tag{28}$$

Therefore, the total input power is

$$P_{in} = P_{in.a} + P_{in.b} + P_{in.c}. \tag{29}$$

2) *Analysis of THD and PF*

From Fig. 3 (c) and Fig. 9, before the three-phase PFC converter stage is the input filter. The input filter eliminates high-frequency components of input inductance current $i_{in.x}$ (representing $i_{in.a}$, $i_{in.b}$, or $i_{in.c}$), as well as the zero-sequence components because of using an artificial neutral point of the input filter [32]. Note the average current of input inductance current $i_{in.x}$ in a switching period T_s as $i_{avg.x}$ (representing $i_{avg.a}$, $i_{avg.b}$, or $i_{avg.c}$), called as average input inductance current, as shown in Fig. 10, which can be transformed to Fourier series and then its THD (only related to D_{ab} and m value) is obtained by calculation. Because zero-sequence components (including third harmonic and its odd multiples) are eliminated, THD of line current i_x (representing line current i_a, i_b, or i_c) is much smaller than that of $i_{avg.x}$.

True PF is the result that displacement PF (PF_{dp}) multiplied with distortion PF (PF_{dt}). It can be analyzed that displacement PF is 1 theoretically and then true PF can be calculated by:

$$PF = PF_{dp} \cdot PF_{dt} = PF_{dt} = 1 \Big/ \sqrt{1 + THD_i^2}. \tag{30}$$

Fig. 11 shows the THD of average input inductance current $i_{avg.x}$ and line current i_x at different m conditions. It is obvious that THD of i_x is much lower than that of $i_{avg.x}$.

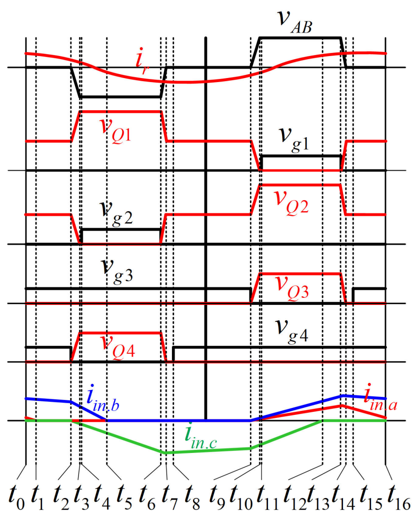


Fig. 12. Operation waveforms during a switching period

D. Single-stage operation and analysis

Input power can be obtained from (24) – (28), and output power P_o can be derived from (8) – (10). If the converter is designed with constant output voltage V_o, then P_o is:

$$P_o = \frac{V_o^2}{R} = \frac{8V_o^2}{\pi^2}\sqrt{\frac{\left(\frac{V_{sp}\cdot\sin\left(D_{ab}\pi/2\right)}{2mV_o}\right)^2-\left(\frac{L_p}{M}-\frac{1}{\omega_s^2 C_1 M}\right)^2}{\left(\frac{\omega_s^2 L_p L_s-\frac{L_s}{C_1}-\frac{L_p}{C_2}+\frac{1}{\omega_s^2 C_1 C_2}}{\omega_s M}-\omega_s M\right)^2}}. \quad (31)$$

For single-stage operation, ideally, P_{in} is equal to P_o at all times. Once P_{in} is not equal to P_o, V_{bus} will change in order to make them equal to realize steady-state condition.

By FHA method, the resonant tank and secondary side can be equivalent to an impedance Z_r, then the detailed operation analysis is illustrated in Fig. 12 and Fig. 13. The waveforms of Fig. 12 are taken from a switching period of Fig. 8 (a). In the following analysis, i_{abc} is defined as the sum of $i_{in.a}$, $i_{in.b}$, and $i_{in.c}$, as shown in Fig. 14.

Stage 1 ($t_0 – t_2$): From t_0 to t_2, Q_3 and Q_4 are ON, whereas Q_1 and Q_2 are OFF. At t_1, $i_{in.a}$ decreased to zero. Current paths of $t_0 – t_1$ and $t_1 – t_2$ are shown in Fig. 13 (a) and (b), respectively.

Stage 2 ($t_2 – t_4$): At t_2, Q_4 is turned OFF. C_{s4} and C_{s1} start to be charged, and C_{s2} starts to be discharged by i_r and i_{abc}. At t_3, C_{s4} and C_{s1} is charged to $V_{bus}/2$ and V_{bus} respectively while C_{s2} is discharged to zero. At this instant, D_2 starts to conduct. At t_4, v_{Q2} has been zero and Q_2 is turned ON. Q_4's turning OFF and Q_2's turning ON realize zero voltage switching (ZVS). Current paths of $t_2 – t_3$ and $t_3 – t_4$ are shown in Fig. 13 (c) and (d), respectively.

Stage 3 ($t_4 – t_6$): From t_4 to t_6, Q_2 and Q_3 are ON, whereas Q_1 and Q_4 are OFF. At t_5, $i_{in.b}$ decreased to zero. Current paths of $t_4 – t_5$ and $t_5 – t_6$ are shown in Fig. 13 (e) and (f), respectively.

Stage 4 ($t_6 – t_8$): At t_6, Q_2 is turned OFF. C_{s4} and C_{s1} start to be discharged, and C_{s2} starts to be charged by i_r and i_{abc}. At t_7, C_{s4} and C_{s1} are discharged to zero and $V_{bus}/2$ respectively while C_{s2} is charged to $V_{bus}/2$. At this instant, D_4 starts to conduct. At t_8, v_{Q4} has been zero and Q_4 is turned ON. Q_2's turning OFF and Q_4's turning ON realize ZVS. Current paths of $t_6 – t_7$ and $t_7 – t_8$ are shown in Fig. 13 (g) and (h), respectively.

Stage 5 ($t_8 – t_9$): From t_8 to t_9, Q_3 and Q_4 are ON, whereas Q_1 and Q_2 are OFF. The current path of this stage is shown in Fig. 13 (i).

Stage 6 ($t_9 – t_{11}$): At t_9, Q_3 is turned OFF. C_{s3} and C_{s2} start to be charged, and C_{s1} starts to be discharged by i_r and i_{abc}. At t_{10}, C_{s3} and C_{s2} are charged to $V_{bus}/2$ and V_{bus} respectively while C_{s1} is discharged to zero. At this instant, D_1 starts to conduct. At t_{11}, v_{Q1} has been zero and Q_1 is turned ON. Q_3's turning OFF and Q_1's turning ON realize ZVS. Current paths of $t_9 – t_{10}$ and $t_{10} – t_{11}$ are shown in Fig. 13 (j) and (k), respectively.

Stage 7 ($t_{11} – t_{13}$): From t_{11} to t_{13}, Q_1 and Q_4 are ON, whereas Q_2 and Q_3 are OFF. At t_{12}, $i_{in.c}$ decreased to zero. Current paths of $t_{11} – t_{12}$ and $t_{12} – t_{13}$ are shown in Fig. 13 (l) and (m), respectively.

Stage 8 (*$t_{13} – t_{15}$*): At t_{13}, Q_1 is turned OFF. C_{s3} and C_{s2} start to be discharged, and C_{s1} starts to be charged by i_r and i_{abc}. At t_{14}, C_{s3} and C_{s2} is discharged to zero and $V_{bus}/2$ respectively while C_{s1} is charged to $V_{bus}/2$. At this instant, D_3 starts to conduct. At t_{15}, v_{Q3} has been zero and Q_3 is turned ON. Q_1's turning OFF and Q_3's turning ON realize ZVS. Current paths of $t_{13} – t_{14}$ and $t_{14} – t_{15}$ are shown in Fig. 13 (n) and (o), respectively.

Stage 9 ($t_{15} – t_{16}$): This stage is the same with stage 1.

E. ZVS conditions

As shown in Fig. 14, the critical point of ZVS operation is node A because i_1, i_2, i_4 (i_3), i_{abc}, and i_r flow and collect here. i_{abc} is defined as the sum of $i_{in.a}$, $i_{in.b}$, and $i_{in.c}$. There are three necessary conditions for a switch to achieve ZVS: dead time, a snubber capacitor, and an appropriate current flowing through the switch. At the instant of turning-OFF, the current flowing through the switch (from Drain to Source) is required to be positive and relatively large enough. In the proposed topology, i_{abc} and i_r determine the directions and magnitudes of i_1, i_2, i_3, and i_4 (Q_1, Q_2, Q_3, and Q_4's drain currents) at the turning-OFF instants of Q_1, Q_2, Q_3, and Q_4. By analysis, operation at stage 4 or 8 can achieve ZVS definitely at any load conditions because the sum of i_{abc} and i_r is always negative or positive respectively (i_{abc} and i_r both collect at or diverge from node A) and large enough. Operation of stage 2 or stage 6 can also achieve ZVS when the sum of i_{abc} and i_r is positive or negative respectively. However, at t_2 or t_9, the sum of i_{abc} and i_r is not always positive or negative respectively. Assume all the snubber capacitors (C_{s1}, C_{s2}, C_{s3}, and C_{s4}) of $Q_1 – Q_4$ are with the same capacitance value C_s, then the ZVS conditions of stage 2 are obtained as:

$$\begin{cases} I_{zvs} > 0 \\ \dfrac{3C_s V_{bus}}{2I_{zvs}} \le T_{dt} \end{cases}, \quad (32)$$

where T_{dt} is the switching dead time between Q_2 and Q_4 (also is the switching dead time between Q_1 and Q_3); I_{zvs} is the ZVS current of stage 2, defined as the minimum sum of i_{abc} and i_r at t_2, which is calculated by (44) of Appendix. The dead time is considered small enough compared with the switching period that during the dead time i_r and i_{abc} are considered to be constant. Because of symmetry the switching characteristics, the ZVS conditions of stage 6 is the same as that of stage 2. It can be analyzed that ZVS operation of stage 2 or stage 6 cannot be achieved when D_{ab} is relatively small (at low load conditions). The critical and specific conditions of ZVS operations can be obtained only when the operation and design

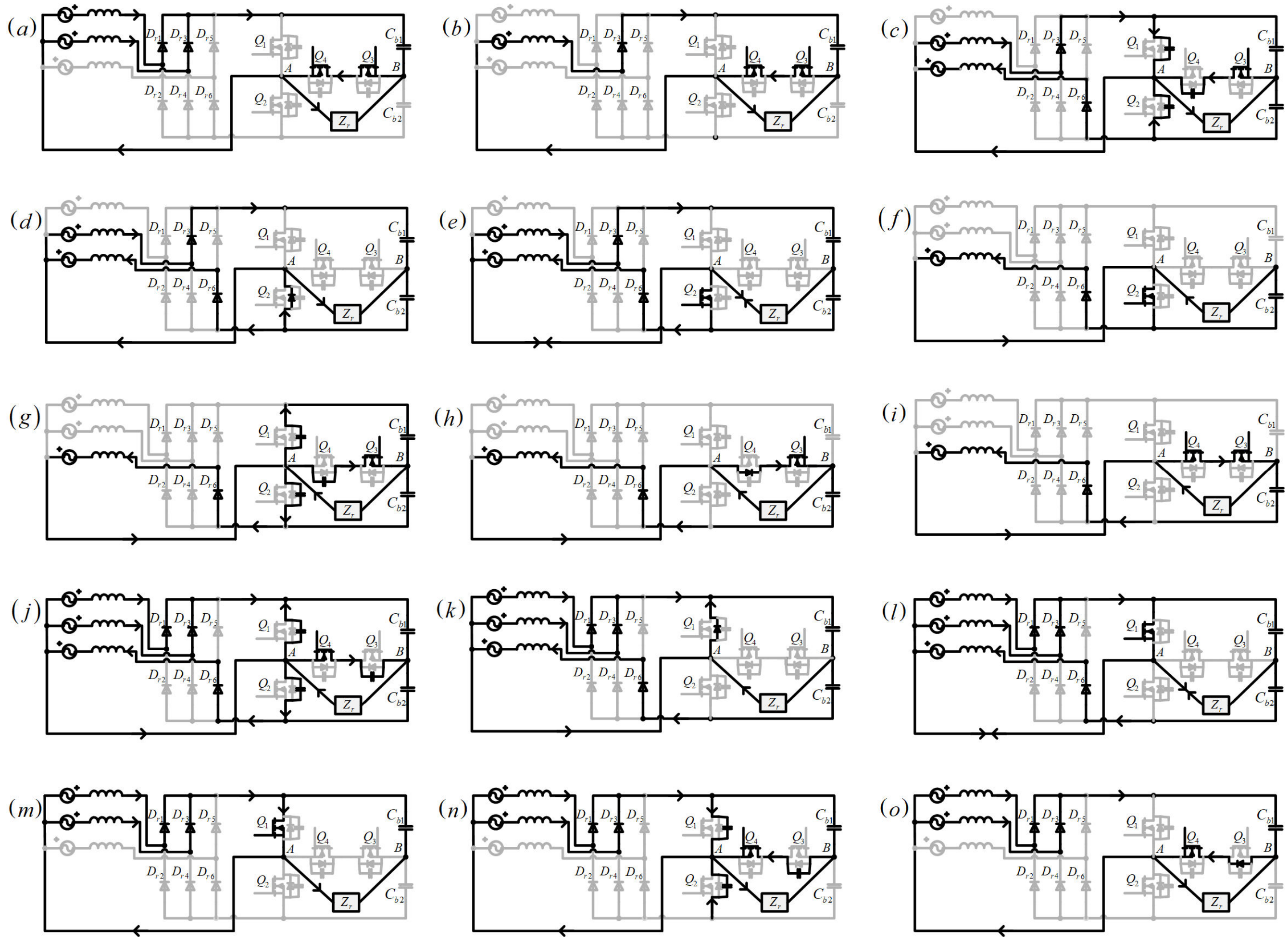


Fig. 13. Operation modes during a switching period: (a) $t_0 - t_1$; (b) $t_1 - t_2$; (c) $t_2 - t_3$; (d) $t_3 - t_4$; (e) $t_4 - t_5$; (f) $t_5 - t_6$; (g) $t_6 - t_7$; (h) $t_7 - t_8$; (i) $t_8 - t_9$; (j) $t_9 - t_{10}$; (k) $t_{10} - t_{11}$; (l) $t_{11} - t_{12}$; (m) $t_{12} - t_{13}$; (n) $t_{13} - t_{14}$; (o) $t_{14} - t_{15}$;

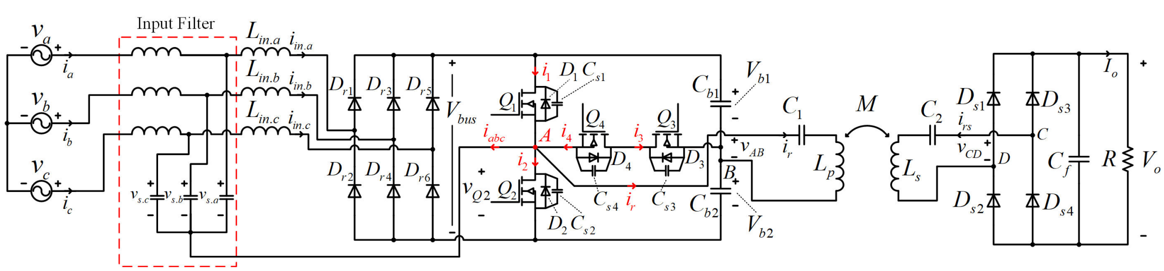


Fig. 14. Proposed converter with marked critical currents

parameters of the proposed converter are confirmed. Generally speaking, when the load condition is larger than 50%, ZVS operations can be achieved. In chapter IV, table II implies whether ZVS operations are achieved or not at different load conditions according to (32). The details can be found in section A of Appendix.

F. Control method

1) Description

The bus voltage (V_{bus}) of the topology is very significant as it decides the maximum voltage ratings of diodes $D_{r1} - D_{r6}$, switching devices $Q_1 - Q_4$, and bus capacitors C_{b1} and C_{b2}. Usually, for single-stage topologies, bus voltage fluctuates with load variations and could be very high at light load condition [32], [41]. Too high bus voltage is unacceptable and therefore many single-stage topologies cannot work at light load condition or standby (zero-load) condition. In this paper, a bus voltage control method is proposed to control V_{bus} stably within a wide load range. In this analysis, the input voltage is assumed to be constant (constant V_{sp}). If allowable maximum bus voltage $V_{bus.\max}$ is confirmed, then minimum m value ($m_{\min}$) will be obtained. From Fig. 11, generally THD of i_x decreases with m value decreases (V_{bus} increases). Therefore, V_{bus} is controlled to be equal to $V_{bus.\max}$ stably to obtain the best THD performance.

D_{ab} and f_s are two control parameters used for regulating output voltage V_o and bus voltage V_{bus}. Fig. 15 shows the curves of P_{in} (dotted lines) and P_o (solid lines) under different D_{ab} and f_s conditions, with constant m value and V_o. At specific D_{ab} and f_s condition, when P_{in} is equal to P_o, V_o and V_{bus} will be stable.

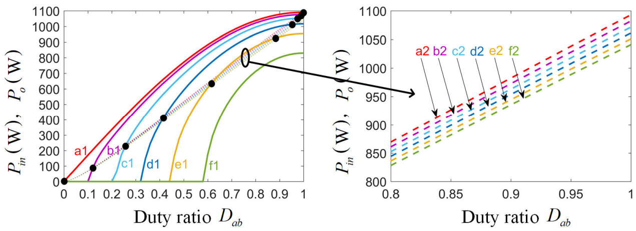


Fig. 15. An example of P_{in} and P_o vs D_{ab} under different operation frequency with parameters: L_{in}=73.5 μH; L_p=L_s=246 μH; C_1=C_2=10.3 nF; M=46 μH; m=0.5; V_{sp}=110√2 V; V_o=250 V. There are six sets of curves with operation frequency: a1 and a2 (ω_s=ω_3); b1 and b2 (ω_s=1.01*ω_3); c1 and c2 (ω_s=1.02*ω_3); d1 and d2 (ω_s=1.03*ω_3); e1 and e2 (ω_s=1.04*ω_3); f1 and f2 (ω_s=1.05*ω_3).

However, when P_{in} is larger than P_o, V_{bus} will increase, and therefore V_o will increase and vice versa. Increasing f_s will decrease both P_{in} and P_o. However, the decrement of P_o is much larger than that of P_{in}, which means that increasing f_s can increase V_{bus}.

D_{ab} is mainly for V_o control, and f_s is mainly for V_{bus} control. When V_o is detected to be higher, D_{ab} will be decreased; simultaneously, when V_{bus} is detected to be higher, f_s will be decreased, and vice versa. Black dots of Fig. 15 are the real operation points at different load conditions. Such a method can realize a wide load range operation and bus voltage control. From Fig. 15, the operation range of f_s within the full load range is very small (around 6% of f_3), so it is easy to design input EMI filter and efficiency of resonant tanks is kept high.

2) Limitation of resonant coils design

There is a limitation of the proposed control method that characteristics of input and output power are required to be similar to those of Fig. 15, which means that the output power should be smaller than the input power at the conditions of f_s larger than f_3 when D_{ab} is equal to 1, resulting in the limitation expressed as:

$$\frac{V_o}{n} \geq \frac{V_{bus}}{\sqrt{2}}. \tag{33}$$

Therefore, when bus voltage V_{bus} and output voltage V_o are confirmed, there will be a restriction for the design of the resonant coils: the square root of the ratio of L_s and L_p are required to fulfill (33). The details can be found in section B of Appendix.

3) Control block diagram

Fig. 16 shows the block diagram of the proposed control method. There are three control loops including an output voltage loop, a bus voltage loop, and a bus voltage balance loop. The output signal of the output voltage loop is duty cycle D_{ab}, while those of bus voltage loop and bus voltage balance loop are frequency f_s and phase difference P_h, respectively. The upper and lower bus voltages and output voltage (V_{b1}, V_{b2}, and V_o) are three signals measured and sampled from the power circuit. The balance of the V_{b1} and V_{b2} (voltages of C_{b1} and C_{b2}) are controlled automatically by regulating the phase difference of driving PWM signals of Q_1 and Q_2. Ideally, when the phase difference is 180 degree, the current flowing through the middle path (Q_3 – Q_4 path) in a switching period is zero, and the bus voltages will be in balance. However, due to the practical difference of the middle switches with different leakage current and parasitic parameters, the current flowing through the middle path (Q_3 – Q_4 path) in a switching period is not zero when the phase difference is 180 degree, resulting in bus voltages imbalance. Therefore, in practical, the phase difference needs to be fine-tuned by the controller automatically all the time to ensure the balance of bus voltages.

TABLE I
PARAMETERS OF THE LABORATORY PROTOTYPE

Components	Details
$L_{in.a}$, $L_{in.b}$, $L_{in.c}$	102.8 μH, 103.9 μH, and 103.3 μH
D_{r1} – D_{r6}	STTH6010
Q_1, Q_2	CREE C2M0080120D
Q_3, Q_4	CREE C3M0065090D
C_{b1}, C_{b2}	1080 μH, 450 V (electrolytic capacitors)
C_{s1}, C_{s2}	1 nF, 1 kV (polypropylene capacitors)
L_p, L_s, M	330.2 μH; 150.9 μH; 48.5 μH
C_1, C_2	10.66 nF; 23.34 nF (10 kV polypropylene capacitors)
D_{s1}, D_{s2}, D_{s3}, D_{s4}	Vishay VS-30EPH06PbF
C_f	220 μF, 450 V (electrolytic capacitor)
L_{if}, C_{if}	(1.97 mH, 1.98 mH, 1.98 mH), (0.92 μF, 0.91 μF, 0.89 μF)
f_s	Min: 85.0 kHz; Max: 90.5 kHz
D_{ab}	0 – 1

III. DESIGN PROCEDURE AND CONSIDERATIONS

A. Design procedure

To verify the design and control of the proposed topology, a 3.3-kW laboratory prototype with constant V_o is designed and implemented. The design procedures are given as follows:

1) Requirements of input and output: Phase voltage v_x of the three-phase voltage source is designed to be 220 V$_{rms}$, 50 Hz. Maximum output power $P_{o.max}$ is 3.3 kW, with constant output voltage V_o to be 330 V and hence maximum output current $I_{o.max}$ is 10 A (minimum load resistance R_{min} being 33 Ω).

2) Requirements of bus voltage: $V_{bus.max}$ is designed to be 640 V and hence V_{bus} is kept to be $V_{bus.max}$ during wide load variation. Then, m value is obtained as 220√2/640 = 0.486.

3) Minimum operation frequency $f_{s.min}$ and mutual inductance M: From Fig. 12, maximum output power condition occurs at the condition with D_{ab} being 1 and f_s being f_3, and $P_{o.max}$ is expressed as:

$$P_{o.\max} = \frac{2V_o V_{sp}}{\pi^3 m f_3 M}. \tag{34}$$

According to SAE J2954 for wireless EV charging, operation frequency is suggested to be 81.39 – 90 kHz. Therefore, $f_{s.\min}$ is selected to be around 85.0 kHz. When f_3 ($f_{s.\min}$) is set as 85.0 kHz, then mutual inductance M is calculated to be 48.6 μH.

4) Design of resonant tank: From (33), the square root of the ratio of L_s and L_p, n, is limited as:

$$n \leq \frac{\sqrt{2}V_o}{V_{bus}} = \frac{\sqrt{2}\times 330}{640} = 0.73. \tag{35}$$

Therefore, the ratio of self-inductance values of primary-side and secondary-side coils is required to be smaller than 0.53. For mid-range wireless power transfer, the coupling coefficient k_{ps}

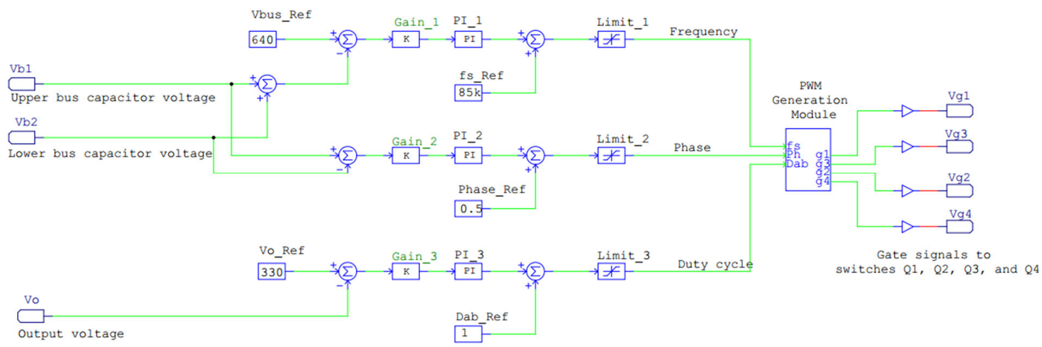


Fig. 16. Block diagram of the proposed control method

of two resonant coils ranges from 0.1 to 0.3 [11], [44]. And considering for EV charging application, air gap distance d_{ag} of two coils is designed to be 150 mm. Therefore, integrating the known parameters of k_{ps}, M, and d_{ag}, the two resonant coils are designed in a spiral shape with the average diameter d to be 400 mm. Their coils numbers are designed to be 25 and 15 respectively. To reduce AC resistance of resonant coils, litz wire with 1000 strands (each strand's diameter is 0.1 mm) are used. The strand's diameter is smaller than two times of skin depth d_{sk}, which is obtained as:

$$d_{sk} = \sqrt{\rho / \left(\pi f_s \mu\right)} \approx 0.23\text{mm}, \tag{36}$$

where ρ and μ are resistivity and permeability of copper litz wire. Therefore, the skin effect can be significantly reduced. Finally, the measured values of the L_p, L_s, and M are 330.2 μH, 150.9 μH, and 48.5 μH, respectively. Values of L_p and L_s fulfill the requirement of (35). According to (13), assuming f_3 to be 85.0 kHz, then C_1 and C_2 are calculated as 10.62 nF and 23.23 nF respectively. Practically, the measured values of C_1 and C_2 are 10.66 nF and 23.34 nF.

5) The Inductance of input inductors L_{in}: Ideally, maximum input power ($P_{in.max}$) is equal to $P_{o.max}$, and also occurs when D_{ab}=1 and f_s=f_3. With known m value (0.486) and V_{sp} (220√2 V), L_{in} can be calculated from (23) – (29), which is 112.0 μH.

6) Maximum operation frequency $f_{s.max}$: By analysis and calculation, at operation frequency f_s equal to 1.065f_3, P_{in} and P_o curves have only one intersection point. Hence, $f_{s.max}$ is confirmed to be 1.065f_3, which is 90.5 kHz.

7) Input filter design: To design the input filter, input resistance of the proposed converter need to be confirmed. Because the input filter configuration of each phase is the same, input resistance of one phase (v_x) is calculated. Here only half-positive cycle of v_x are considered. When $0 \le v_x \le (1\text{-}D_{ab})V_{bus}/2$, input resistance R_i is:

$$R_i = \frac{8L_{in} f_s \left(V_{bus} - 2v_x\right)}{{D_{ab}}^2 V_{bus}}, \tag{37}$$

and when $v_x > (1\text{-}D_{ab})V_{bus}/2$, R_i is:

$$R_i = \frac{32L_{in} f_s v_x \left(V_{bus} - v_x\right)}{2v_x V_{bus}\left(1+{D_{ab}}^2\right) - {V_{bus}}^2\left(1-D_{ab}\right)^2}. \tag{38}$$

It can be analyzed that minimum input resistance $R_{i.\min}$ occurs when D_{ab}=1 (100% load) and v_x=220√2 V. And $R_{i.\min}$ is calculated to be 39 Ω. Note inductance and capacitance of the input filter of each phase as L_{if} and C_{if}, then $\omega_l L_{if} \ll R_{i.\min}$ should

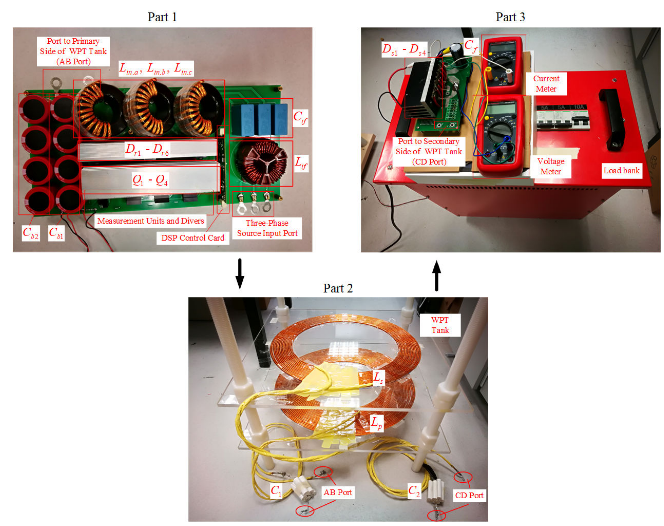


Fig. 17. Setup of the laboratory prototype.

be fulfilled. Therefore, L_{if} is designed to be 1.8 mH first. Because f_s is around 85.0 kHz, the cutoff frequency is designed to be smaller than 8.5 kHz. Therefore, C_{if} is designed to be around 1.0 μF. In practice, L_{if} is measured to be 1.97 mH, 1.98 mH, 1.98 mH (three-phase common mode choke Wurth Elektronik 744837018220) and C_{if} is measured to be 0.92 μF, 0.91 μF, and 0.89 μF (three polypropylene capacitors).

B. Design summary and laboratory prototype

Setup of the laboratory prototype is shown in Fig. 17 and Table I gives the detailed design parameters of the laboratory prototype. Input inductor $L_{in.a}$, $L_{in.b}$, and $L_{in.c}$ are designed to be the same; however, they are a little different due to manufacturing errors and their values are measured to be 102.8 μH, 103.9 μH, and 103.3 μH respectively. Kool Mμ magnetic core in toroid shape (with 125 relative permeability, 62.0 mm outer diameter, 32.6 mm inner diameter, and 25.0 mm height) is used as the core of input inductors and the values of k, α, and β are 1.18, 1.63, and 2.2 respectively. A three-phase auto-transformer is used to output 220 V_{rms} three-phase voltage. CREE discrete SiC MOSFETs are used as the switches $Q_1 - Q_4$ in order to reduce switching loss. Measured ESRs of primary-side and secondary-side coils of WPT tank are 0.41 Ω and 0.29 Ω respectively.

IV. Experimental Results

According to the proposed design procedure, the laboratory

TABLE II
IDEAL OPERATION PARAMETERS AND ZVS CONDITIONS AT DIFFERENT LOAD CONDITIONS

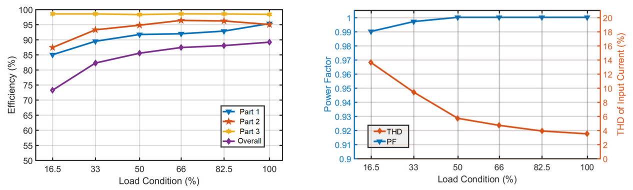
Load conditions	Load resistance R	Duty ratio D_{ab}	Operation frequency f_s	Q_1, Q_2's turning off and Q_3, Q_4's turning on	Q_1, Q_2's turning on and Q_3, Q_4's turning off
100% load (3300 W)	33 Ω	1.00	85.0 kHz	ZVS	ZVS
82.5% load (2722.5 W)	40 Ω	0.88	90.3 kHz	ZVS	ZVS
66% load (2178 W)	50 Ω	0.72	90.2 kHz	ZVS	ZVS
50% load (1650 W)	66 Ω	0.58	89.6 kHz	ZVS	ZVS
33% load (1089 W)	100 Ω	0.41	88.6 kHz	ZVS	ZVS
16.5% load (544.5 W)	200 Ω	0.25	87.5 kHz	ZVS	non-ZVS

TABLE III
COMPARISONS WITH STATE-OF-THE-ART AC-DC OR AC-AC TOPOLOGIES FOR WPT

Topologies	Efficiency (%)		Count of power devices		PF	THD$_i$ (%)	Ratio of bus voltage and input phase voltage	Power level (W)	Soft switching techniques	Three- or single-phase
	AC-AC Part	Overall	AC-AC Part	Overall						
Proposed topology	95.4	89.2	6 diodes + 4 MOSFETs	10 diodes + 4 MOSFETs	1.0	3.5	640/220	3300	ZVS	three-phase
Single-stage AC-AC matrix converter [38]	89.4	not reported	6 diodes + 7 MOSFETs	not reported	0.67	110.8	not reported	267	ZCS	three-phase
Single-stage AC-AC matrix converter [39]	not reported	85	8 MOSFETs	not reported	<0.95	>20.0	not reported	300	no soft switching	three-phase
Single-stage Bidirectional AC-AC matrix converter [40]	92.0	not reported	8 MOSFETs	12 MOSFETs	0.98	19.0	not reported	95	ZCS	single-phase
Single-stage AC-DC converter [41]	93.5	90.1	2 diodes + 4 MOSFETs	6 diodes + 4 MOSFETs	0.99	15.4	745/220	2560	ZVS	single-phase
Two-stage AC-DC converter [45]	not reported	< 85%	7 diodes + 5 MOSFETs	11 diodes + 5 MOSFETs	<0.98	>5.0	180/38	850	not reported	three-phase
Two-stage AC-DC converter [46]	not reported	91.0	12 MOSFETs	4 diodes + 12 MOSFETs	not reported	not reported	750/220	25000	ZVS	three-phase
Two-stage AC-DC wireless charger [47]	95.4	85.2	not reported	not reported	0.93	>20.0	324/221	6600	not reported	single-phase
Two-stage AC-AC converter [48]	91.7	not reported	8 MOSFETs	not reported	0.99	4.5	200/120	100	ZVS	single-phase

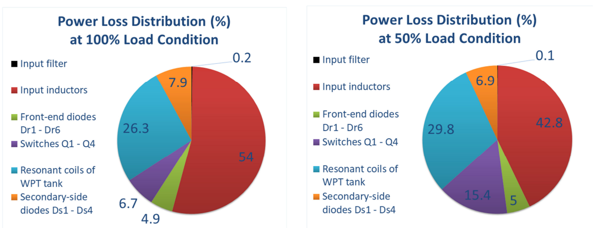
prototype is implemented with rated 3300 W output power. In the experiments, due to the limitation of load bank, operations at 16.5%, 33%, 50%, 66%, 82.5%, and 100% load conditions (544.5 W – 3300 W) are tested to verify the functionalities and advantages of the proposed topology. Table II gives the ideal operation parameters and ZVS conditions at different load conditions. It should be noted that the ideal operating parameters are obtained by simulation results without considering power losses.

Fig. 18 (a) shows the measured overall efficiency and partial efficiencies of different parts (part 1: from three-phase ac line input to input port (AB) of WPT tank; part 2: from input port (AB) to output port (CD) of WPT tank; part 3: from output port (CD) of WPT tank to load, as shown in Fig. 17) at different load conditions. Fig. 18 (b) shows the measured power factor and THD of input current at different load conditions. At full load condition, efficiency, power factor, and THD of input current achieve the best performances (89.2%, 1.0, and 3.5%, respectively). Part 1 of the system can be considered as the AC-AC converter for the WPT tank, which can achieve 95.4% efficiency at full load condition. The efficiency of part 2 (WPT tank) drops when load resistance deviates from the optimum load resistance of the WPT tank. Fig. 19 presents the power loss distributions by theoretical analysis and calculation at 100% and 50% load conditions. The detailed calculation of power losses can be found in section D of Appendix. Power losses of input inductors, of which 99% are the core losses, are the most dominant among total power losses. Such losses can be



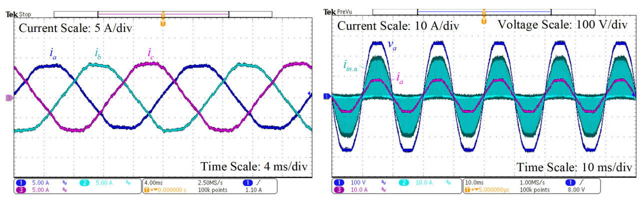
(a) (b)

Fig. 18. Performances at different load conditions: (a) Efficiencies of different parts; (b) Power factor and THD of the three-phase input current.



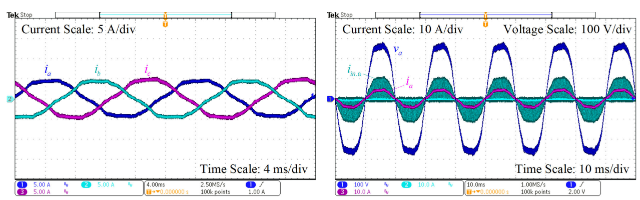
(a) (b)

Fig. 19. Power loss distribution at different load conditions: (a) at 100% load condition; (b) at 50% load condition.



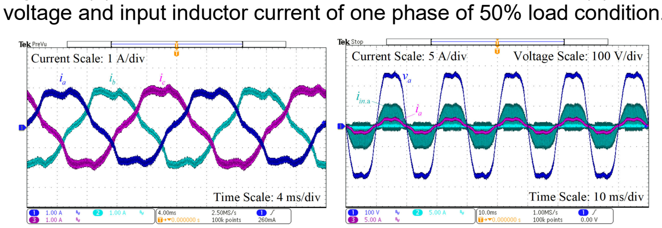
(a) (b)

Fig. 20. (a) Three-phase input current at 100% load condition; (b) Phase voltage and input inductor current of one phase of 100% load condition.



(a) (b)

Fig. 21. (a) Three-phase input current at 50% load condition; (b) Phase voltage and input inductor current of one phase of 50% load condition.

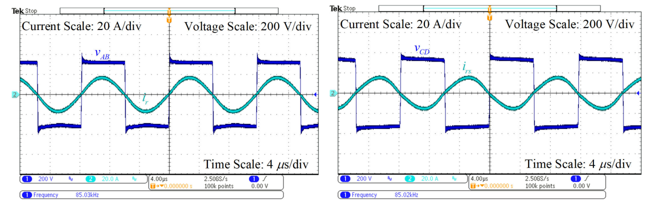


(a) (b)

Fig. 22. (a) Three-phase input current at 16.5% load condition; (b) Phase voltage and input inductor current of one phase of 16.5% load condition.

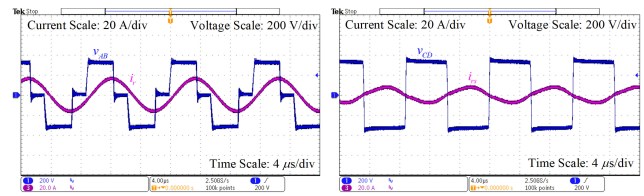
minimized furtherly by choosing a proper magnetic core with relatively low permeability. Power losses of Q_1 – Q_4 are small because ZVS is achieved so that there are only conduction losses. At 50% load condition, the inductive current resulting from the WPT tank is relatively larger, and conductions of Q_3 and Q_4 are remarkable, hence, the ratio of power losses of Q_1 – Q_4 is obviously larger than that at 100% load condition.

Table III presents comparisons of the proposed topology with other state-of-the-art AC-DC or AC-AC topologies for WPT in terms of efficiency, count of power devices, power quality, power level, and soft-switching technique. Compared with the three-phase single-stage AC-AC matrix converters for WPT



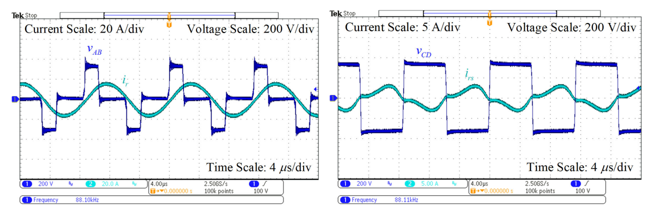
(a) (b)

Fig. 23. Waveforms of resonant tank at 100% load condition: (a) v_{AB} (in blue) and i_r (in cyan); (b) v_{CD} (in blue) and i_{rs} (in cyan).



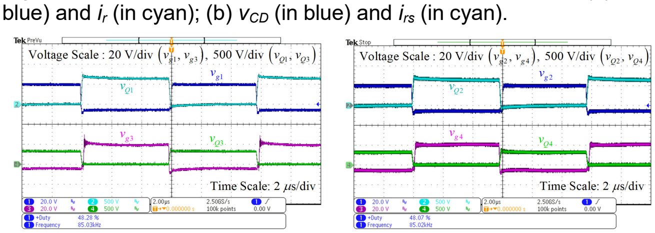
(a) (b)

Fig. 24. Waveforms of resonant tank at 50% load condition: (a) v_{AB} (in blue) and i_r (in purple); (b) v_{CD} (in blue) and i_{rs} (in purple).



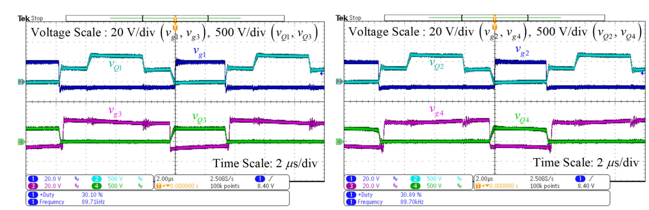
(a) (b)

Fig. 25. Waveforms of resonant tank at 16.5% load condition: (a) v_{AB} (in blue) and i_r (in cyan); (b) v_{CD} (in blue) and i_{rs} (in cyan).



(a) (b)

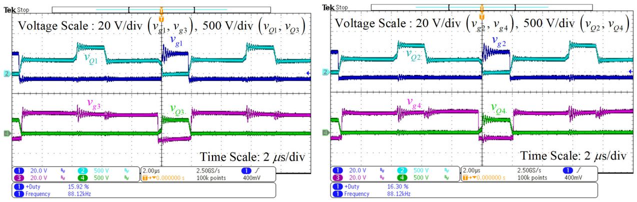
Fig. 26. Switching waveforms at 100% load condition: (a) GS voltages (v_{g1} and v_{g3}) and DS voltages (v_{Q1} and v_{Q3}) of Q_1 and Q_3; (b) GS voltages (v_{g2} and v_{g4}) and DS voltages (v_{Q2} and v_{Q4}) of Q_2 and Q_4.



(a) (b)

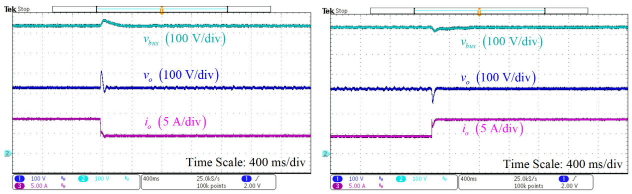
Fig. 27. Switching waveforms at 50% load condition: (a) GS voltages (v_{g1} and v_{g3}) and DS voltages (v_{Q1} and v_{Q3}) of Q_1 and Q_3; (b) GS voltages (v_{g2} and v_{g4}) and DS voltages (v_{Q2} and v_{Q4}) of Q_2 and Q_4.

[38], [39] and three-phase two-stage AC-DC topologies for WPT [45], [46], the proposed topology performs remarkably better efficiency (except for the topology of [46]) and power quality and uses less count of power MOSFETs. Throughout the wide load-varying range, bus voltage is maintained to be stable (640 V) as designed previously, which is lower than that of single-phase single-stage topology [41]. Compared to the single-phase single-stage and two-stage topologies for WPT [40], [41], [47], [48], the power quality of the proposed topology is also much better. In general, the proposed topology exhibits significant and dominant advantages considering the integrated performances of power quality, efficiency, count of



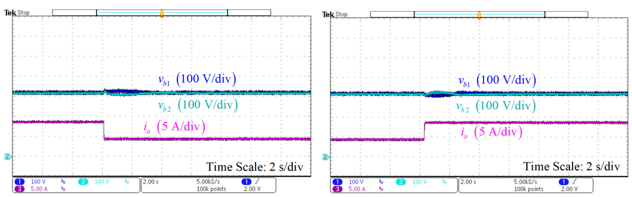
(a) (b)

Fig. 28. Switching waveforms at 16.5% load condition: (a) GS voltages (v_{g1} and v_{g3}) and DS voltages (v_{Q1} and v_{Q3}) of Q_1 and Q_3; (b) GS voltages (v_{g2} and v_{g4}) and DS voltages (v_{Q2} and v_{Q4}) of Q_2 and Q_4.



(a) (b)

Fig. 29. Step responses of V_{bus} and V_o: (a) from 82.5% to 41.25% load condition; (b) from 41.25% to 82.5% load condition.



(a) (b)

Fig. 30. Step responses of V_{b1} and V_{b2}: (a) from 82.5% to 41.25% load condition; (b) from 41.25% to 82.5% load condition.

power devices, and power capability compared with existing topologies for WPT.

Fig. 20 – Fig. 22 show the input current, phase input voltage, and input inductor current at 100%, 50%, and 16.5% load conditions respectively. Fig. 23 – Fig. 25 show the voltages and currents of the WPT tank at 100%, 50%, and 16.5% load conditions respectively. Fig. 26 – Fig. 28 show the switching waveforms of Q_1 – Q_4 at 100%, 50%, and 16.5% load conditions respectively. It is evident that at 100% and 50% load conditions, Q_1 – Q_4 can realize soft-switching at both turn-on and turn-off instants. However, when load condition is lower than 30%, such as 16.5% load condition, soft-switching cannot be totally realized due to insufficient inductive resonant current and therefore the efficiency of part 1 drops remarkably. Fig. 29 and Fig. 30 show the dynamic responses of the proposed converter with the proposed control method. Both bus voltage and output voltage are controlled stable and constant with good dynamic performances and voltages of upper and lower bus capacitors are also controlled in balance stably when the load changes.

V. Conclusions

A three-phase single-stage AC-DC WPT resonant converter with PFC is firstly proposed, studied, and developed in this paper. The proposed topology combines a three-phase rectifier bridge and a T-type three-level inverter together to realize the functionalities of AC-DC power factor correction and DC-DC WPT simultaneously. The proposed three-phase topology can improve efficiency and reduce control complexity compared to three-phase two-stage AC-DC WPT converters. In addition, bus voltage is also maintained to be a relatively low level when the load condition varies. Detailed description and analysis, design procedure, and a laboratory prototype are presented. The experimental results verify the functionalities and performances of the proposed topology.

Appendix

A. Derivation of the ZVS conditions

Here operation of stage 2 is taken to analyze the ZVS conditions. At t_2, $i_{in.c}$ is zero to ensure DCM operation, and hence i_{abc} is equal to the sum of $i_{in.a}$ and $i_{in.b}$, expressed as:

$$i_{in.a}\big|_{t_2}=\begin{cases}\dfrac{v_{s.a}}{L_{in.a}}\cdot\dfrac{D_{ab}T_s}{2}-\dfrac{V_{bus}/2-v_{s.a}}{L_{in.a}}\cdot\dfrac{(1-D_{ab})T_s}{2}, & v_{s.a}\ge\dfrac{V_{bus}}{2}(1-D_{ab})\\ 0, & v_{s.a}<\dfrac{V_{bus}}{2}(1-D_{ab})\end{cases}, \tag{39}$$

$$i_{in.b}\big|_{t_2}=\begin{cases}\dfrac{v_{s.b}}{L_{in.b}}\cdot\dfrac{D_{ab}T_s}{2}-\dfrac{V_{bus}/2-v_{s.b}}{L_{in.b}}\cdot\dfrac{(1-D_{ab})T_s}{2}, & v_{s.b}\ge\dfrac{V_{bus}}{2}(1-D_{ab})\\ 0, & v_{s.b}<\dfrac{V_{bus}}{2}(1-D_{ab})\end{cases}. \tag{40}$$

By analysis, minimum i_{abc} at t_2 is expressed as (input inductors $L_{in.a}$, $L_{in.b}$, and $L_{in.c}$ are assumed to be the same, equal to L_{in}):

$$\left(i_{abc.}\big|_{t_2}\right)_{\min}=\begin{cases}\dfrac{T_s}{4L_{in}}\left[\sqrt{3}V_{sp}-(1-D_{ab})V_{bus}\right], & D_{ab}\ge1-\dfrac{\sqrt{3}V_{sp}}{V_{bus}}\\ 0, & D_{ab}<1-\dfrac{\sqrt{3}V_{sp}}{V_{bus}}\end{cases}. \tag{41}$$

At t_2, the current of the primary side of WPT tank, i_r, is expressed as:

$$i_r\big|_{t_2}=\frac{-(2V_{bus}/\pi)\sin(D_{ab}\pi/2)\sin\left[(1-D_{ab})\pi/2-\angle Z_r\right]}{|Z_r|}, \tag{42}$$

where Z_r is defined as the equivalent impedance of the resonant tank and secondary side:

$$Z_r=j\omega_sL_p-\frac{j}{\omega_sC_1}+\frac{\omega_s^{2}M^2}{j\omega_sL_s-j/(\omega_sC_2)+R_e}. \tag{43}$$

Therefore, the ZVS current of stage 2, defined as the minimum sum of i_{abc} and i_r at t_2, is obtained as:

$$I_{zvs}=\begin{cases}\dfrac{T_s}{4L_{in}}\left[\sqrt{3}V_{sp}-(1-D_{ab})V_{bus}\right]\\ \quad+\dfrac{-(2V_{bus}/\pi)\sin(D_{ab}\pi/2)\sin\left[(1-D_{ab})\pi/2-\angle Z_r\right]}{|Z_r|}, & D_{ab}\ge1-\dfrac{\sqrt{3}V_{sp}}{V_{bus}}\\ \dfrac{-(2V_{bus}/\pi)\sin(D_{ab}\pi/2)\sin\left[(1-D_{ab})\pi/2-\angle Z_r\right]}{|Z_r|}, & D_{ab}<1-\dfrac{\sqrt{3}V_{sp}}{V_{bus}}\end{cases}, \tag{44}$$

B. Derivation of the limitation of resonant coils design

From Fig. 15, the output power should be smaller than the input power at the conditions of f_s larger than f_3 when D_{ab} is equal to 1; hence, the following expression is obtained:

$$P_{in}(\omega_s)\big|_{D_{ab}=1}=P_{in.\max}\frac{\omega_3}{\omega_s}\ge P_o(\omega_s)\big|_{D_{ab}=1}, \tag{45}$$

which means that:

$$\left[\omega_sP_o(\omega_s)\big|_{D_{ab}=1}\right]_{\max}=\omega_3P_o(\omega_3)\big|_{D_{ab}=1}. \tag{46}$$

When D_{ab} is set as 1, output power P_o can be transformed as:

$$P_o\big|_{D_{ab}=1}=\frac{8(V_o/n)^2}{\pi^2}\frac{1}{\omega_s(M/n)}\sqrt{\frac{\left[\dfrac{V_{bus}}{2(V_o/n)}\right]^2-\left[\dfrac{\left(\omega_sL_p-1/(\omega_sC_1)\right)}{\omega_s(M/n)}\right]^2}{\left[\left(\dfrac{\left(\omega_sL_p-1/(\omega_sC_1)\right)}{\omega_s(M/n)}\right)^2-1\right]^2}}, \tag{47}$$

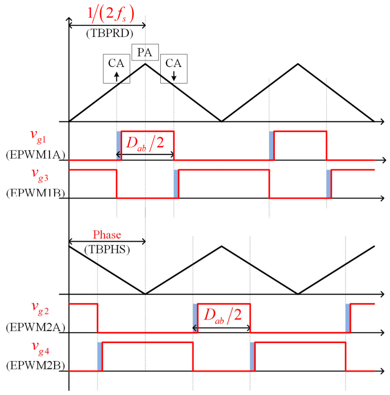


Fig. 31. PWM generation scheme

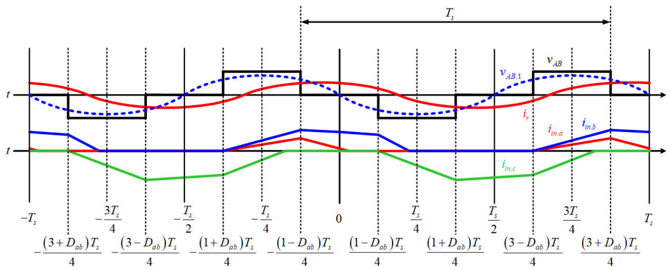


Fig. 32. Ideal waveforms of v_{AB}, $v_{AB.1}$, i_r, $i_{in.a}$, $i_{in.b}$, $i_{in.c}$ for analysis and calculation

where n is defined as the square root of the ratio of L_s and L_p and resonant frequencies (ω_3) of primary and secondary sides are assumed as the same:

$$n=\sqrt{\frac{L_s}{L_p}}, \tag{48}$$

$$\omega_3=\frac{1}{\sqrt{L_pC_1}}=\frac{1}{\sqrt{L_sC_2}}. \tag{49}$$

Hence, from (46) and (47), the following inequality is obtained:

$$\begin{aligned}\omega_s P_o\big|_{D_{ab}=1}&=\frac{8(V_o/n)^2}{\pi^2}\cdot\frac{1}{(M/n)}\cdot\sqrt{\frac{\left[\dfrac{V_{bus}}{2(V_o/n)}\right]^2-\left[\dfrac{\left(\omega_s L_p-\dfrac{1}{\omega_s C_1}\right)}{\omega_s(M/n)}\right]^2}{\left[\left(\dfrac{\left(\omega_s L_p-\dfrac{1}{\omega_s C_1}\right)}{\omega_s(M/n)}\right)^2-1\right]^2}}\\ &\le\frac{8(V_o/n)^2}{\pi^2}\cdot\frac{1}{(M/n)}\cdot\frac{V_{bus}}{2(V_o/n)},\end{aligned} \tag{50}$$

which is solved with the result of (33).

C. PWM generation scheme

TI DSP28335 control card is used as the controller of the proposed topology and Fig. 31 shows its PWM generation scheme. Two EPWM modules (EPWM1 and EPWM2) are used to provide driving signals for switches Q_1-Q_4: EPWM1A for v_{g1}; EPWM1B for v_{g3}; EPWM2A for v_{g2}; and EPWM2B for v_{g4}. The modules' registers TBPRD, CMPA, and TBPHS are control variables corresponding to frequency f_s, duty cycle D_{ab}, and phase difference P_h.

D. Power loss analysis

The overall power loss of the proposed topology mainly consists of power losses of the input filter, input inductors, front-end diodes $D_{r1}-D_{r6}$, switches Q_1-Q_4, resonant coils of WPT tank, and secondary-side diodes $D_{s1}-D_{s4}$, which are analyzed and calculated in details as follows:

1) Input filter

The power loss of the input filter mainly results from its inductors. Due to the current flowing through them is 50 Hz, the core loss is very small and can be ignored compared to the copper loss. Therefore, the power loss of the input filter is calculated as:

$$P_{if}=\begin{cases}\dfrac{6R_{if}}{\pi}\left[\begin{aligned}&\int_0^{\arcsin\left(\frac{1-D_{ab}}{2m}\right)}\left(\frac{V_{sp}T_s}{L_{in}}\frac{D_{ab}{}^2\sin\theta}{8(1-2m\sin\theta)}\right)^2d\theta+\\&\int_{\arcsin\left(\frac{1-D_{ab}}{2m}\right)}^{\frac{\pi}{2}}\left(\frac{V_{sp}T_s}{L_{in}}\frac{-(1/m)(1-D_{ab})^2+2\left(1+D_{ab}{}^2\right)\sin\theta}{32(1-m\sin\theta)}\right)^2d\theta\end{aligned}\right], & D_{ab}>1-2m\\ \dfrac{6R_{if}}{\pi}\displaystyle\int_0^{\frac{\pi}{2}}\left(\frac{V_{sp}T_s}{L_{in}}\frac{D_{ab}{}^2\sin\theta}{8(1-2m\sin\theta)}\right)^2d\theta, & D_{ab}\le 1-2m\end{cases}, \tag{51}$$

where m is defined as the ratio of V_{sp} and V_{bus}, and R_{if} is the equivalent series resistance (ESR) of the inductors of the input filter.

2) Input inductors

From [49] – [51], the formula to calculate core loss with DCM boost inductor current waveform can be derived, and the core loss of input inductors is given by:

$$P_{L_{in}.core}=\begin{cases}3V_ef_s\cdot\dfrac{2}{\pi}\left[\begin{aligned}&\int_0^{\arcsin\left(\frac{1-D_{ab}}{2m}\right)}k_i\left(\frac{\mu_r\mu_0N}{l_e}\frac{V_{sp}\sin\theta}{L_{in}}\frac{D_{ab}}{2f_s}\right)^{\beta-\alpha}\left[\begin{aligned}&\left(\frac{V_{sp}\sin\theta}{NA_e}\right)^{\alpha}\frac{D_{ab}}{2f_s}\\&+\left(\frac{(V_{bus}/2)-V_{sp}\sin\theta}{NA_e}\right)^{\alpha}\frac{D_{ab}}{2f_s}\frac{V_{sp}\sin\theta}{(V_{bus}/2)-V_{sp}\sin\theta}\end{aligned}\right]d\theta+\\&\int_{\arcsin\left(\frac{1-D_{ab}}{2m}\right)}^{\frac{\pi}{2}}k_i\left(\frac{\mu_r\mu_0N}{l_e}\frac{V_{sp}\sin\theta}{L_{in}}\frac{D_{ab}}{2f_s}\right)^{\beta-\alpha}\left[\begin{aligned}&\left(\frac{V_{sp}\sin\theta}{NA_e}\right)^{\alpha}\frac{D_{ab}}{2f_s}+\left(\frac{(V_{bus}/2)-V_{sp}\sin\theta}{NA_e}\right)^{\alpha}\frac{1-D_{ab}}{2f_s}\\&+\left(\frac{V_{bus}-V_{sp}\sin\theta}{NA_e}\right)^{\alpha}\frac{V_{sp}\sin\theta-(V_{bus}/2)(1-D_{ab})}{2(V_{bus}-V_{sp}\sin\theta)f_s}\end{aligned}\right]d\theta\end{aligned}\right], & D_{ab}>1-2m\\ 3V_ef_s\cdot\dfrac{2}{\pi}\displaystyle\int_0^{\frac{\pi}{2}}k_i\left(\frac{\mu_r\mu_0N}{l_e}\cdot\frac{V_{sp}\sin\theta}{L_{in}}\cdot\frac{D_{ab}}{2f_s}\right)^{\beta-\alpha}\left[\begin{aligned}&\left(\frac{V_{sp}\sin\theta}{NA_e}\right)^{\alpha}\frac{D_{ab}}{2f_s}\\&+\left(\frac{(V_{bus}/2)-V_{sp}\sin\theta}{NA_e}\right)^{\alpha}\frac{D_{ab}}{2f_s}\frac{V_{sp}\sin\theta}{(V_{bus}/2)-V_{sp}\sin\theta}\end{aligned}\right]d\theta, & D_{ab}\le 1-2m\end{cases}, \tag{52}$$

where A_e and V_e stand for the cross-sectional area and the volume of the magnetic core respectively. N is the number of coils, μ_r is relative permeability, and μ_0 is the permeability constant. k_i is the constant related to k, α, β, defined as:

$$k_i=\frac{k}{2^{\beta+1}\pi^{\alpha-1}\left(0.2761+\dfrac{1.7061}{\alpha+1.354}\right)}, \tag{53}$$

where constants k, α, β (constants to calculate core loss) can be found from the relevant datasheet.

Copper loss of input inductors is given by:

$$P_{L_{in}.copper}=\begin{cases}\dfrac{6R_{L_{in}}}{\pi}\left[\begin{aligned}&\int_0^{\arcsin\left(\frac{1-D_{ab}}{2m}\right)}\left(\frac{V_{sp}T_s}{L_{in}}\frac{D_{ab}{}^2\sin\theta}{8(1-2m\sin\theta)}\right)^2d\theta+\\&\int_{\arcsin\left(\frac{1-D_{ab}}{2m}\right)}^{\frac{\pi}{2}}\left(\frac{V_{sp}T_s}{L_{in}}\frac{-(1/m)(1-D_{ab})^2+2\left(1+D_{ab}{}^2\right)\sin\theta}{32(1-m\sin\theta)}\right)^2d\theta\end{aligned}\right], & D_{ab}>1-2m\\ \dfrac{6R_{L_{in}}}{\pi}\displaystyle\int_0^{\frac{\pi}{2}}\left(\frac{V_{sp}T_s}{L_{in}}\frac{D_{ab}{}^2\sin\theta}{8(1-2m\sin\theta)}\right)^2d\theta, & D_{ab}\le 1-2m\end{cases}, \tag{54}$$

where R_{Lin} is the ESR of input inductors.

3) Diodes $D_{r1}-D_{r6}$

By analyzing the operation of the proposed topology, each front-end diode conducts for a half-cycle of the line period. Hence, the total losses of diodes $D_{r1}-D_{r6}$ are calculated by:

$$P_{Dr}=\begin{cases}\dfrac{6V_{fr}}{\pi}\left[\begin{aligned}&\int_0^{\arcsin\left(\frac{1-D_{ab}}{2m}\right)}\left(\frac{V_{sp}T_s}{L_{in}}\frac{D_{ab}{}^2\sin\theta}{8(1-2m\sin\theta)}\right)d\theta+\\&\int_{\arcsin\left(\frac{1-D_{ab}}{2m}\right)}^{\frac{\pi}{2}}\left(\frac{V_{sp}T_s}{L_{in}}\frac{-(1/m)(1-D_{ab})^2+2\left(1+D_{ab}{}^2\right)\sin\theta}{32(1-m\sin\theta)}\right)d\theta\end{aligned}\right], & D_{ab}>1-2m\\ \dfrac{6V_{fr}}{\pi}\displaystyle\int_0^{\frac{\pi}{2}}\left(\frac{V_{sp}T_s}{L_{in}}\frac{D_{ab}{}^2\sin\theta}{8(1-2m\sin\theta)}\right)d\theta, & D_{ab}\le 1-2m\end{cases}, \tag{55}$$

where V_{fr} is the forward drop voltage of diodes $D_{r1} – D_{r6}$.

4) Switches $Q_1 – Q_4$

Q_1 and Q_2's conductions occur at stage 3 and stage 7, as shown in Fig. 13 (e), (f), (l) and (m) and their conduction losses are calculated as (56) and (57). Q_3 and Q_4's conductions occur at stage 1 and stage 5, as shown in Fig. 13 (a), (b), and (i) and their conduction losses are calculated as (58).

$$P_{Q_1.con} = \frac{6R_{ds.on.12}}{T_l T_s}\int_0^{\frac{T_l}{6}}\left[\int_{\frac{3-D_{ab}}{4}T_s}^{\frac{3+D_{ab}}{4}T_s}\left(i_{abc}+i_r\right)^2 dt\right]dt, \tag{56}$$

$$P_{Q_2.con} = \frac{6R_{ds.on.12}}{T_l T_s}\int_0^{\frac{T_l}{6}}\left[\int_{\frac{1-D_{ab}}{4}T_s}^{\frac{1+D_{ab}}{4}T_s}\left(i_{abc}+i_r\right)^2 dt\right]dt, \tag{57}$$

$$P_{Q_3.con} = P_{Q_4.con} = \frac{6R_{ds.on.34}}{T_l T_s}\int_0^{\frac{T_l}{6}}\left[\int_{-\frac{1-D_{ab}}{4}T_s}^{\frac{1-D_{ab}}{4}T_s}\left(i_{abc}+i_r\right)^2 dt + \int_{\frac{1+D_{ab}}{4}T_s}^{\frac{3-D_{ab}}{4}T_s}\left(i_{abc}+i_r\right)^2 dt\right]dt, \tag{58}$$

where i_r and i_{abc} can be obtained from (65) and (69) in Appendix. $R_{ds.on.12}$ is defined as the drain-source ON resistance of Q_1 and Q_2 while $R_{ds.on.34}$ is defined as that of Q_3 and Q_4.

If ZVS can be achieved for switches $Q_1 – Q_4$, there will be no switching loss theoretically. However, as analyzed in section II.E, ZVS cannot be fully achieved for the switches at relatively low load conditions. At the instant of Q_2's turning-ON and Q_4's turning-OFF, when i_{abc} reaches zero and i_r is negative, hard-switching will occur instead of ZVS. Due to the symmetry of operation, power losses of Q_1's turning-ON and Q_3's turning-OFF are equal to those of Q_2's turning-ON and Q_4's turning-OFF respectively and can be calculated as:

$$P_{Q_1.sw} = P_{Q_2.sw} = \frac{1}{2}\cdot\frac{V_{bus}}{2}\cdot\left(i_r\big|_{t=\frac{(3-D_{ab})T_s}{4}}\right)\cdot t_{r.12}\cdot f_s, \tag{59}$$

$$P_{Q_3.sw} = P_{Q_4.sw} = \frac{1}{2}\cdot\frac{V_{bus}}{2}\cdot\left(i_r\big|_{t=\frac{(3-D_{ab})T_s}{4}}\right)\cdot t_{f.34}\cdot f_s, \tag{60}$$

where i_r can be obtained from (65) in Appendix. $t_{r.12}$ is the rise time of switches Q_1 and Q_2 while $t_{f.34}$ is the fall time of switches Q_3 and Q_4, which can be obtained from relevant datasheets.

5) Resonant coils of WPT tank

Copper losses of primary-side and secondary-side coils of WPT tank are calculated as:

$$P_{Lp} = \left[\frac{\sqrt{2}V_{bus}\sin\left(D_{ab}\pi/2\right)}{\pi\left|Z_r\right|}\right]^2\cdot R_{lp}, \tag{61}$$

$$P_{Ls} = \left[\frac{2\sqrt{2}V_o}{\pi R_e}\right]^2\cdot R_{ls}, \tag{62}$$

where Z_r and R_e can be obtained from (43) and (8) respectively.

6) Diodes $D_{s1} – D_{s4}$

The total losses of secondary-side diodes $D_{s1} – D_{s4}$ are calculated as:

$$P_{Ds} = 4\cdot\frac{1}{\pi}\cdot\frac{4V_o}{\pi R_e}\cdot V_{fs} = \frac{16V_oV_{fs}}{\pi^2 R_e}, \tag{63}$$

where V_{fs} is the forward drop voltage of diodes $D_{s1} – D_{s4}$.

E. Other expressions

Fig. 32 shows the ideal waveforms of the proposed converter for analysis and calculation, where $v_{AB.1}$ is the fundamental component of v_{AB}, calculated as:

$$v_{AB.1} = -\left(2V_{bus}/\pi\right)\sin\left(D_{ab}\pi/2\right)\sin\left(\omega_s t\right). \tag{64}$$

Z_r is defined as the equivalent impedance of the WPT resonant tank and the secondary-side circuit, calculated as (43). Therefore, the current flowing through the primary side of the WPT resonant tank, i_r, is calculated as:

$$i_r = \frac{v_{AB.1}}{Z_r} = \frac{-\left(2V_{bus}/\pi\right)\sin\left(D_{ab}\pi/2\right)\sin\left[\omega_s t - \angle Z_r\right]}{\left|Z_r\right|}, \tag{65}$$

In the following calculations, $v_{s.x}$ (x=a, b, or c) means equivalent phase voltage $v_{s.a}$, $v_{s.b}$, or $v_{s.c}$:

$$v_{s.a} = V_{sp}\sin\left(\omega_l t\right), \tag{66}$$

$$v_{s.b} = V_{sp}\sin\left(\omega_l t - \frac{2}{3}\pi\right), \tag{67}$$

$$v_{s.c} = V_{sp}\sin\left(\omega_l t - \frac{4}{3}\pi\right), \tag{68}$$

$i_{in.x}$ means input inductor current $i_{in.a}$, $i_{in.b}$, or $i_{in.c}$. i_{abc} is the sum of $i_{in.a}$, $i_{in.b}$, and $i_{in.c}$:

$$i_{abc} = i_{in.a} + i_{in.b} + i_{in.c}, \tag{69}$$

where $i_{in.a}$, $i_{in.b}$, and $i_{in.c}$ are calculated as (70):

$$i_{in.x} = \begin{cases}
\begin{cases}
\frac{v_{s.x}}{L_{in}}\frac{D_{ab}T_s}{2} - \frac{V_{bus}/2 - v_{s.x}}{L_{in}}\left(t + \frac{(1-D_{ab})T_s}{4}\right) & -\frac{(1-D_{ab})T_s}{4} \le t < \frac{(1-D_{ab})T_s}{4} \\
\frac{v_{s.x}}{L_{in}}\frac{D_{ab}T_s}{2} - \frac{V_{bus}/2 - v_{s.x}}{L_{in}}\frac{(1-D_{ab})T_s}{2} - \frac{V_{bus} - v_{s.x}}{L_{in}}\left(t - \frac{(1-D_{ab})T_s}{4}\right) & \frac{(1-D_{ab})T_s}{4} \le t < t_w \\
0 & t_w \le t < \frac{(3-D_{ab})T_s}{4} \\
\frac{v_{s.x}}{L_{in}}\left(t - \frac{(3-D_{ab})T_s}{4}\right) & \frac{(3-D_{ab})T_s}{4} \le t \le \frac{(3+D_{ab})T_s}{4}
\end{cases}, & v_{s.x} > \frac{(1-D_{ab})}{2}V_{bus} \\
\begin{cases}
\frac{v_{s.x}}{L_{in}}\frac{D_{ab}T_s}{2} - \frac{V_{bus}/2 - v_{s.x}}{L_{in}}\left(t + \frac{(1-D_{ab})T_s}{4}\right) & -\frac{(1-D_{ab})T_s}{4} \le t < t_x \\
0 & t_x \le t < \frac{(3-D_{ab})T_s}{4} \\
\frac{v_{s.x}}{L_{in}}\left(t - \frac{(3-D_{ab})T_s}{4}\right) & \frac{(3-D_{ab})T_s}{4} \le t \le \frac{(3+D_{ab})T_s}{4}
\end{cases}, & 0 \le v_{s.x} \le \frac{(1-D_{ab})}{2}V_{bus} \\
\begin{cases}
0 & -\frac{(1-D_{ab})T_s}{4} \le t < \frac{(1-D_{ab})T_s}{4},\ t_y \le t < \frac{(3+D_{ab})T_s}{4} \\
\frac{v_{s.x}}{L_{in}}\left(t - \frac{(1-D_{ab})T_s}{4}\right) & \frac{(1-D_{ab})T_s}{4} \le t < \frac{(1+D_{ab})T_s}{4} \\
\frac{v_{s.x}}{L_{in}}\frac{D_{ab}T_s}{2} - \frac{-V_{bus}/2 - v_{s.x}}{L_{in}}\left(t - \frac{(1+D_{ab})T_s}{4}\right) & \frac{(1+D_{ab})T_s}{4} \le t < t_y
\end{cases}, & 0 > v_{s.x} \ge -\frac{(1-D_{ab})}{2}V_{bus} \\
\begin{cases}
0 & -\frac{(1-D_{ab})T_s}{4} \le t < \frac{(1-D_{ab})T_s}{4},\ t_z \le t < \frac{(3+D_{ab})T_s}{4} \\
\frac{v_{s.x}}{L_{in}}\left(t - \frac{(1-D_{ab})T_s}{4}\right) & \frac{(1-D_{ab})T_s}{4} \le t < \frac{(1+D_{ab})T_s}{4} \\
\frac{v_{s.x}}{L_{in}}\frac{D_{ab}T_s}{2} - \frac{-V_{bus}/2 - v_{s.x}}{L_{in}}\left(t - \frac{(1+D_{ab})T_s}{4}\right) & \frac{(1+D_{ab})T_s}{4} \le t < \frac{(3-D_{ab})T_s}{4} \\
\frac{v_{s.x}}{L_{in}}\frac{D_{ab}T_s}{2} - \frac{-V_{bus}/2 - v_{s.x}}{L_{in}}\frac{(1-D_{ab})T_s}{2} - \frac{-V_{bus} - v_{s.x}}{L_{in}}\left(t - \frac{(3-D_{ab})T_s}{4}\right) & \frac{(3-D_{ab})T_s}{4} \le t < t_z
\end{cases}, & v_{s.x} < -\frac{(1-D_{ab})}{2}V_{bus}
\end{cases} \tag{70}$$

where t_w, t_x, t_y, t_z are calculated as:

$$t_w = \frac{2v_{s.x} - V_{bus}\left(1-D_{ab}\right)}{V_{bus} - v_{s.x}}\cdot\frac{T_s}{4} + \frac{\left(1-D_{ab}\right)T_s}{4}, \tag{71}$$

$$t_x = \frac{v_{s.x}}{V_{bus}/2 - v_{s.x}}\cdot\frac{D_{ab}T_s}{2} - \frac{\left(1-D_{ab}\right)T_s}{4}, \tag{72}$$

$$t_y = \frac{-v_{s.x}}{V_{bus}/2 + v_{s.x}}\cdot\frac{D_{ab}T_s}{2} + \frac{\left(1+D_{ab}\right)T_s}{4}, \tag{73}$$

$$t_z = \frac{-2v_{s.x} - V_{bus}\left(1-D_{ab}\right)}{V_{bus} + v_{s.x}}\cdot\frac{T_s}{4} + \frac{\left(3-D_{ab}\right)T_s}{4}. \tag{74}$$

REFERENCES

[1] Y. Jang and M. M. Jovanovic, "A contactless electrical energy transmission system for portable-telephone battery chargers," *IEEE Trans. Ind. Electron.*, vol. 50, no. 3, pp. 520–527, Mar. 2003.

[2] G. B. Joung and B. H. Cho, "An energy transmission system for an artificial heart using leakage inductance compensation of transcutaneous transformer," *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1013–1022, Nov. 1998.

[3] Y. Wang and D. Ma, "Design of integrated dual-loop Δ−Σ modulated switching power converter for adaptive wireless powering in biomedical implants," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4241–4249, Sep. 2011.

[4] D. Ahn and S. Hong, “Wireless power transmission with self-regulated output voltage for biomedical implant,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2225–2235, May 2014.

[5] S. Li and C.C. Mi, “Wireless power transfer for electric vehicle applications,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Vol. PP, pp. 1, Apr, 2014

[6] C. S. Wang, O. H. Stielau, and G. A. Covic, “Design considerations for a contactless electric vehicle battery charger,” *IEEE Trans. Ind. Electron.*, vol. 52, no. 5, pp. 1308–1313, Oct. 2005.

[7] J. Shin, S. Shin, Y. Kim, S. Ahn, S. Lee, G. Jung, S. Jeon, and D. H. Cho, “Design and implementation of shaped magnetic resonance based wireless power transfer system for roadway-powered moving electric vehicles,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1179–1192, Mar. 2014.

[8] G. A. Covic, J. T. Boys, M. L. G. Kissin, and H. G. Lu, “A three-phase inductive power transfer system for roadway-powered vehicles,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3370–3378, Dec. 2007.

[9] N. L. Zhen, R. A. Chinga, R. Tseng, and L. Jenshan, “Design and test of a high-power high-efficiency loosely coupled planar wireless power transfer system,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1801–1812, May 2009.

[10] J. J. Casanova, Z. N. Low, and J. Lin, “A loosely coupled planar wireless power system for multiple receivers,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3060–3068, Aug. 2009.

[11] S. C. Moon, B. C. Kim, S. Y. Cho, C. H. Ahn, and G. W. Moon, “Analysis and design of a wireless power transfer system with an intermediate coil for high efficiency,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5861–5870, Nov 2014.

[12] D. Ahn and S. Hong, “A study on magnetic field repeater in wireless power transfer,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 360–371, Jan. 2013.

[13] U. K. Madawala and D. J. Thrimawithana, “A bidirectional inductive power interface for electric vehicles in V2G systems,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4789–4896, Oct. 2011.

[14] A. J. Moradewicz and M. P. Kazmierkowski, “Contactless energy transfer system with FPGA-controlled resonant converter,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3181–3190, Sep. 2010.

[15] Y. Li, R. Mai, L. Lu, and Z. He, “Active and reactive currents decomposition-based control of angle and magnitude of current for a parallel multiinverter IPT system,” *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1602–1614, Feb. 2017.

[16] B. L. Cannon, J. F. Hoburg, D. D. Stancil, and S. C. Goldstein, “Magnetic resonant coupling as a potential means for wireless power transfer to multiple small receivers,” *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1819–1825, Jul. 2009.

[17] T. C. Beh, M. Kato, T. Imura, S. Oh, and Y. Hori, “Automated impedance matching system for robust wireless power transfer via magnetic resonance coupling,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3689–3698, Sep. 2013.

[18] C. Linhui, L. Shuo, C. Z. Yong, and J. C. Tie, “An optimizable circuit structure for high-efficiency wireless power transfer,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 339–349, Jan. 2013.

[19] R. Johari, J. V. Krogmeire, and D. J. Love, “Analysis and practical considerations in implementing multiple transmitters for wireless power transfer via coupled magnetic resonance,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 4, pp. 1774–1783, Apr. 2013.

[20] A. P. Sample, D. A. Meyer, and J. R. Smith, “Analysis, experimental results, and range adaptation of magnetically coupled resonators for wireless power transfer,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 544–554, Feb. 2011.

[21] T. Imura and Y. Hory, “Maximizing air gap and efficiency of magnetic resonant coupling for wireless power transfer using equivalent circuit and Neumann formula,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4746–4752, Oct. 2011.

[22] André Kurs, Aristeidis Karalis, Robert Moffatt, J. D. Joannopoulos, Peter Fisher, Marin Soljačić, “Wireless power transfer via strongly coupled magnetic resonances,” in *Science Express* on 7 June 2007, Vol. 317. no. 5834, pp. 83 – 86.

[23] M. Liserre, F. Blaabjerg and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," in *IEEE Trans. on Ind. Appl.*, vol. 41, no. 5, pp. 1281-1291, Sept.-Oct. 2005.

[24] L. Huber, M. Kumar and M. M. Jovanović, "Performance comparison of three-step and six-step PWM in average-current-controlled three-phase six-switch boost PFC rectifier," in *IEEE Trans. on Power Electron.*, vol. 31, no. 10, pp. 7264-7272, Oct. 2016.

[25] J. W. Kolar and T. Friedli, "The essence of three-phase PFC rectifier systems—part I," in *IEEE Trans. on Power Electron.*, vol. 28, no. 1, pp. 176-198, Jan. 2013.

[26] Y. Jang and M. M. Jovanović, "The Taipei rectifier — A new three-phase two-switch ZVS PFC DCM boost rectifier," in *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 686-694, Feb. 2013.

[27] K. Yao, Q. Meng, Y. Bo and W. Hu, "Three-phase single-switch DCM boost PFC converter with optimum utilization control of switching cycles," in *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 60-70, Jan. 2016.

[28] P. J. Grbovic, P. Delarue and P. Le Moigne, "A novel three-phase diode boost rectifier using hybrid half-DC-bus-voltage rated boost converter," in *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1316-1329, Apr. 2011.

[29] V. F. Pires and J. F. A. Silva, "Single-stage three-phase buck-boost type AC-DC converter with high power factor," in *IEEE Trans. Power Electron.*, vol. 16, no. 6, pp. 784-793, Nov. 2001.

[30] M. Narimani and G. Moschopoulos, “A new interleaved three-phase single-stage PFC AC-DC converter,” in *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 648-654, Feb. 2014.

[31] M. Narimani and G. Moschopoulos, "A new interleaved three-phase single-stage PFC AC-DC converter with flying capacitor," in *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3695-3702, Jul. 2015.

[32] P. M. Barbosa, F. Canales, J. M. Burdio and F. C. Lee, "A three-level converter and its application to power factor correction," in *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1319-1327, Nov. 2005.

[33] D. S. Wijeratne and G. Moschopoulos, "A three-phase single-stage AC-DC PWM buck-type full-bridge converter: analysis, design, and characteristics," in *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4201-4214, Oct. 2013.

[34] F. S. Hamdad and A. K. S. Bhat, "A novel soft-switching high-frequency transformer isolated three-phase AC-to-DC converter with low harmonic distortion," in *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 35-45, Jan. 2004.

[35] J. G. Contreras and I. Barbi, "A three-phase high power factor PWM ZVS power supply with a single power stage," *Power Electronics Specialists Conference, PESC '94 Record., 25th Annual IEEE*, Taipei, 1994, pp. 356-362 vol.1.

[36] D. Wijeratne and G. Moschopoulos, "Analysis and design of a novel integrated three-phase single-stage ac-dc PWM full-bridge converter," *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Palm Springs, CA, 2010, pp. 829-836.

[37] Y. Jang and M. M. Jovanović, "The single-stage Taipei rectifier—design consideration and performance evaluation," in *IEEE Trans. on Power Electron.*, vol. 29, no. 11, pp. 5706-5714, Nov. 2014.

[38] M. Moghaddami, A. Anzalchi and A. I. Sarwat, "Single-stage three-phase AC-AC matrix converter for inductive power transfer systems," in *IEEE Trans. Ind. Electron.*, vol. 63, no. 10, pp. 6613-6622, Oct. 2016.

[39] N. Xuan Bac, D. M. Vilathgamuwa and U. K. Madawala, "A SiC-Based Matrix Converter Topology for Inductive Power Transfer System," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4029-4038, Aug. 2014.

[40] M. Moghaddami and A. I. Sarwat, "Single-phase soft-switched AC–AC matrix converter with power controller for bidirectional inductive power transfer systems," in *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3760-3770, July-Aug. 2018.

[41] J. Liu, K. W. Chan, C. Y. Chung, N. H. L. Chan, M. Liu and W. Xu, "Single-stage wireless-power-transfer resonant converter with boost bridgeless power-factor-correction rectifier," in *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2145-2155, March 2018.

[42] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," in *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899-907, Feb. 2013.

[43] STMicroelectronics Group of Companies, “LLC resonant half-bridge converter design guideline,” STMicroelectronics, Geneva, Switzerland, Appl. Note AN2450.

[44] W. X. Zhong and S. Y. R. Hui, "Maximum energy efficiency tracking for wireless power transfer systems," in *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 4025-4034, Jul. 2015.

[45] X. Zhou, W. Sun, D. Gao, S. Lin, and Z. Hu, “Power factor correction method using three-phase single-switch circuit for wireless power transfer system,” in *Automation of Electric Power Systems*, Vol. 43, No. 2, Jan. 25, 2019.

[46] M. Bojarski, E. Asa, K. Colak and D. Czarkowski, "A 25 kW industrial prototype wireless electric vehicle charger," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 1756-1761.
[47] O. C. Onar, S. Campbell, L. Seiber, C. White, M. Chinthavali, L. Tang, P. Chambon, B. Ozpineci, and D. E. Smith, *Oak Ridge National Laboratory Wireless Charging of Electric Vehicles - CRADA Report*, United States: N. p., 2016. Web. doi:10.2172/1263875.
[48] L. Jiang, F. Tamjid, C. Zhao, D. Costinett, A. Fath and S. Yang, "A GaN-based 100 W two-stage wireless power transmitter with inherent current source output," *2016 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (WoW)*, Knoxville, TN, 2016, pp. 65-72.
[49] F. D. Tan, J. L. Vollin, and S. M. Cuk, “A practical approach for magnetic core-loss characterization,” in *IEEE Trans. Power Electron.*, vol. 10, no. 2, pp. 124–129, Mar. 1995.
[50] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, “Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters,” in *Proc. IEEE Workshop Comput. Power Electron.*, Jun. 2002, pp. 36–41.
[51] T. Nussbaumer, K. Raggl, and J. W. Kolar, “Design guidelines for interleaved single-phase boost PFC circuits,” in *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2559–2573, Jul. 2009.

Junwei Liu received his B.Eng. degree in water conservancy and hydropower engineering from Huazhong University of Science and Technology, China, in 2012, and the Ph.D. degree in the Department of Electrical Engineering, The Hong Kong Polytechnic University, Hong Kong, in 2018.

His research interests include wireless power transfer, AC-DC single-stage topologies, and high power DC-DC conversions.

Wenzheng Xu received his B.Eng. degree from the Department of Electrical Engineering, Beijing Jiaotong University, Beijing, China, in 2012, and the M.Sc. degree from the Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong, in 2013. He is currently working toward the Ph.D. degree in the Department of Electrical Engineering, the Hong Kong Polytechnic University, Hong Kong.

His research interests include power electronics topologies and control of bidirectional converters.

Ka Wing Chan (M’98) received the B.Sc. (Hons) and Ph.D. degrees in electronic and electrical engineering from the University of Bath, U.K., in 1988 and 1992, respectively.

Currently he is an Associate Professor and Associate Head in the Department of Electrical Engineering of the Hong Kong Polytechnic University. His general research interests include power system stability, analysis and control, power grid integration, security, resilience and optimization, demand response management, etc.

Ming Liu received his B.Eng. degree in electrical engineering from Qingdao University, Qingdao, China, in 2014. Currently, he is working toward the Ph.D. degree in the Department of Electrical Engineering, The Hong Kong Polytechnic University, Hong Kong.

His research interests include electric machine design and control, wireless power transfer topologies, and finite element analysis.

Xian Zhang received the B.Sc. degree from North China Electric Power University, China, in 2009, the M.Sc. degree from Tsinghua University, China, in 2012, and the Ph.D. degree from The Hong Kong Polytechnic University, in 2019, all in electrical engineering.

Her main fields of interest include smart grid and electric vehicle.

Nelson H. L. Chan received his B.Eng. and Ph.D. Degree from the Department of Electrical Engineering, The Hong Kong Polytechnic University (HKPolyU) in 1996 and 2000 respectively. He has been working with HKPolyU as senior research fellow since 2010.

His research interests include power electronics, power system, control theory and artificial intelligence.