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An Adaptive Fault Ride-Through Scheme for Grid-Forming Inverters under Asymmetrical Grid Faults

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[1]***Abstract*—Three-phase four-wire (3P4W) grid-forming (GFM) inverters are promising to interface distributed energy resources (DERs) into low-voltage networks. However, these inverters are prone to overcurrent under grid faults. Physically increasing the inverter current capacity is not cost-effective to cope with complicated fault conditions. In this paper, an adaptive fault ride-through (FRT) scheme based on instantaneous saturators and virtual negative- and zero-sequence resistances is proposed. It features not only overcurrent limitation by modifying voltage references but also seamless transition between normal and grid fault conditions. The proposed FRT scheme is first analyzed from different aspects, including the virtual sequence resistances, grid short-circuit ratio (*SCR*), fault types, and fault levels. The virtual sequence resistances are then designed to be adaptive to ensure high voltage quality at the healthy phase. The proposed FRT scheme is verified by MATLAB/Simulink simulations under asymmetrical faults. A laboratory platform with a grid-connected 3kW GFM inverter is further constructed to demonstrate its effectiveness. (A video of the experimental results under three asymmetrical faults is attached)**

***Index Terms*—Asymmetrical faults, current limiting, fault ride-through, grid-forming inverter, three-phase four-wire, virtual impedance.**

I. INTRODUCTION

RENEWABLE energy sources (RESs), like wind and solar, play a significant role in reducing carbon emissions. They are usually interfaced to power grids via a voltage-source inverter (VSI) with grid-following (GFL) strategies [1-3]. However, the high penetration of GFL inverters leads to issues such as voltage rise [1] and system instability [2].

Meanwhile, grid-forming (GFM) inverters, which were initially developed for islanded microgrids, regain researchers' attention as alternatives for RES integration. Unlike GFL, GFM inverters behave as voltage sources and synchronize with the external system via power exchange [4] as synchronous generators (SGs). Therefore, they can operate under both islanded and grid-tied modes and provide frequency damping and resilience [5], [6]. Several GFM strategies, including droop control [7], virtual synchronous generator (VSG) [8], synchronous-power control (SPC) [9], have been proposed and achieved satisfactory performances in electric systems.

In real-world systems, there are inevitable grid disturbances, and grid faults threaten system safety severely. GFM inverters are very sensitive to grid voltage variations and easily experience failures when subjected to grid faults because they can usually withstand a maximum current of only about 1.2~2.0p.u. [10-15]. Traditionally, inverters can be tripped to prevent overcurrent damage. However, in future inverter-dominant power networks, GFM inverters have to keep connected and ride through grid faults [6]. In addition, similar to SGs, GFM inverters may also experience transient instability if the fault is not timely cleared [7], [16]. Hence, a current limiting function with the consideration of transient stability becomes compulsory for GFM inverters.

Available current limiting strategies for GFM inverters can be categorized as hardware-based and software-based. In the first category, additional hardware devices, including fault current limiter [17] and hysteresis compensator [18], are used to suppress fault currents. Nevertheless, they are costly and not suitable for GFM inverters. In contrast, software-based strategies do not require any additional hardware elements. Despite issues related to digital control and signal sampling delays and the nonexistence in power circuits, software-based strategies present more intelligence and can be flexibly integrated into inverter controllers. Such software-based schemes can be further divided into direct and indirect methods.

The basic idea behind the direct current limitation methods is to control current references if a fault is detected. In [18-21], the GFM inverter is switched from the normal voltage-source mode (VSM) to a current-source mode (CSM) during the fault to output predefined currents. With CSM, the inverter voltage is left uncontrolled, and the healthy phase(s) may experience overvoltage during asymmetrical faults, which can be

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alleviated by a parallel virtual impedance [20], [21]. Though CSM can achieve good current limitation performance, the inverter's voltage source characteristics are lost. Besides, fast and accurate fault detection is needed. Moreover, an additional scheme for the seamless transition between VSM and CSM increases the computation burden significantly.

Alternatively, current references can also be modified directly based on the maximum value [7], [10], [13-15], [22]. A simple method is to saturate the *dq*-axis current components [15]. The inverter current is well limited in symmetrical faults; however, distortions occur in asymmetrical faults, which is also the case with amplitude limiters in [7] and [22]. Thus, a current limiting factor (CLF) [10], circular current limiter (CCL) [9], sinusoidal current limiter (SCL) [13], and natural reference frame current limiter (NARF-CL) [14] are proposed to scale down references and enhance power qualities. Shortcomings in [10] are the necessary fault detection, amplitude calculation, and two sets of controllers. The CCL-based scheme in [9] comes with a dedicated, dynamic virtual resistor to dampen the postfault response and is not yet examined by asymmetrical faults. As for the SCL in [13], the calculation of current references and the couplings between the SCL and virtual impedance make it challenging to design the whole strategy. In [14], the fast magnitude calculator of the NARF-CL is based on derivative operations, which cannot work properly under distorted conditions.

On the other hand, the indirect methods modify voltage references to limit currents without losing the voltage source behavior. For directly voltage-controlled inverters, they are protected from overcurrent by calculating the voltage controller output using the connection point voltage, filter impedance, and pre-fault current [23]. A similar voltage limiter is also found in [4]. Nevertheless, these schemes fail to obtain satisfactory results under asymmetrical faults. Compared with the voltage limitation, virtual impedances are more popular for overcurrent protection [11], [16], [24-27]. A virtual impedance, either constant [24], [26], [27] or proportional to current errors [11], [16], [25], is activated to reduce voltage references once output currents exceed a threshold. Here, it is emphasized that the inverter current may not be well limited due to the dependence on fault levels, network impedances, and the selected virtual impedance [9], [28]. A large virtual impedance is desirable for current limitations, but it can cause instabilities. Thus, maximum current and practical networks need to be considered in the virtual impedance design [25, 26]. It is also noted that synchronization stability and asymmetrical faults are rarely studied in the virtual impedance schemes. Though adaptive droop gains in [16] increase the critical clearing time to about 0.95s, it is still not sufficient for GFM inverters in low-voltage systems, in which 1~3s are required to clear grid faults [29].

A recent overview concerning GFM inverters can be found in [30], in which the state-of-the-art FRT functions, mainly focused on the current limiting and fault recovery process, are presented. Nevertheless, in the future development of GFM inverters, the desired FRT capabilities need to go further to include 1) maintaining the voltage source behavior, 2) limiting the faulty phase current, 3) preserving the healthy phase voltage with good power qualities, and 4) stable synchronization during faults. The GFM inverters should also handle both symmetrical and asymmetrical faults under complicated grid and fault conditions. Unfortunately, to the best of our knowledge, the currently available limiting strategies still cannot meet all these requirements simultaneously.

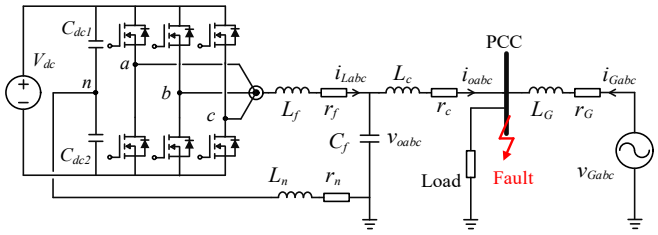


Fig. 1. Droop-controlled inverter connected to a three-phase four-wire grid.

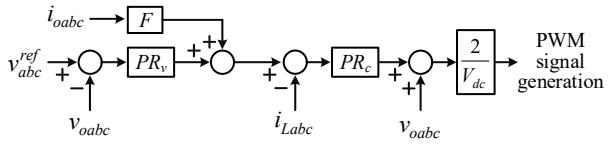


Fig. 2. Inner voltage and current controllers of the inverter on the *abc* frame.

Therefore, to bridge the above research gaps, an adaptive FRT scheme built on our previous efforts in [28] is proposed here for GFM inverters. Since the current limiting and synchronization stability under symmetrical grid faults have already been addressed in [28], this paper will mainly focus on various asymmetrical grid faults. Equipped with the proposed FRT scheme, the GFM inverters can deal with both symmetrical and asymmetrical faults, and the scheme can also be easily adapted for three-phase three-wire (3P3W) inverters by eliminating the zero-sequence. Specifically, the proposed FRT scheme shows the following distinct advantages:

1) Faulty phase current is effectively limited without losing the voltage source characteristics.
2) Healthy phase voltage is maintained within the allowable range to continue power supplies with good power quality.
3) Sharing of negative- and zero-sequence currents is enhanced under both normal and faulty conditions.
4) Easy implementation is achieved without modifying the inner loop voltage and current controllers.
5) Seamless transition between the normal and grid fault conditions is realized without fault detection and change of control principles.

II. Proposed Fault Ride-Through Scheme with Virtual Sequence Resistances

Fig. 1 shows a three-phase four-wire (3P4W) inverter system. The grid is represented by a voltage source v_{Gabc} and its equivalent inductance L_G and resistance r_G. In this work, the grid voltage is V_G=1.0p.u. and its impedance ratio r_G/X_G is set to 1 to emulate the minimum power decoupling of a low voltage distribution network for integrating distributed generations with droop-controlled inverters [31]. The inverter has a three-phase, three-leg topology, and the neutral point is created by splitting dc capacitors and grounded via a resistor r_n and an inductor L_n. An output LC filter is to attenuate switching ripples. The system is multi-grounded, as shown in Fig. 1. The coupling impedance Z_c with L_c and r_c connects the inverter to the point of common coupling (PCC). In order to realize GFM

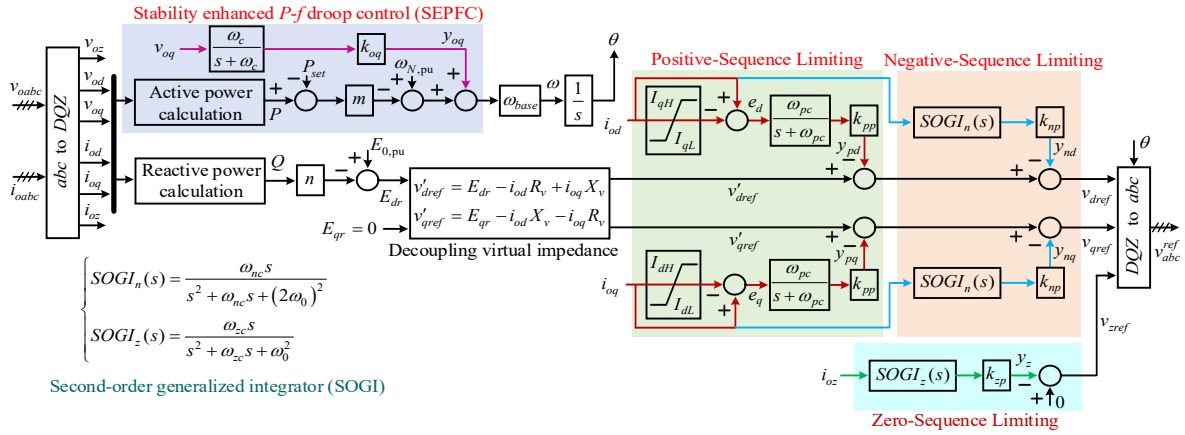


Fig. 3. The proposed PNZSL-SEPFC scheme for droop-controlled inverters to ride through various grid faults.

functionalities, the *P-f* and *Q-V* droop is adopted. Virtual resistance R_v and reactance X_v are also introduced to decouple the active and reactive droops. After voltage references are generated in the primary controller, they are fed to the inner loop controllers, which are implemented on the *abc* frame using proportional and resonant (*PR*) controllers, as depicted in Fig. 2. The maximum current is $I_{N\max}$=2.0p.u., and other parameters of the inverter are presented in Table I.

The desired FRT scheme for GFM inverters should limit the faulty phase current and maintain the healthy phase power supplies. It should also ensure proper sharing of negative- and zero-sequence currents under asymmetrical faults; otherwise, the inverter electrically close to the fault would pick up most of the negative- and zero-sequence currents, causing large ripples in its dc link. Bearing in mind these characteristics, an FRT scheme in Fig. 3, namely, positive-negative-zero-sequence limiting with stability enhanced *P-f* droop control (PNZSL-SEPFC), is proposed for droop-controlled inverters. In Fig. 3, the SEPFC can help maintain the inverter's synchronization stability with the external system under severe grid faults, and the PNZSL is adaptively responsible for limiting faulty phase current(s), maintaining healthy phase voltage(s), and ensuring the proper sharing of unbalanced currents. This strategy can also be easily implemented in the inverter's primary control and does not change the inner loop voltage and current control. Therefore, the PNZSL-SEPFC can satisfy the mentioned desirable FRT functions in GFM inverters, which will be explained in the remaining part of this article.

A. Positive-sequence limiting with SEPFC

As illustrated in Fig. 3, the positive-sequence limiting is based on instantaneous saturators using *dq*-axis currents as inputs to generate a current error vector

$$\mathbf{e}_{dq} = \begin{cases} \mathbf{i}_{odq} - \mathbf{I}_{dqH}, & \mathbf{i}_{odq} > \mathbf{I}_{dqH} \\ 0, & \mathbf{I}_{dqL} \le \mathbf{i}_{odq} \le \mathbf{I}_{dqH} \\ \mathbf{i}_{odq} - \mathbf{I}_{dqL}, & \mathbf{i}_{odq} < \mathbf{I}_{dqL} \end{cases} \quad (1)$$

where $\mathbf{e}_{dq} = [e_d, e_q]$ is the current error vector, $\mathbf{i}_{odq} = [i_{od}, i_{oq}]$ the *dq*-axis per-unit current vector, and the upper and lower threshold vectors are $\mathbf{I}_{dqH} = [I_{dH}, I_{qH}]$ and $\mathbf{I}_{dqL} = [I_{dL}, I_{qL}]$, respectively. When either i_{od} or i_{oq} exceeds its thresholds, a corresponding component y_{pd} or y_{pq} will be generated to change the positive-sequence voltage components accordingly. A low-pass filter (LFP) with cutoff frequency ω_{pc} is to slow down dynamics and attenuate harmonics, especially second-order oscillations caused by the negative-sequence current.

Similar to SGs, a *P-f* droop-controlled inverter may also fail to synchronize with external systems under grid faults because the current and power are constrained [7]. Hence, as presented in Fig. 3, the *q*-axis voltage is fed back to regulate the inverter frequency. This stability enhanced *P-f* droop control (SEPFC) [7] shows superior performance with the positive-sequence limiting under symmetrical faults [28]. Therefore, this article will be focused on negative- and zero-sequence limitings.

B. Negative- and zero-sequence limitings

At the primary control stage, the grid-forming control algorithm sets the synchronous phase and modifies the positive-sequence voltage amplitude, leading to a nonlinear and operating point-based positive-sequence impedance [32, 33]. While the negative- and zero-sequence voltage settings are usually zero [29], and as a result, the primary control stage presents zero negative- and zero-sequence impedances. In addition, with well-designed voltage and current controllers, the inner loop control will also have negligible sequence output impedances at the fundamental frequency. Although virtual impedance may be used to decouple the active and reactive droops, it is usually small and slightly changes the positive- and negative-sequence impedances. Hence, from the perspective of the external system, the inverter is of small negative- and zero-sequence output impedances and prone to substantial negative- and zero-sequence currents when an asymmetrical fault is electrically close. The negative-sequence current will appear as oscillations in i_{od} and i_{oq}, which can be clipped by the positive-sequence limiting, leading to unwanted three-phase voltage drops under asymmetrical faults. At the same time, the zero-sequence current flows into the neutral point and causes stresses to dc side components.

Therefore, virtual negative- and zero-sequence limitings are introduced in Fig. 3 to handle asymmetrical faults. Though the virtual negative-sequence resistance has been used to improve power-sharing under normal conditions [34], it fails to consider asymmetrical faults. In the negative- and zero-sequence limitings, the targeted current components are extracted by

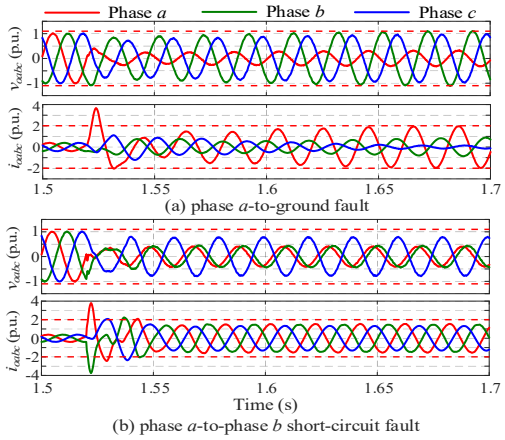


Fig. 4. Simulation results of the inverter voltages and currents using PNZSL-SEPFC with k_{np} = 0.2pu, k_{zp} = 0.6p.u. under two asymmetrical faults.

second-order generalized integrators (*SOGI*s) to generate the associated sequence voltage drops as

$$\begin{cases} \mathbf{y}_{ndq} = k_{np} \cdot SOGI_n(s) \cdot \mathbf{i}_{odq} \\ y_z = k_{zp} \cdot SOGI_z(s) \cdot i_{oz} \end{cases} \tag{2}$$

here $\mathbf{y}_{ndq}$ = [y_{nd}, y_{nq}] is the negative-sequence voltage drop vector, and y_z the zero-sequence voltage drop. ω_{nc} and ω_{zc} are bandwidths of $SOGI_n(s)$ and $SOGI_z(s)$, respectively. With proper values of the virtual negative-sequence resistance k_{np} and zero-sequence resistance k_{zp}, the PNZSL-SEPFC can effectively suppress negative- and zero-sequence currents and maintain the healthy phase voltage under asymmetrical faults.

C. Issues of the PNZSL-SEPFC with constant virtual sequence resistances

Based on the Fig. 1 system and parameters in Table I, the PNZSL-SPEFC with constant k_{np} and k_{zp} is examined under asymmetrical faults with fault impedance Z_f=0.05p.u. and grid short-circuit ratio (*SCR*) *SCR*=5. As shown by the results in Fig. 4(a), the faulty phase current is limited quickly, and the healthy phase voltage amplitudes are within the normal range of 0.88~1.1p.u. [35], where $V_b \approx$ 1.06p.u. and $V_c \approx$ 0.93p.u. in the steady-state. Therefore, the PNZSL-SEPFC can enable the inverter to meet the desired FRT requirements under this single-line to ground (*SLG*) fault. If it becomes a line-to-line (*LL*) fault, Fig. 4(b) illustrates that the strategy can still limit the faulty phase currents; however, the healthy phase voltage is only $V_c \approx$ 0.78p.u., much lower than the normal range. A straightforward idea to maintain the healthy phase voltage is increasing k_{np} and k_{zp}. Nevertheless, the inverter may instead experience overvoltage if k_{np} and k_{zp} are large and the grid *SCR* and fault conditions vary. Thus, constant k_{np} and k_{zp} cannot handle complicated grid and fault conditions, and how to design them appropriately will be of vital importance for making the PNZSL-SPEFC attractive to practical applications.

III. In-depth Analysis of the PNZSL-SEPFC under Various Conditions

As illustrated by Fig. 4, the PNZSL-SEPFC with constant k_{np} and k_{zp} fails to achieve the desired FRT performance under complicated grid and fault conditions. Besides, since the proposed scheme indirectly realizes overcurrent protection, it is also necessary to investigate to what extent the output current is limited under different scenarios. Therefore, a theoretical fault model of the inverter with the PNZSL-SEPFC is developed to analyze the influence of grid *SCR*, fault types, and fault impedances on the inverter voltages and currents.

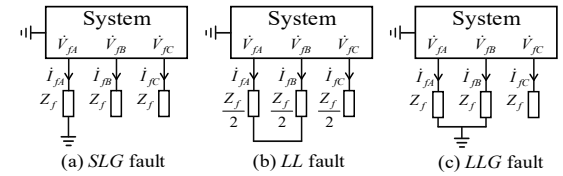


Fig. 5. Representation of a system under different asymmetrical faults.

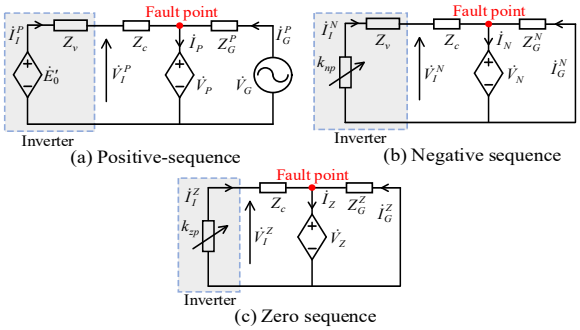


Fig. 6. Sequence networks of the faulty system.

A. The inverter sequence voltages and currents

The inverter three-phase output voltages and currents can be expressed by sequence components in the local *dq* frame and zero-sequence domain as

$$\begin{cases} \mathbf{v}_{odq} = V_I^P e^{j\varphi_v^P} + V_I^N e^{-j\left(2\theta+\varphi_v^N\right)} \\ \mathbf{i}_{odq} = I_I^P e^{j\varphi_c^P} + I_I^N e^{-j\left(2\theta+\varphi_c^N\right)} \end{cases}, \begin{cases} v_{oz} = V_I^Z \cos\left(\theta+\varphi_v^Z\right) \\ i_{oz} = I_I^Z \cos\left(\theta+\varphi_c^Z\right) \end{cases} \tag{3}$$

where $\mathbf{v}_{odq}$ and $\mathbf{i}_{odq}$ are voltage and current vectors in the *dq* frame, v_{oz} and i_{oz} are the zero-sequence voltage and current. V_I^{PNZ} and I_I^{PNZ} are amplitudes of positive, negative, and zero sequence voltages and currents, and their phase angles are φ_v^{PNZ} and φ_c^{PNZ}. The inverter's phase θ is chosen as the reference. As shown in (3), the negative-sequence components appear as 2nd-order oscillations, while the zero-sequence components are of the fundamental frequency. Typically, voltage settings of the negative- and zero-sequence are zero in the primary controller. Then, according to Fig. 3, the voltage references are

$$\begin{bmatrix} v_{dref} \\ v_{qref} \\ v_{zref} \end{bmatrix} \approx \begin{bmatrix} E_0 - y_{pd} \\ -y_{pq} \\ 0 \end{bmatrix} - \begin{bmatrix} R_v & -X_v & 0 \\ X_v & R_v & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_I^P \cos\left(\varphi_c^P\right) \\ I_I^P \sin\left(\varphi_c^P\right) \\ 0 \end{bmatrix} - \begin{bmatrix} k_{np}+R_v & -X_v & 0 \\ X_v & k_{np}+R_v & 0 \\ 0 & 0 & k_{zp} \end{bmatrix} \begin{bmatrix} I_I^N \cos\left(2\theta+\varphi_c^N\right) \\ -I_I^N \sin\left(2\theta+\varphi_c^N\right) \\ I_I^Z \cos\left(\theta+\varphi_c^N\right) \end{bmatrix} \tag{4}$$

here the *Q*-*V* droop is ignored. Due to the LPF's attenuation, y_{pd} and y_{qd} are nearly dc components and only modify the

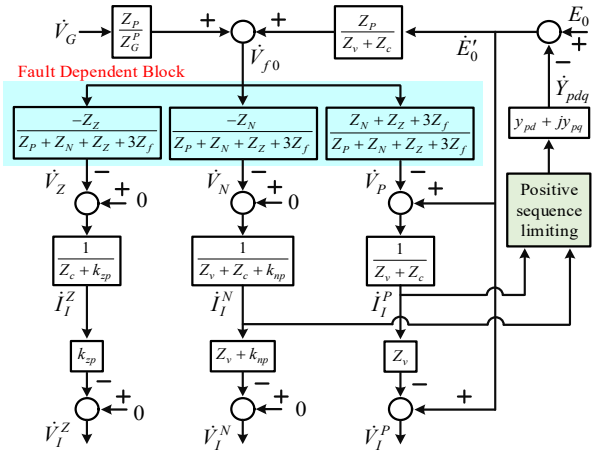


Fig. 7. Calculation diagram of the inverter sequence voltages and currents when the PCC phase *a* experiences an *SLG* fault.

positive-sequence voltage. Assuming that the inner loop controllers are ideal, the inverter voltages are equal to the references and can be expressed in the phasor form as

$$\dot{V}_I^P = \dot{E}_0' - Z_v \dot{I}_I^P,\ \dot{V}_I^N = -\left(Z_v + k_{np}\right)\dot{I}_I^N,\ \dot{V}_I^Z = -k_{zp}\dot{I}_I^Z \quad (5)$$

here the modified internal voltage is $\dot{E}_0' = (E_0 - y_{pd}) - jy_{pq}$, and the decoupling virtual impedance $Z_v = R_v + jX_v$. It should be noted that high nonlinearities of the positive-sequence limiting and oscillations in i_{od} and i_{oq} hinder an explicit expression of $\dot{E}_0'$. Fortunately, this can be solved by a numerical solver *ode*4 (Runge-Kutta) in MATLAB.

B. Determination of the Inverter sequence voltages and currents under asymmetrical grid faults

In practical utility grids, asymmetrical faults usually include single-line to ground (*SLG*), line-to-line (*LL*), and two-line to ground (*LLG*), and Fig. 5 presents three faults for analysis. In order to obtain a general form, it is convenient to describe the faulty system using sequence networks as in Fig. 6 [36, 37]. The sequence voltages and currents of the fault point satisfy

$$\dot{V}_P = \dot{V}_{f0} - Z_P \dot{I}_P,\ \dot{V}_N = -Z_N \dot{I}_N,\ \dot{V}_Z = -Z_Z \dot{I}_Z \quad (6)$$

Z_P, Z_N, Z_Z are equivalent sequence impedances seen into the system from the fault point, and they are calculated as

$$Z_P = Z_G^P \| \left(Z_v + Z_c\right), Z_N = Z_G^N \| \left(Z_v + Z_c + k_{np}\right), Z_Z = Z_G^Z \| \left(Z_c + k_{zp}\right) \quad (7)$$

where Z_G^P, Z_G^N, and Z_G^Z are grid sequence impedances, and the equivalent voltage in the positive-sequence network is

$$\dot{V}_{f0} = \frac{Z_v + Z_c}{Z_G^P + Z_v + Z_c}\dot{V}_G + \frac{Z_G^P}{Z_G^P + Z_v + Z_c}\dot{E}_0' \quad (8)$$

Additionally, the fault point voltages and currents are also constrained by the following relationship [38]

$$SLG:\ \dot{I}_{fB} = \dot{I}_{fC} = 0, \dot{V}_{fA} = Z_f \dot{I}_{fA} \quad (9)$$

$$LL:\ \dot{I}_{fA} + \dot{I}_{fB} = 0, \dot{I}_{fC} = 0, \dot{V}_{fA} - \dot{V}_{fB} = Z_f \dot{I}_{fA} \quad (10)$$

$$LLG:\ \dot{I}_{fC} = 0, \dot{V}_{fA} = Z_f \dot{I}_{fA}, \dot{V}_{fB} = Z_f \dot{I}_{fB} \quad (11)$$

For a specific fault in Fig. 5, the inverter sequence components can be calculated using (5), (6), (8) and the associated constraints in (9), (10), or (11). Taking the *SLG* fault as an example, based on (5), (6), (8), and (9), the inverter sequence voltages and currents are calculated as in Fig. 7.

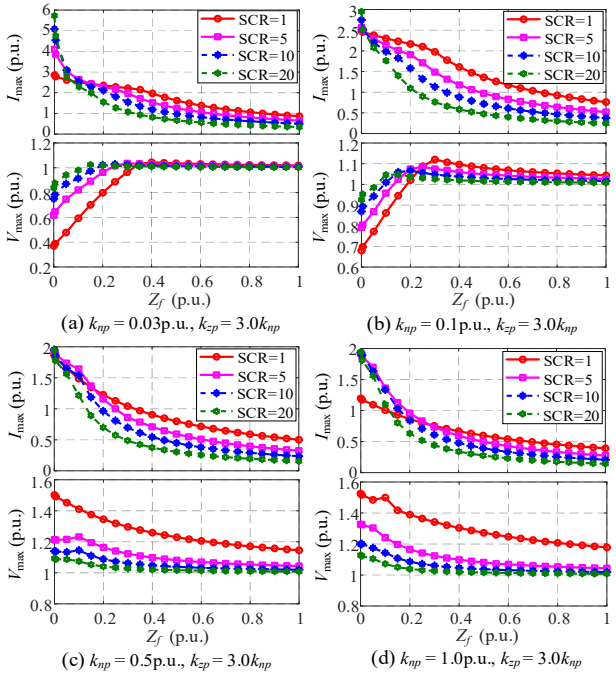


Fig. 8. The calculated maximum current and voltage magnitudes under an *SLG* fault with various *SCR*, Z_f ,and virtual sequence resistances.

C. Influence of k_{np} and k_{zp} on the maximum inverter voltage and current under complicated conditions

After obtaining sequence components, the inverter phase voltages and currents can be obtained as

$$X_a = X_P + X_N + X_Z, X_b = h^2 X_P + hX_N + X_Z, X_c = hX_P + h^2 X_N + X_Z \quad (12)$$

where X_{abc} represents three-phase voltages or currents and X_{PNZ} sequence components. The operators are $h = e^{j2\pi/3}$ and $h^2 = e^{j4\pi/3}$. In this work, we assume that $Z_G^P = Z_G^N = Z_G^Z$. The virtual zero-sequence resistance is chosen as k_{zp}=3.0k_{np} to get a virtual grounding resistance, seen into the inverter at its output terminal, equal to k_{np} for simplifying analysis. For the *SLG* fault in Fig. 5, the inverter's maximum phase voltage and current amplitudes are investigated under various k_{np}, grid *SCR*, and fault impedance Z_f. With the inverter parameters in Table I, the results are presented in Fig. 8.

As depicted in Fig. 8, if a small k_{np} is adopted under $Z_f \approx 0$, say k_{np}=0.03p.u. in Fig. 8(a), I_{max} is larger than 2.0p.u. regardless of the *SCR*; however, it becomes well constrained when k_{np} is increased to 0.5p.u. in Fig. 8(c), and over-limited in Fig. 8(d) under *SCR*=1. Once Z_f increases and the fault becomes less severe, I_{max} decreases gradually under the investigated grid conditions as expected. It is interesting to find that I_{max} varies more significantly when Z_f increases in a strong grid.

Meanwhile, the maximum voltage V_{max} also displays some interesting characteristics in Fig. 8. When k_{np} is small, as in Fig. 8(a) and (b), V_{max} is lower than 1.0p.u. under severe faults, and the weaker the grid, the larger the voltage drops. As soon as the fault becomes less critical and Z_f increases, V_{max} will increase first and then be clamped within the normal range in Fig. 8(a) and (b). On the contrary, if the PNZSL-SEPFC uses large k_{np} as

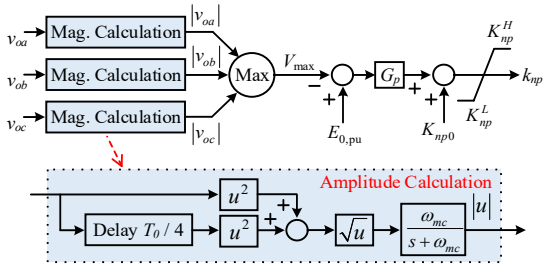


Fig. 9 Block diagram of the adaptive k_{np} scheme for PNZSL-SEPFC.

in Fig. 8(c) and (d), $V_{\max}$ tends to have the maximum at $Z_f \approx 0$ and decreases with an increasing Z_f. The weaker the grid, the higher the overvoltage under severe faults in Fig. 8(c) and (d), in which $V_{\max}$ can be around 1.5p.u. with a grid *SCR*=1.

Though Fig. 8 shows only the *SLG* fault results, $I_{\max}$ and $V_{\max}$ also present similar characteristics under *LL* and *LLG* faults, which are not presented here due to page limitations. The phenomena observed in Fig. 8 visually illustrate the influence of k_{np}, grid *SCR*, and fault impedance Z_f. The k_{np} imposes its impact by changing the inverter's negative- and zero-sequence impedances, grid *SCR* decides grid sequence impedances, while Z_f determines the level of sequence voltages and currents at the PCC. Therefore, with different k_{np} and grid *SCR*, the inverter will present different positive-sequence voltage levels and proportionally supply the negative- and zero-sequence currents according to the corresponding sequence impedance ratio between the inverter and grid. When Z_f becomes relatively large, it will dwarf the impact of equivalent negative- and zero-sequence impedances and make the positive-sequence voltage and current components dominant at the PCC. As a result, the inverter's $I_{\max}$ and $V_{\max}$ appear sensitive when these factors are varied. From the calculated results, some conclusions can be drawn as

(1) The PNZSL-SEPFC with constant k_{np} and k_{zp} fails to achieve the current limiting and overvoltage avoidance considering different fault types, Z_f, and grid *SCR*s.
(2) $I_{\max}$ generally reaches its peak under the solid fault and decreases as Z_f increases. If k_{np} and k_{zp} are higher than a specific value, $I_{\max}$ will be limited within an acceptable range regardless of fault types, Z_f, and *SCR*.
(3) $V_{\max}$ shows complicated characteristics, and it is difficult to predict when $V_{\max}$ reaches its lowest and peak values. However, $V_{\max}$ increases with k_{np} and k_{zp}, and varies widely in a weak grid with different Z_f.
(4) Solid faults in a strong grid are most challenging for limiting $I_{\max}$, while a weak grid is critical to $V_{\max}$.

IV. Further Enhancement with Adaptive Virtual Negative and Zero Sequence Resistances

As revealed in the previous simulation results and analysis, the PNZSL-SEPFC cannot achieve desirable performance with constant k_{np} and k_{zp}. Provided that $k_{zp} = 3.0k_{np}$ in this work, k_{np} should vary widely above a minimum value to limit the faulty phase current and maintain the healthy phase voltage concerning uncertain fault types, fault levels, and grid *SCR*s. Since a minimum value K_{np}^{L} can ensure the current limiting, k_{np} is designed to be adaptive to $V_{\max}$. When $V_{\max}$ is larger than a set level, k_{np} is reduced proportionally to avoid overvoltage, vice versa. Based on this idea, an adaptive k_{np} scheme in Fig. 9 is integrated into PNZSL-SEPFC. It can be written as

$$k_{np} = G_p\left(E_{0,\mathrm{pu}} - V_{\max}\right) + K_{np0} \tag{13}$$

here G_p is the proportional gain, $V_{\max}$ the maximum voltage amplitude, and the setting voltage level is equal to the droop voltage $E_{0,\mathrm{pu}}$. An offset K_{np0} is used to maintain k_{np} at a relatively high level under normal conditions and improve the inverter's dynamic performances at fault occurrences. By delaying a quarter of the fundamental period T_0, voltage amplitudes are easily calculated, as in Fig. 9. An LPF with cutoff frequency $\omega_{mc}=\omega_{pc}$ is to attenuate harmonics and smooth k_{np}. Therefore, a fast voltage calculation is not required. The G_p, K_{np0}, K_{np}^{L}, and K_{np}^{H} can be determined as the following steps.

Step 1: specify the desired range for the healthy phase voltage. According to [35], the allowable continuous voltage range of 0.88~1.10p.u. is adopted in this work.

Step 2: select a relatively high K_{np0} so that it is $k_{np} \approx K_{np0}$ to improve unbalanced load sharings under normal operations and the dynamic performance at fault occurrences. It may take some effort to find a proper K_{np0}. Here K_{np0}=1.0p.u. is utilized.

Step 3: determine the lower threshold K_{np}^{L}. Due to the complicated grid and fault conditions, a small K_{np}^{L} can result in large current limiting errors, while a large K_{np}^{L} may lead to unacceptable overvoltages under high impedance faults in a weak grid. Therefore, based on the fault analysis in Fig. 8, a tradeoff is made, and it is selected K_{np}^{L} = 0.1p.u. in this work.

Step 4: design k_{np} to reach the lower limit K_{np}^{L} when it is $V_{\max}$=1.10p.u. and the upper limit K_{np}^{H} at $V_{\max}$=0.88p.u., then

$$\begin{cases} G_p\left(E_{0,\mathrm{pu}} - 1.10\right) + K_{np0} = K_{np}^{L} \\ G_p\left(E_{0,\mathrm{pu}} - 0.88\right) + K_{np0} = K_{np}^{H} \end{cases} \tag{14}$$

By solving (14), one can obtain G_p= 9.0 and K_{np}^{H} = 2.08p.u.

V. Simulation Results

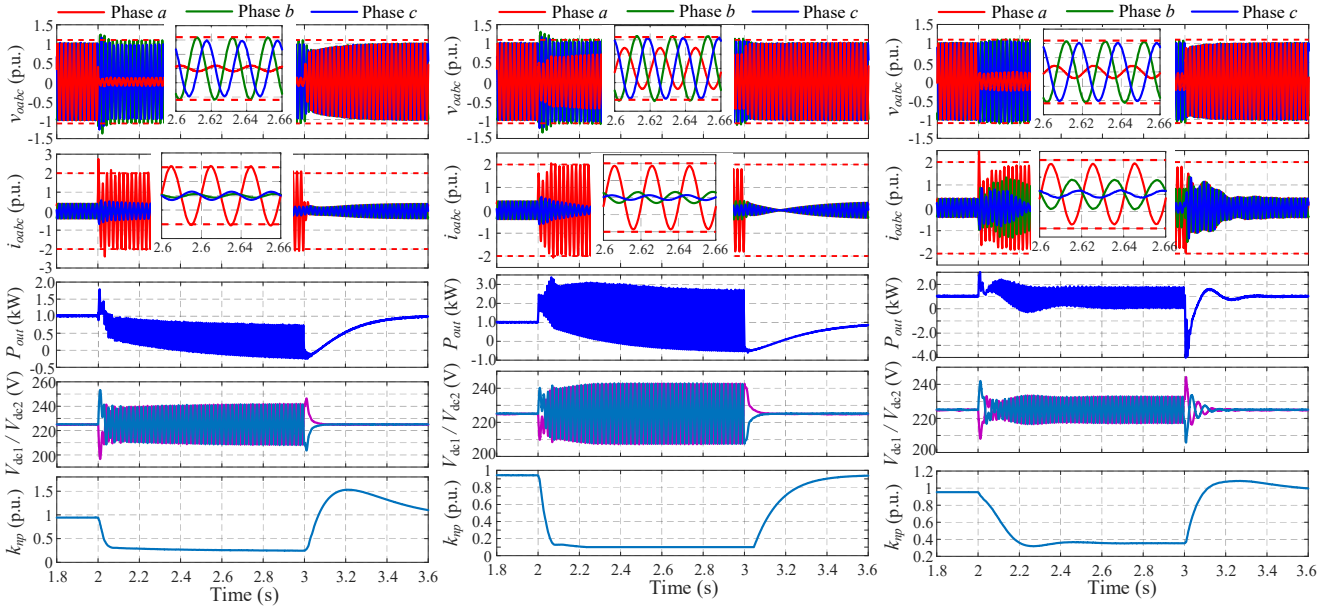
In order to examine the proposed PNZSL-SEPFC with adaptive k_{np}, the Fig. 1 system with the Table I parameters is developed in MATLAB/Simulink for simulation studies. There is no load connected at the PCC, to where grid faults are applied at t=2.0s and cleared after 1.0s.

A. Demonstration of the Proposed Strategy

Due to page limitation, only results are presented when the PCC phase *a* suffers from *SLG* faults in the following scenarios:

1) Case 1: weak grid *SCR*=1 and severe fault Z_f= 0.01p.u.
2) Case 2: weak grid *SCR*=1 and moderate fault Z_f = 0.3p.u.
3) Case 3: strong grid *SCR*=20 and severe fault Z_f=0.01p.u.
4) Case 4: constant k_{np}= 0.2p.u. ($k_{zp}=3k_{np}$) under Case 1.

Fig. 10(a) gives the inverter performance under Case 1. At the fault inception, one can find that the inverter experiences a short time transient overvoltages in the healthy phases and overcurrent in the faulty phase. The overvoltage peak is about 1.35p.u. in phase *b* and 1.28p.u. in phase *c*, and the overcurrent



(a) Case 1 scenario (b) Case 2 scenario (c) Case 3 scenario

Fig. 10. Simulation results of the inverter output voltages, currents, active power, and dc capacitor voltages with adaptive k_{np} under different case scenarios.

peak is about 2.62p.u. Fortunately, after a short transient of about a quarter of a cycle (5ms) following the fault inception, the proposed scheme becomes effective and constrains the faulty phase current and healthy phase voltage. During the fault, the healthy phase voltages are maintained with good power quality, and they are V_{ob}≈1.08p.u. and V_{oc}≈0.97p.u. Meanwhile, the faulty phase current is limited to the defined thresholds with an error of about 5%. The instantaneous active power of the inverter inevitably contains second-order ripples because of the negative- and zero-sequence components. The peak-to-peak value of the ripples can reach about 900W. On the dc-link, the capacitors also experience ripples with a peak-to-peak value of about 30V. Once the fault is cleared, the inverter recovers seamlessly without any fault detection.

If the *SLG* fault becomes less severe, as in Case 2, Fig. 10(b) shows that the inverter current is well limited within the defined range without transient overcurrent, but the overvoltage is still similar to that in Fig. 10(a). During the fault, k_{np} is adaptive and clamped to K_{np}^{L}, indirectly indicating the inverter $V_{\max}$. In the steady state, healthy phase voltages are V_{ob}≈1.13p.u. and V_{oc}≈1.06p.u. It is expected that V_{ob} will be lower than 1.1p.u. if K_{np}^{L} has a smaller value; however, the inverter may suffer from a little higher current limiting error in other grid conditions. The active power now has larger ripples with the peak-to-peak value of about 3000W because the faulty phase voltage is at a relatively high level, while the dc voltage ripples still have a peak-to-peak value of about 30V.

When the inverter operates with a strong grid in Case 3, Fig. 10(c) presents the inverter performance. It is found that both the inverter voltage and current are satisfactorily controlled within the allowable ranges with adaptive k_{np}. The healthy phase voltages are smooth at the fault inception and clearance. Under this case, the transient overcurrent peak is about 2.5p.u., smaller than that in Fig. 10(a). The inverter now delivers an average power of about 1000W, and the peak-to-peak of the

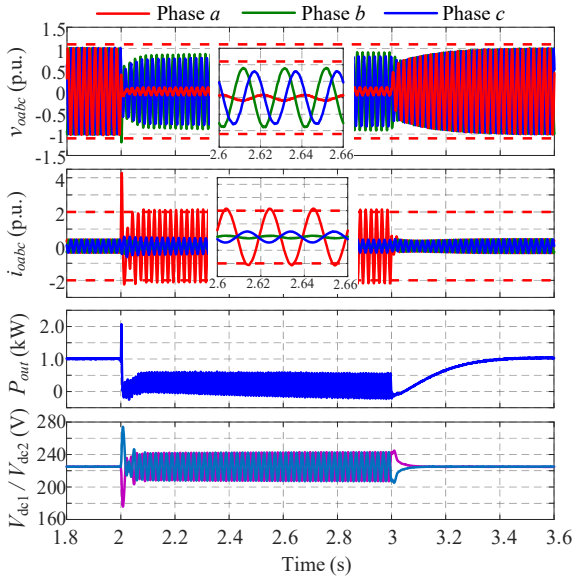
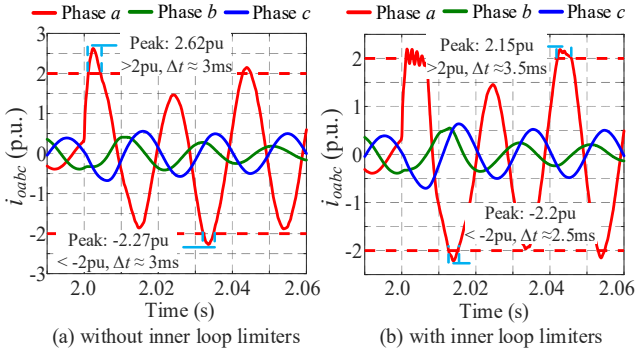
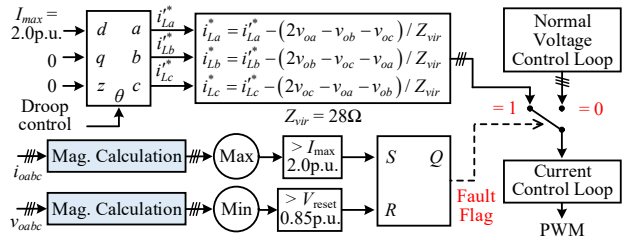


Fig. 11. Simulation results of the inverter under the Case 4 scenario

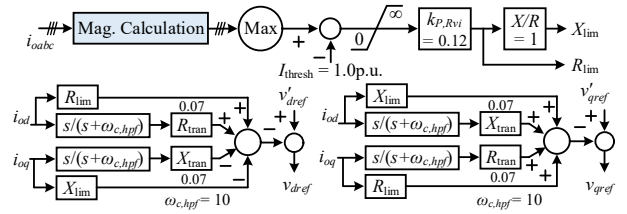


(a) without inner loop limiters (b) with inner loop limiters

Fig. 12. Inverter output currents under Case 1.



(a) the control switching and parallel virtual impedance-based strategy [20].



(b) the virtual impedance-based method [25]

Fig. 13. Existing current limiting methods for comparison study.

ripples is 1700W. The dc voltage ripples are about 15V, much smaller than the other two cases.

If k_{np} is 0.2p.u. and kept constant, as in Case 4, Fig. 11 shows that the transient overcurrent is up to 4.2p.u. and the dc capacitors also suffer from a high transient voltage (≈275V) at the fault inception. In the steady state, the faulty phase current is well constrained, but the healthy phase voltages are not desirable, where V_{ob}≈0.91p.u. and V_{oc}≈0.81p.u. The averaged active power is about 300W, and second-order ripples are with a peak-to-peak value of about 700W. The dc capacitors also experience voltage ripples with a peak-to-peak value of about 35V. On the other hand, by using adaptive k_{np}, the inverter achieves a smaller transient overcurrent and dc voltage at the fault occurrence and more satisfactory voltage levels in the healthy phases under the steady-state condition, as previously demonstrated in Fig. 10(a).

One may have noted that the faulty phase current exceeds the defined thresholds (±2.0p.u.) in Fig. 10(a) and (b) during the short transient following fault occurrences. This is an expected deficiency of the PNZSL-SEPFC because it is designed to modify voltage references for the current limiting. The low-pass filters in the positive-sequence limiting and limited voltage control bandwidth are also the causes. Fortunately, the deficiency can be solved easily using inner loop instantaneous limiters to constrain current references during the fault transient [10]. Fig. 12 presents results with and without the inner loop instantaneous limiters. The limiters have a threshold of ±1.25I_{max} (±2.5p.u.), slightly higher than I_{max} to avoid interfering with the PNZSL-SEPFC. Fig. 12(a) shows two noticeable peaks exceeding the defined range, and durations are about 3.0ms when the inner loop limiters are not used. On the other hand, in Fig. 12(b), the inner loop instantaneous limiter is active to suppress the transient faulty phase current, and after about a quarter of a cycle (5ms), the PNZSL-SEPFC becomes responsible for constraining the faulty phase current.

Therefore, it can be concluded that the PNZSL-SEPFC with adaptive k_{np} can enable the inverter to operate safely under the *SLG* faults without degrading the healthy phase power supply

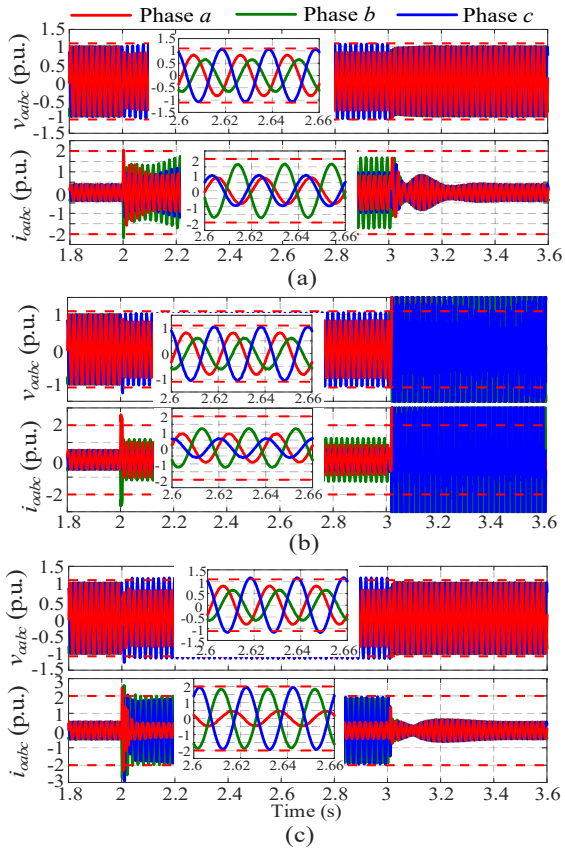


Fig. 14. Simulation results of the inverter under phase-*a*-to-phase-*b* short-circuit fault with Z_f = 0.1p.u. and *SCR* = 20. (a) the proposed PNZSL-SEPFC with adaptive k_{np}, (b) the control switching and parallel virtual impedance-based strategy from [20], (c) the virtual impedance-based method of [25].

after about the first quarter of a cycle following fault occurrence. Though there are minor limiting errors in the faulty phase current and a healthy phase voltage, the errors will become smaller if the grid *SCR* >1.0. Simulation results under *LL* and *LLG* faults with various Z_f and grid *SCR*, which are not presented here, can further prove the feasibility.

B. Comparison Study

Here, the proposed PNZSL-SEPFC with adaptive k_{np} strategy is compared with two well-received methods in [20] and [25], as shown in Fig. 13. In Fig. 13(a), phase voltage and current amplitudes are calculated to detect faults and reset the control scheme after fault clearance. Based on the parameters in Table I, the parallel virtual impedance should be Z_{vir} < $\sqrt{3}$ V_{dc}/I_{max} = 31.8Ω [20]. Hence, Z_{vir} = 28Ω is chosen here. As for the virtual impedance-based method in Fig. 13(b), the maximum phase current amplitude is used to generate an extra virtual impedance to limit the output current. The voltage and current control is implemented with *PR* controllers in the *abc* frame, and inner loop instantaneous limiters with a threshold ±1.25I_{max} are applied to constrain transient current references.

When the PCC suffers from an *LL* short-circuit fault with Z_f = 0.1p.u. in a grid with *SCR* = 20, the inverter performance is shown in Fig. 14. The results show that all three strategies can successfully limit the inverter currents and maintain the healthy phase voltage with good quality during the fault. However, the

fault current i_{ob} in Fig. 14(b) is significantly smaller than the others shown in Fig. 14 (a) and (c), and would therefore have a lower FRT support; whereas, the healthy phase current i_{oc} in Fig. 14(c) is significantly larger than the others shown in Fig. 14 (a) and (b), leading to voltage violation in the healthy phase. Once the fault is cleared, Fig. 14(b) shows that the control switching and parallel virtual impedance-based method can induce instability because the voltage control loop is broken and suffers from windups during the fault, while the proposed strategy and virtual impedance-based method can ensure the inverter has a smooth recovery.

Simulations with different Z_f and *SCR* have also been done. When the *LL* fault is less severe with Z_f = 0.3p.u., the control switching and parallel virtual impedance-based strategy is inactive because $V_{\min}$ > 0.85p.u. and the fault flag is 0. As a result, the inner loop limiters are saturated and the inverter presents distorted voltages and currents. On the other hand, the virtual impedance-based method can make the inverter suffer from distortions if the fault occurs in a grid with *SCR* = 1.0. Meanwhile, the proposed strategy is robust against varying Z_f and *SCR* and guarantees a proper current limiting and voltage quality.

VI. Experimental Verifications

To further verify the PNZSL-SEPFC with adaptive k_{np}, an experimental platform in Fig. 15 is developed. It has a similar topology as in Fig. 1, whereas an isolated transformer is to step down the real-life utility voltage. With limited components, the equivalent grid inductance is constructed to be L_G=15mH and resistance r_G=5Ω, making the grid *SCR* ≈ 1.9. The inverter is built using a CREE MOSFET module with the driver board CGD15FB45P1. An OP4510 is adopted as a rapid control prototyping (RCP) system to realize the control strategies. In the experiment, one of the OP4510 CPUs (Intel Xeon E3, 4 cores, 3.5GHz) is assigned to implement the inverter control

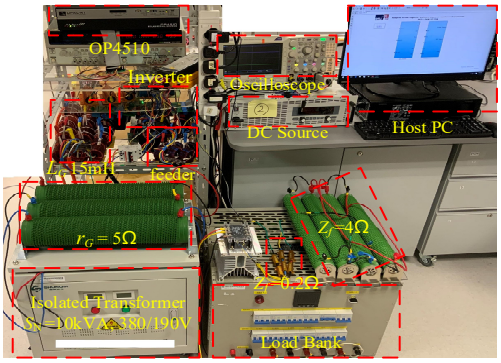
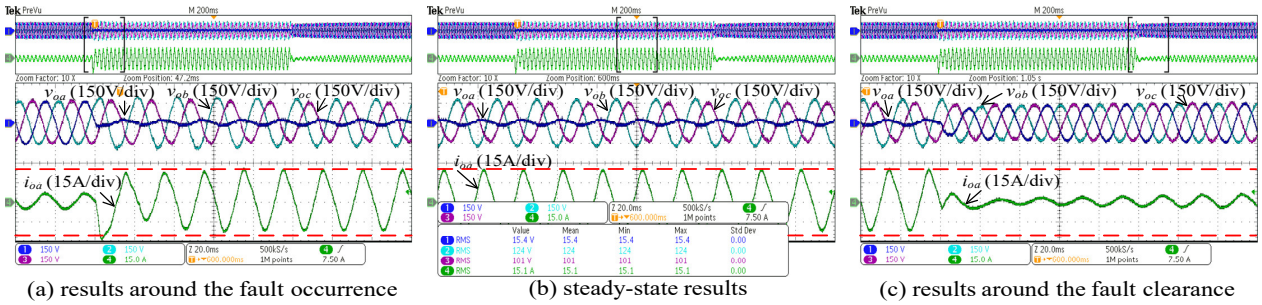


Fig. 15. The experimental platform.

algorithm and generate PWM signals with an execution time of about 3.0us. An Elektro Automatik DC source supplies power to the inverter. The current controller's proportional gain is k_{pc} =7.2, while the other parameters are the same as in Table I. In the experiments, there is a linear load of *P*=1.0kW and *Q*=0.5kVar. Grid faults are applied to the PCC and last for 1.0s.

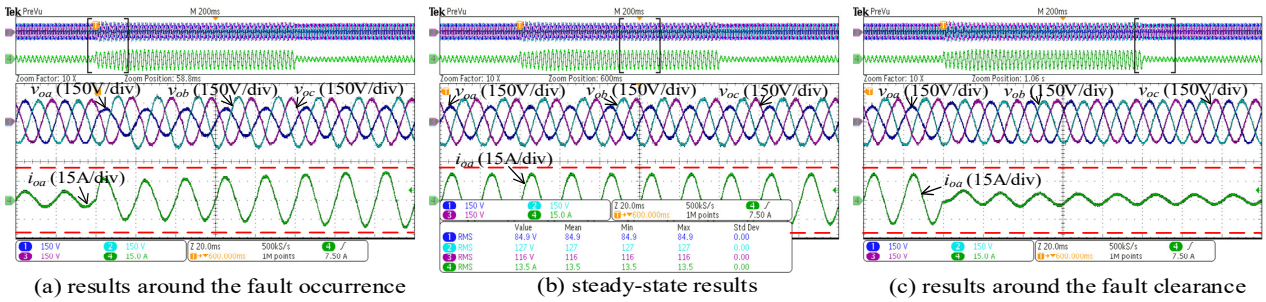
A. Experiments with SLG faults

Fig. 16 presents waveforms of the inverter output voltages and faulty phase current when the PCC phase *a* suffers from a severe *SLG* fault. As shown in Fig. 16(a), the faulty phase voltage v_{oa} drops sharply at the fault occurrence, and the current i_{oa} is well constrained after a short transient. When the fault reaches a steady state, as in Fig. 16(b), the healthy phase voltages are maintained with good waveform qualities, in which THDs of v_{ob} and v_{oc} are about 2% and 3.2%, respectively. The RMS value of v_{ob} is 124V (1.07p.u.), while that of v_{oc} is 101V (0.87p.u.), a little lower than the defined threshold (0.88p.u.). From the recorded data, k_{np} is adaptive to around 0.39p.u. during the fault. Once the fault is cleared, one can find in Fig. 16(c) that the inverter voltages and current are smoothly



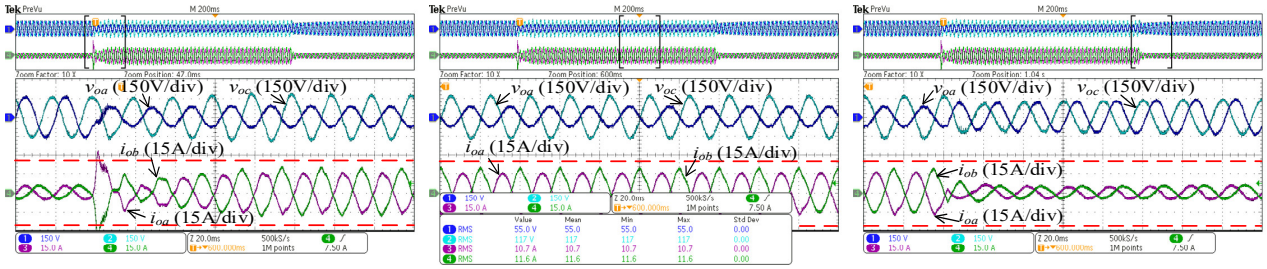
(a) results around the fault occurrence (b) steady-state results (c) results around the fault clearance

Fig. 16. Experimental results when the PCC phase *a* experiences a severe *SLG* fault with Z_f= 0.2Ω (0.015p.u.).



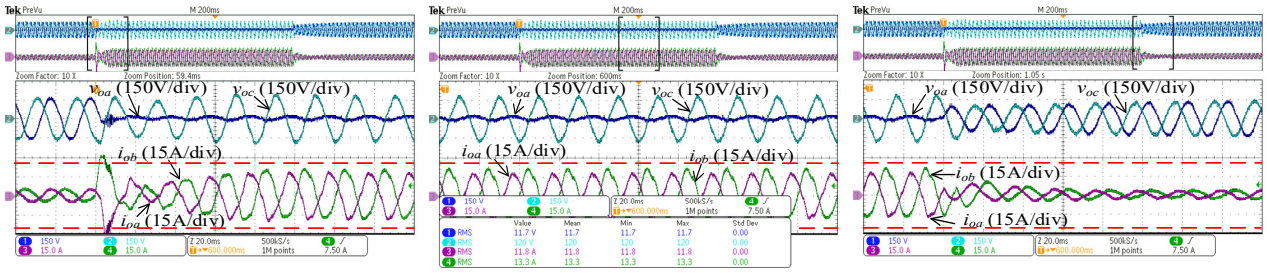
(a) results around the fault occurrence (b) steady-state results (c) results around the fault clearance

Fig. 17. Experimental results when the PCC phase *a* experiences a moderate *SLG* fault with Z_f= 4.0Ω (0.3p.u.).



(a) results around the fault occurrence (b) steady-state results (c) results around the fault clearance

Fig. 18. Experimental results when the PCC phase *a* and phase *b* experience a severe *LL* fault with Z_f= 0.2Ω (0.015p.u.).



(a) results around the fault occurrence (b) steady-state results (c) results around the fault clearance

Fig. 19. Experimental results when the PCC phase *a* and phase *b* experience a severe *LLG* fault with Z_f= 0.2Ω (0.015p.u.).

back to the pre-fault condition in 6~7 cycles.

When the *SLG* fault impedance becomes Z_f=4.0Ω (0.3p.u.), Fig. 17 shows the inverter performance. In Fig. 17(a), there is not transient overcurrent at the fault inception, and the voltages are smoothly transitioned to the faulty condition. In the steady state in Fig. 17(b), the faulty phase current i_{oa} is well limited within the defined range. The RMS values of v_{ob} and v_{oc} are 127V(1.095p.u.) and 116V(1.0p.u.), staying within the defined range. The k_{np} is now about 0.137p.u. Furthermore, THDs of v_{ob} and v_{oc} are respectively around 1.9% and 2.2%, suggesting good power qualities of the healthy phases. If the fault is cleared in Fig. 17(c), the inverter recovers autonomously in about 2 cycles.

B. Experiments with severe LL and LLG faults

If the PCC suffers from a severe *LL* fault between phase *a* and phase *b*, Fig. 18 illustrates the inverter performance. At the fault occurrence in Fig. 18(a), the faulty phase currents experience a transient overcurrent as expected, and the peak can reach about 33A (2.7p.u.) in phase *a*. The duration exceeding the defined range is about 5.0ms, and then the inverter can constrain the fault currents effectively. When it reaches a steady-state point in Fig. 18(b), the healthy phase voltage v_{oc} has an RMS value of 117V (1.01p.u.) and a THD ≈ 2.8%, and the RMS value of the faulty phase voltage v_{oa} is 55V (0.47p.u.). Once the fault is cleared, Fig. 18(c) shows that the inverter voltages and currents are able to recover quickly without noticeable transients.

Fig. 19 gives the experimental results under a severe *LLG* fault at the PCC. In Fig. 19(a), it can see that the inverter voltages and currents experience a short transient after the fault occurrence. The faulty phase voltage v_{oa} drops sharply and suffers some high-frequency ripples, and the faulty phase currents i_{oa} and i_{ob} are similar to that under the *LL* fault in Fig. 18(a). During the steady-state condition, Fig. 19(b) shows that the RMS values of the healthy phase voltage v_{oc} and the faulty phase voltage v_{oa} are 120V (1.03p.u.) and 11.7V (0.1p.u.), respectively. The THD of v_{oc} is about 3.8%, a little higher than under other fault types. After the fault is cleared, the inverter regains the normal operation smoothly, as shown in Fig. 19(c).

TABLE I
PRIMARY PARAMETERS OF THE SYSTEM IN FIG. 1

Symbol	Description	Values
S_N	Inverter rated power and power base	3kVA
V_{base}	Voltage amplitude base	164V
V_{dc}	DC voltage	450V
C_{dc1} / C_{dc2}	DC capacitors	2000uF
f_{sw}	Inverter switching frequency	28kHz
f_{ss}	Signal sampling frequency	100kHz
ω_{base}	Rated angular frequency	100π rad/s
$E_{0,pu}$	Droop setting voltage	1.0p.u.
$\omega_{N,pu}$	Droop setting angular frequency	1.0pu
m / n	Droop gains	0.01/0.05pu
P_{set}	Active power setting	0.5pu
R_v, X_v	Decoupling Virtual impedance	0.03pu
L_f / C_f	LC filter inductance and capacitance	0.05/0.13pu
L_c / r_c	Line inductance and resistance	0.035/0.01pu
L_n / r_n	Netural inductance and resistance	0.01/0.23pu
k_{pv} / k_{iv}	Voltage controller parameters	0.16/80Ω^{-1}
k_{pc} / k_{ic}	Current controller parameters	10/40Ω
F	Output current feedforward gain	0.6
k_{oq}	Stability enhanced gain	0.1
k_{pp}, ω_{pc}	Parameters of Positive-sequence limiting	25, 6.7rad/s
I_{dH}, I_{qH}	Upper current thresholds	I_{Nmax} / $\sqrt{2}$
I_{dL}, I_{qL}	Lower current thresholds	-I_{Nmax} / $\sqrt{2}$
ω_{nc}, ω_{zc}	Negative and zero sequence bandwidths	157rad/s

VII. CONCLUSIONS

An adaptive fault ride-through (FRT) scheme is proposed in this paper for three-phase four-wire (3P4W) droop-controlled inverters to ensure their fundamental FRT capabilities during grid faults. As demonstrated in simulations and hardware

experiments, the proposed FRT scheme can allow the inverter to ride through asymmetrical faults, limit the faulty phase current, and continue the power supply in the healthy phase(s). The adaptive virtual negative- and zero-sequence resistances of the scheme also enable the inverter to handle complicated grid and fault conditions with small current limiting and voltage supporting errors. It is found that the current limiting error is about 5% under a severe single-line-to ground (*SLG*) fault with a fault impedance Z_f = 0.01p.u. and grid short-circuit ratio (*SCR*) in the range of 1 to 20. Meanwhile, the healthy phase voltage can also maintain in the allowable range of 0.88~1.1p.u. with THD below 3.8% during various asymmetrical fault types and impedances. In addition, the stronger the grid, the better FRT performance of the proposed scheme would be. Comparison studies with two existing methods have further demonstrated the superior performance of the proposed strategy. In short, GFM inverters equipped with the proposed scheme are promising to allow distributed generation units to operate safely and stably with good voltage supporting in future inverter-dominant systems under various grid faults and *SCR*s, and more advanced auxiliary FRT functionalities are being incorporated in our ongoing work.

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