

# Opportunities and challenges of 2D materials in back-end-of-line interconnect scaling <sup>EP</sup>

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## ABSTRACT

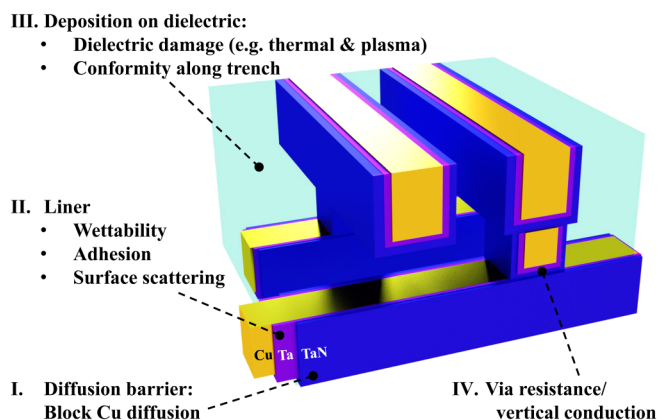
As the challenges in continued scaling of the integrated circuit technology escalate every generation, there is an urgent need to find viable solutions for both the front-end-of-line (transistors) and the back-end-of-line (interconnects). For the interconnect technology, it is crucial to replace the conventional barrier and liner with much thinner alternatives so that the current driving capability of the interconnects can be maintained or even improved. Due to the inherent atomically thin body thicknesses, 2D materials have recently been proposed and explored as Cu diffusion barrier alternatives. In this Perspective article, a variety of 2D materials that have been studied, ranging from graphene, h-BN, MoS<sub>2</sub>, WSe<sub>2</sub> to TaS<sub>2</sub>, will be reviewed. Their potentials will be evaluated based on several criteria, including fundamental material properties as well as the feasibility for technology integration. Using TaS<sub>2</sub> as an example, we demonstrate a large set of promising properties and point out that there remain challenges in the integration aspects with a few possible solutions waiting for validation. Applications of 2D materials for other functions in Cu interconnects and for different metal types will also be introduced, including electro-migration, cobalt interconnects, and radio-frequency transmission lines.

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## I. INTRODUCTION

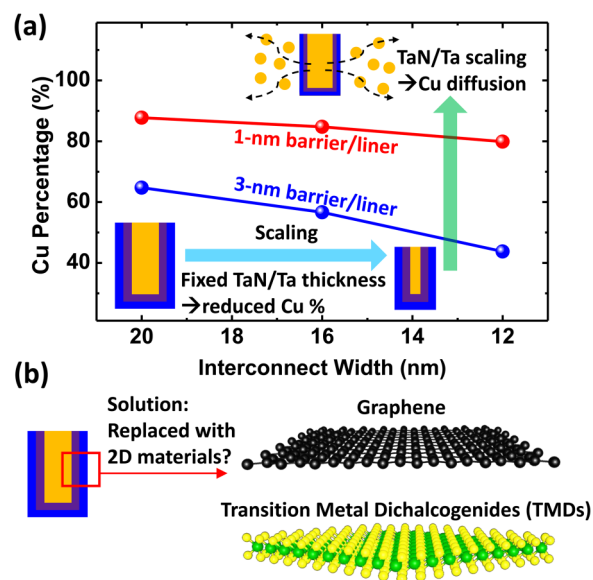
Copper (Cu) has been the material of choice for interconnects in today's IC chips for more than 20 years. Before the integration scheme for Cu interconnects was available, aluminum (Al) was used as metal interconnects. However, with increasing demands of lower resistivity and better electromigration endurance, Al was eventually replaced with Cu in the late 1990s, after many integration challenges had been solved. Overviews of the technology development can be found in Refs. 1 and 2. Although Cu offers the advantage of improving interconnect performance, its high diffusivity results in diffusion of Cu atoms/ions into the surrounding dielectric that isolates individual Cu interconnect wires, causing short-circuiting and chip failure.<sup>3–6</sup> To prevent this, TaN has been

adopted as the “diffusion barrier” to block Cu diffusion.<sup>7,8</sup> While possessing a decent diffusion barrier property, the adhesion between TaN and Cu is not ideal. Therefore, Ta has been introduced as the “liner” between Cu and TaN to improve the adhesion.<sup>7,8</sup> The schematic of basic interconnect structures is shown in Fig. 1, with two levels of Cu interconnects being connected through a “via.” Although the TaN/Ta/Cu stack gives an optimal diffusion barrier and liner properties, both TaN and Ta are much more resistive than Cu. Since the TaN/Ta stack occupies a certain percentage of the interconnect volume, the effective portion for high current conduction is less than the actual dimension of the interconnect. As a result, thinning down of the TaN/Ta layer must be carried out every few generations to reach the targeted current driving capability.



**FIG. 1.** Schematic of an interconnect structure with two metal levels and "via" connections. Qualifying criteria for both barrier and liner are listed. These aspects must be investigated before concluding any 2D material is qualified as a TaN/Ta alternative.

However, with the advent of 5-nm node and beyond, interconnect width can be as narrow as 20 nm or below. Meanwhile, the thickness of the TaN/Ta stack must be at least 3–4 nm<sup>9</sup> in order to provide a reasonable barrier and liner functions. Taking an interconnect with 20 nm in width and 40 nm in trench depth as an example, at least 35% of the entire interconnect cross-sectional area is occupied by a 3-nm thick TaN/Ta layer. Further scaling will lead to an even less percentage of Cu occupancy, largely suppressing the current conduction, as illustrated in Fig. 2(a). Even though scaling below 3 nm has been demonstrated by introducing atomic-layer deposition (ALD) TaN,<sup>10</sup> achieving a sub-nm barrier/liner will be necessary for advanced technology nodes, which is extremely challenging for these conventional materials due to their three-dimensional (3D) nature. On the other hand, two-dimensional (2D) materials, including graphene, hexagonal-boron-nitride (h-BN), and transition-metal-dichalcogenides (TMDs), can be atomically thin, e.g., ~0.3 nm for a single layer graphene.<sup>11</sup> Consequently, research has been carried out to evaluate 2D materials for their potential as a diffusion barrier replacement in the past few years, with the main idea illustrated in Fig. 2(b). Preliminary results have suggested that 2D materials have promising diffusion barrier properties,<sup>12–16</sup> which encourages further studies especially on the perspective of integrating these novel materials to the state-of-the-art technologies. For example, early studies of graphene grown at 1000 °C<sup>12–15</sup> provided the initial evidence that a single layer of carbon atoms is sufficient to block ion diffusion. However, the very high growth temperature is not compatible with the back-end-of-line (BEOL) technologies.<sup>17</sup> Besides, none of the early works discussed the liner properties of 2D materials, which could be an inherent weakness of these materials due to their van der Waals force interaction. Figure 1 summarizes the list of qualifying criteria for both barrier and liner as well as process-related issues to the surroundings materials/structures, all of which must be investigated before making decisions to integrate any of these new 2D materials to the technology. The framework of this

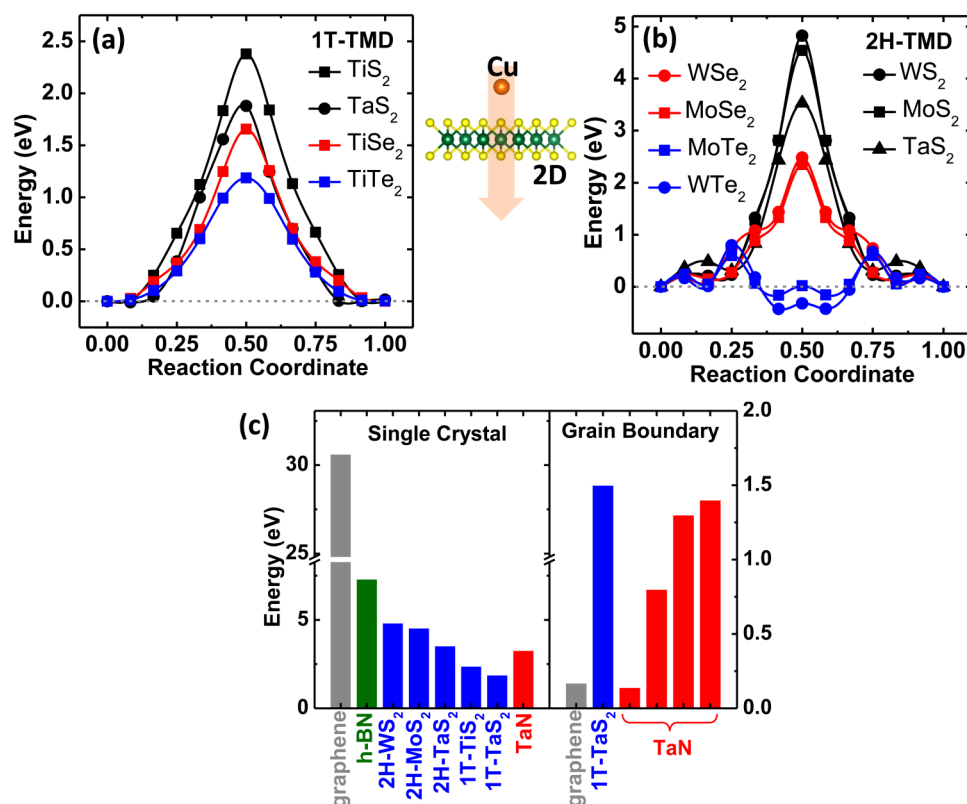


**FIG. 2.** (a) Challenges of interconnect scaling—less cross-sectional area is occupied by Cu with interconnect width scaling. Thus, the total line resistance will increase significantly. Proportionally reducing TaN/Ta thickness is not a viable solution since Cu diffusion will occur. (b) Replacing TaN/Ta with 2D materials can be a promising solution to continue the required interconnect scaling.

article will be based on the reviews and discussions of each criterion. Some of them have already been successfully demonstrated in 2D materials, while the others still remain challenging. Possible solutions to address these remaining challenges and future routes in realizing a 2D-material-based barrier/liner will also be extensively discussed throughout this article to inspire future studies and development.

## II. DIFFUSION BARRIER

In this section, we will provide an overview on both theoretical and experimental studies of diffusion barrier properties of 2D materials. First-principles density functional theory (DFT) calculations have been employed to investigate barrier energies of various 2D materials for blocking Cu diffusion and provide insight into the electronic structures of the interface between Cu and various 2D materials.<sup>18</sup> Details of the calculations are provided in Sec. VIII. Figures 3(a) and 3(b) show the lowest potential energy surfaces for Cu diffusing across various single-layer, perfect crystals of MX<sub>2</sub> TMDs with M = Mo, W, and Ta and X = S, Se, and Te. We show results for the two most stable phases 2H (space group P-6m2) and 1T (space group P-3m1). These calculations are performed on defect-free, perfect crystals that are hardly produced in real growth effort. In fact, most 2D materials in the literature and those available in the market show rather high defects and impurity densities as well as limited grain sizes. Grain boundaries have been established as the dominant diffusion paths in the case of TaN/Ta,<sup>19–21</sup> and they can certainly play important roles in the 2D materials of interest.<sup>22</sup> Nevertheless, exploring performance in ideal materials

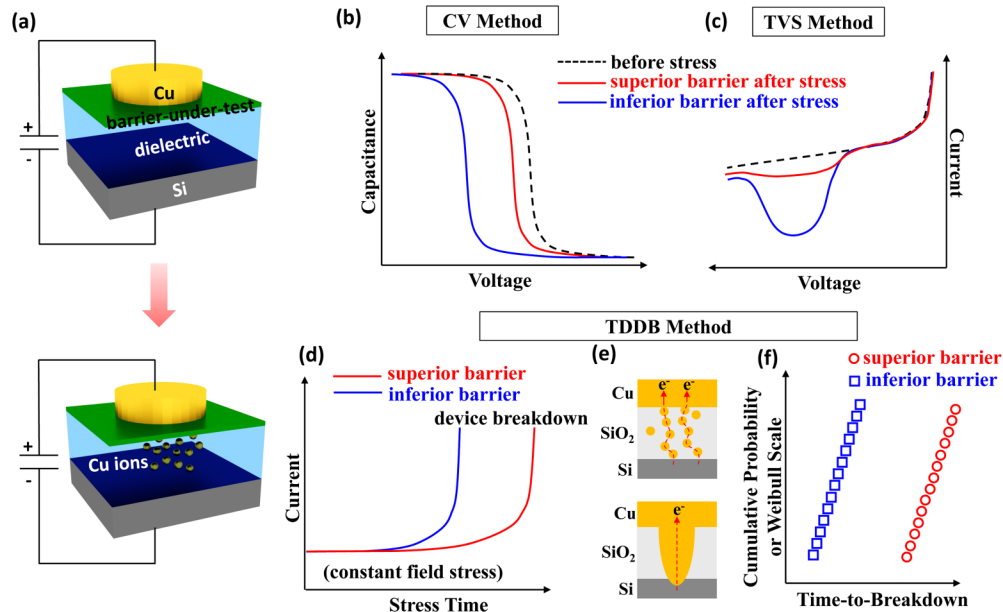


**FIG. 3.** DFT-calculated barrier energy for Cu diffusion across various single-layer, perfect crystals of (a) 1T and (b) 2H TMDs. (c) Summary of barrier energies of various single crystal materials and materials with grain boundaries, both from this work [h-BN and materials in (a) and (b)] and the literature (graphene, grain boundary diffusion of 1T-TaS<sub>2</sub>, and TaN). It can be clearly observed that the energies for diffusion across single crystals are much higher than those across grain boundaries. Some 2D materials show comparable or superior performance than TaN.

by calculations is essential for comparing intrinsic properties among different materials and identifying diffusion mechanisms. Our DFT results show that sulfides impose the highest barriers to diffusion with a reduction as we move to selenides and tellurides [Fig. 3(a)]. In fact, quite surprisingly, Cu prefers interstitial sites over surface sites for 2H tellurides.<sup>23</sup> Due to the great interest in TaS<sub>2</sub> for reasons to be addressed below, the material will be discussed in further detail to fully evaluate its potential. Figures 3(a) and 3(b) show that 2H-TaS<sub>2</sub> is preferable over 1T-TaS<sub>2</sub> because of its higher energy barrier. In addition, 2H-TaS<sub>2</sub> is easier to be produced by low-temperature syntheses.<sup>24</sup> Zhao *et al.*<sup>22</sup> have calculated a very high barrier energy of 30.6 eV in graphene [compared in the left panel of Fig. 3(c)], which promises a good diffusion barrier candidate that we will discuss in the paper. It is important to compare these new 2D materials with the conventional TaN barrier that has been thoroughly studied both theoretically and experimentally. Although the comparison of calculated energy barriers for 2D materials and experimentally extracted values for TaN is rather crude, it is helpful to gain some initial insights in order to quickly identify promising candidates. An experimental barrier energy extraction of 3.27 eV in single crystalline TaN by Wang *et al.*<sup>19</sup> is included in the same figure. Based on these comparisons, we conclude that graphene, h-BN, and some sulfides can be as good as or even better than single crystalline TaN in terms of barrier energy and can be considered for Cu diffusion barrier applications. As mentioned earlier, materials used in practice are normally polycrystalline with grain boundaries. The right panel of Fig. 3(c) displays an experimental extraction of a

reduced barrier energy range from 0.14 to 1.4 eV in TaN due to diffusion through grain boundaries.<sup>20,25,26</sup> The barrier energy for 1T-TaS<sub>2</sub> is calculated to be 1.5 eV,<sup>27</sup> higher than that of TaN. It would be interesting to have the same to be calculated for 2H-TaS<sub>2</sub> as well. Surprisingly, the value for graphene obtained from the same work by Zhao *et al.*<sup>22</sup> reduced significantly.

To experimentally test diffusion barrier properties, various approaches have been utilized, including thermal<sup>12–14</sup> and electrical<sup>15,16,28–31</sup> stress. This article will mainly focus on electrical tests, including three types, namely, capacitance–voltage (CV),<sup>16,28</sup> triangular voltage sweep (TVS),<sup>16,29</sup> and time-dependent dielectric breakdown (TDDB).<sup>15,30–37</sup> To study the intrinsic material properties, especially for novel materials, simple planar structures [Fig. 4(a)] are preferred since they exclude the extrinsic effects from an unoptimized process,<sup>33,35,36</sup> such as post-CMP (chemical–mechanical polishing, a process commonly used in BEOL) damage and contamination.<sup>38</sup> In contrast, inter-digitated damascene structures are more commonly adopted in the state-of-the-art technology to test the performance of the conventional TaN/Ta stack.<sup>39</sup> In general, for all of the electrical tests using either test structure, a constant electric field is applied across a capacitor like structure (Cu electrode/barrier/dielectric/electrode) for a certain duration to drive Cu ions into the dielectric. Note that the mass transport of Cu ions driven by the electric field is actually “Cu drift.” Nevertheless, we still denote it as “Cu diffusion” because of the conventional terminology used in the field. In CV and TVS measurements, the electric fields applied are generally small to



**FIG. 4.** (a) A planar capacitor structure for testing diffusion barrier properties. A constant electric field is applied to drive Cu ions into the dielectric. (b) Device characteristics before and after stressing using the CV method. Flatband voltages shift more in devices with inferior barriers. (c) Device characteristics before and after stressing using the TVS method. The current “bump” is more obvious in devices with inferior barriers. (d) Evolution of device current with stress time of devices with different barriers during the stressing in TDDB measurements. (e) Possible mechanisms of device breakdown caused by drifted Cu ions in the TDDB method. The top panel describes trap-assisted conduction, while the bottom illustrates copper silicide formation. (f) Statistical plot obtained from typical TDDB measurements. Each data point represents the time-to-breakdown ( $t_{BD}$ ) of a single device. A superior barrier results in data points located in the right side of the plot representing longer time to breakdown.

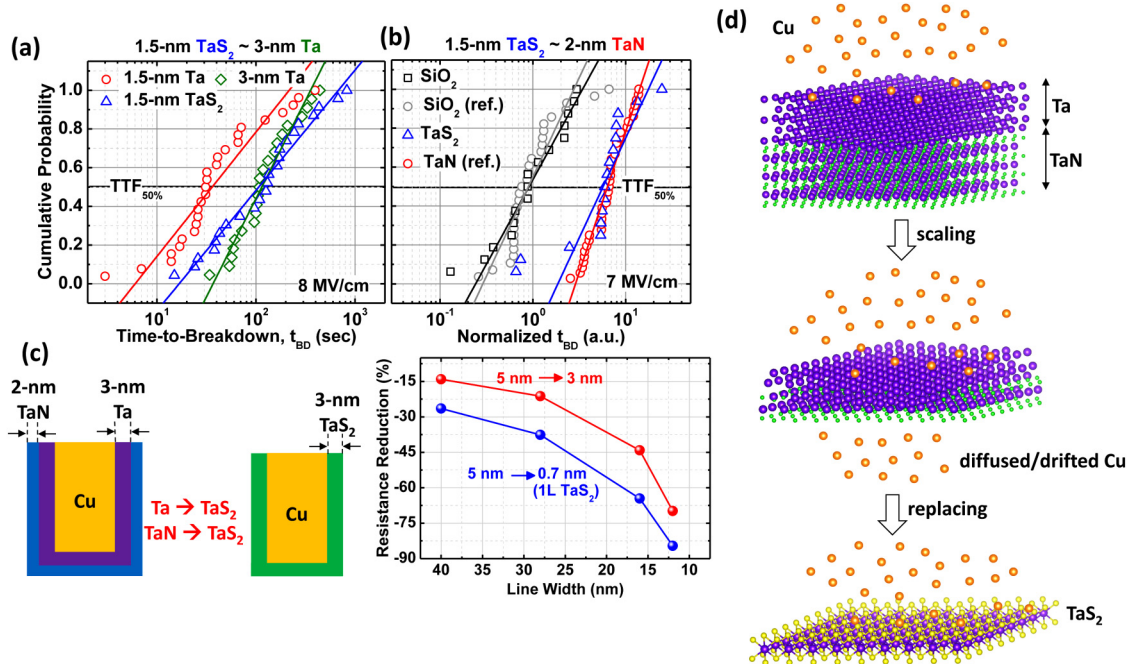
just drive a small amount of Cu ions into the dielectric, while the electric fields applied in TDDB measurements are large enough to cause device breakdown. In the CV method, after the constant field stressing, the flatband voltage will shift with the presence of fixed charges contributed by Cu ions in the dielectric. If a barrier is superior in blocking Cu diffusion, the flatband shift will be less or even negligible, as illustrated in Fig. 4(b). In the TVS method, after the stressing, a voltage sweeping from positive to negative is performed. A “bump” with increased current flow in the negative voltage regime can be observed, as depicted in Fig. 4(c), which is attributed to the presence of Cu ions. A better diffusion barrier will result in a smaller “bump.” Details of the mechanism are described in early literature.<sup>29</sup> The examples of using CV and TVS methods to test barrier properties of graphene can be found in the work of Mehta *et al.*<sup>16</sup>

TDDB measurement is the most widely used method in the industry since statistical information with solid theoretical backup, namely, the percolation theory,<sup>40–42</sup> can be obtained. Unlike the CV and TVS methods, where the “monitoring” of device characteristics is conducted after the stressing, the stressing and monitoring processes are performed simultaneously in TDDB measurements. As depicted in Fig. 4(d), the current is being monitored while the stressing is being applied. After a certain amount of time, a current surge will occur, indicating the device breakdown. The breakdown is attributed to the Cu ions present in the dielectric, which facilitate trap-assisted conduction<sup>34,37</sup> or even short, the electrodes on both sides by forming copper silicide in some extreme cases,<sup>12–14,30</sup> as

depicted in Fig. 4(e). If a barrier is superior, the time-to-breakdown ( $t_{BD}$ ) of devices using that barrier will be longer. The values of  $t_{BD}$  of multiple devices can be obtained and plotted in a statistical fashion shown in Fig. 4(f). When the y axis is presented as the cumulative probability (F), smaller/larger values of  $t_{BD}$  are assigned to have smaller/larger cumulative probabilities. In this way, a clear comparison between different barriers can be obtained. Sometimes, the y axis is presented in the Weibull scale [ $W = \ln(-\ln(1 - F))$ ]. A straight line in the Weibull plot normally indicates that the percolation theory can be applied, as is the case for a gate dielectric breakdown.<sup>40,41</sup> Even though some works claim that the percolation theory can also be applied to a Cu-induced breakdown,<sup>42</sup> we suggest using cumulative probability for the comparison to avoid mis-interpreting the underlying mechanisms of Cu diffusion through these novel materials.

An example of comparing diffusion properties of TaS<sub>2</sub>, Ta, and TaN is presented in Fig. 5. The time to breakdown tends indicate that 1.5-nm TaS<sub>2</sub> is as good as 3-nm Ta [Fig. 5(a)] and equivalent to 2-nm TaN<sup>15</sup> [Fig. 5(b)]. Together with the superior liner properties, which will be discussed in Sec. III, it is possible to replace the 5-nm TaN/Ta bilayer with 3-nm TaS<sub>2</sub>, based on experimentally already achieved TaS<sub>2</sub> performance. This barrier/liner scaling down can significantly increase the percentage of Cu occupancy and decrease the line resistance of ultra-scaled interconnects, as shown in Figs. 5(c) and 5(d). Further development in growth and improvement in material quality would make it possible to use





**FIG. 5.** Benchmarks of the diffusion barrier property of TaS<sub>2</sub> against (a) Ta and (b) TaN. The results show that 1.5-nm TaS<sub>2</sub> is as good as 3-nm Ta, while 1.5-nm TaS<sub>2</sub> performs similarly as 2-nm TaN. (c) Based on the results, conventional TaN/Ta can be replaced with TaS<sub>2</sub> with a thinner thickness, serving as both the liner and the barrier, which significantly reduces the total interconnect resistance. (d) The advantage of TaS<sub>2</sub> is further illustrated. Reproduced with permission from Lo *et al.*, Adv. Mater. **31**, 1902397 (2019). Copyright 2019 Wiley.

high quality, single-layer ( $\sim 0.7$  nm) TaS<sub>2</sub> as the barrier/liner layer. Note that the actual Ta to S ratio of this plasma-enhanced chemical vapor deposition (PECVD)-grown TaS<sub>x</sub> is 1:2.5.<sup>27</sup> However, for simplicity, it is referred as TaS<sub>2</sub> throughout this article. TDDB results of other 2D materials, including graphene, h-BN, and MoS<sub>2</sub>, can also be founded in other works.<sup>15,30</sup> Evaluations of diffusion barrier properties of 2D materials from experimental works in the literature are summarized in Table I.

In addition to the ability to block Cu diffusion, blocking oxygen diffusion is also an important function of the barrier layer.

Since low- $k$  dielectrics used in current BEOL technologies are porous, oxygen can easily diffuse through low- $k$  and oxidize Cu, hence degrading its performance.<sup>3</sup> Testing this property is more straightforward, and both theoretical<sup>43,44</sup> and experimental works<sup>45,46</sup> have shown that 2D materials are adept at preventing O<sub>2</sub> diffusion.

### III. LINER

The liner properties include mainly three aspects, namely, wettability, adhesion, and impact on Cu resistivity. Wettability is

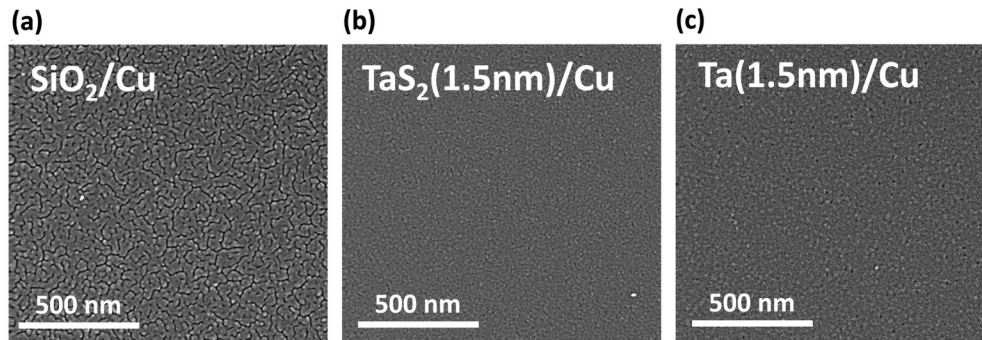
**TABLE I.** Summary of diffusion barrier and liner properties.

Material	Growth temperature	Diffusion barrier (all CVD-based)	Material	Method	Adhesion	Wettability	Scattering
Graphene	1000 °C	Good <sup>15</sup>	Graphene	CVD-based	Poor <sup>27</sup>	Poor <sup>a</sup>	Good (on Cu) <sup>54</sup>
	400 °C	Fair <sup>61</sup>		Exfoliated	N/A <sup>b</sup>	Poor <sup>a</sup>	N/A <sup>c</sup>
h-BN	1000 °C	Good <sup>30</sup>	h-BN	Exfoliated	N/A <sup>b</sup>	Poor <sup>30</sup>	N/A <sup>c</sup>
MoS <sub>2</sub>	850 °C	Good <sup>30</sup>	MoS <sub>2</sub>	Exfoliated	N/A <sup>b</sup>	Fair <sup>30</sup>	Good <sup>55</sup>
	400–450 °C	Fair <sup>31,62,63</sup>		CVD-based	Poor <sup>27</sup>	Fair <sup>31,63</sup>	Fair <sup>63</sup>
TaS <sub>2</sub>	400 °C	Good <sup>27</sup>	TaS <sub>2</sub>	CVD-based	Good <sup>27</sup>	Good <sup>27</sup>	Fair <sup>27</sup>
			WSe <sub>2</sub>	Exfoliated	N/A <sup>b</sup>	Fair <sup>a</sup>	Good <sup>55</sup>

<sup>a</sup>Tested by the author in Ref. 55.

<sup>b</sup>Adhesion tests must be conducted on large-area films.

<sup>c</sup>Cu wetting is poor even when the thickness is larger than  $\sim 20$  nm; hence, it is not possible to conduct a scattering test (requires  $< 15$  nm Cu).

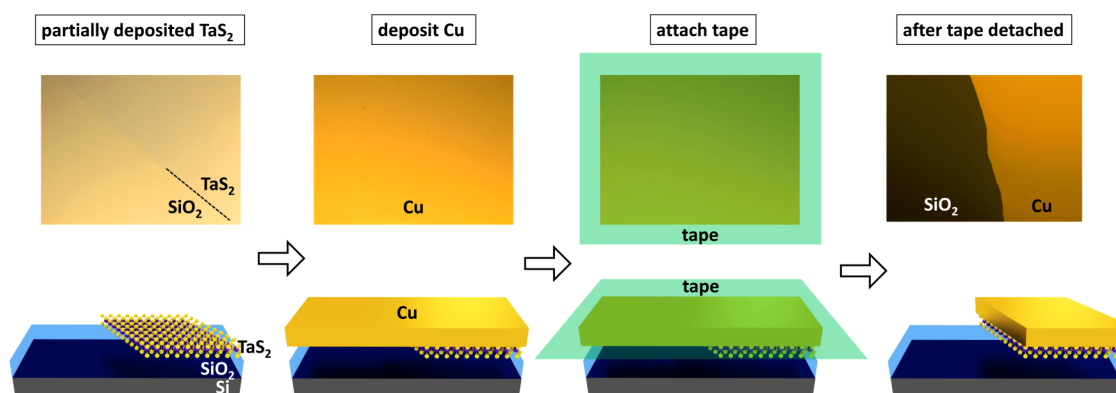


**FIG. 6.** Wettability tested by depositing ultra-thin Cu ( $\sim 10$  nm) on different surfaces. (a) A large number of cracks can be observed when Cu is directly deposited on  $\text{SiO}_2$ . (b) Ultra-thin Cu on 1.5 nm  $\text{TaS}_2$  and (c) 1.5 nm Ta have smooth morphologies. The results show that  $\text{TaS}_2$  can provide a good surface as Ta does for Cu seeding layers, which is important for the subsequent Cu electroplating. Reproduced with permission from Lo *et al.*, *Adv. Mater.* **31**, 1902397 (2019). Copyright 2019 Wiley.

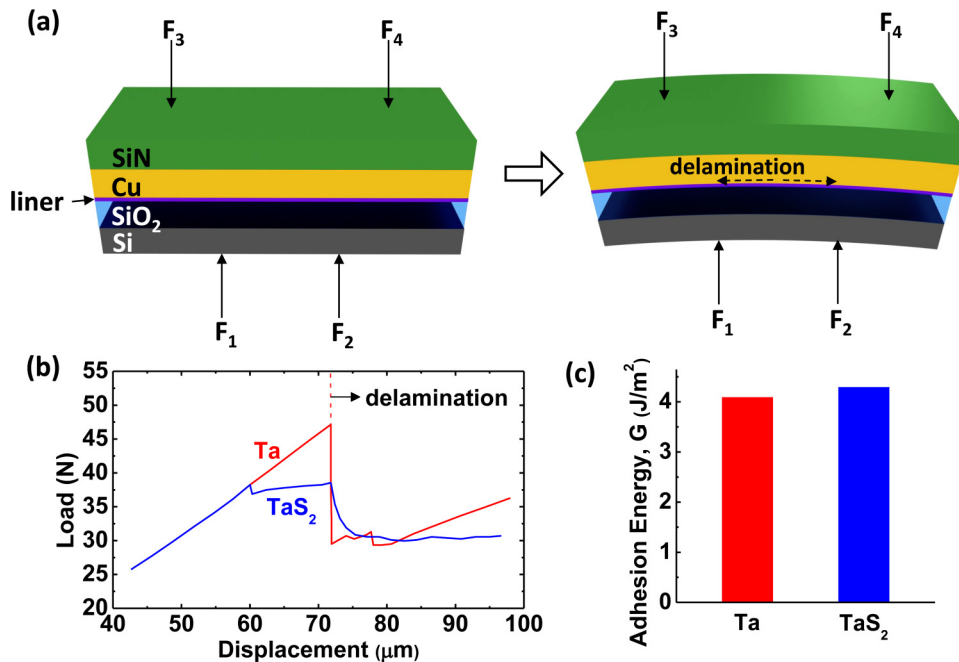
important for the deposition of a thin Cu seeding layer before electroplating the actual Cu interconnects.<sup>3</sup> The testing method is to deposit a thin layer of Cu on different surfaces to evaluate the wetting situation.<sup>27</sup> As shown in Fig. 6(a), when  $\sim 10$  nm Cu is deposited directly on a dielectric, a significant number of cracks are observed, indicating poor wettability. On the other hand, when a  $\text{TaS}_2$  layer is inserted between Cu and the dielectric [Fig. 6(b)], the morphology is significantly improved. It is actually as good as a standard Ta liner shown in Fig. 6(c), suggesting that  $\text{TaS}_2$  serves well as a liner in terms of wettability.

The adhesion property is the most critical factor to determine whether a 2D material can be adopted in the BEOL technology. The weak van der Waals layer-to-layer interaction in 2D materials make them unique in the way that individual layers can be exfoliated from the crystal even by a scotch tape, which was discovered and applied to the first graphene work. However, this weak interaction is not desired between 2D materials and other materials that they need to interface with, such as Cu. Much stronger adhesion is needed at interfaces of different materials to ensure the BEOL

reliability. In the interconnect damascene process, a very harsh chemical-mechanical polishing (CMP) step is performed to remove excess Cu after the electro-plating deposition;<sup>3</sup> therefore, the liner needs to provide strong-enough adhesion to avoid the desired part of Cu being removed.<sup>3</sup> In addition, it has been demonstrated that the inferior adhesion can lead to worse electromigration lifetime.<sup>47</sup> To give a quick assessment of adhesion properties of 2D materials, a simple tape test can be used.<sup>27,48,49</sup> The procedure is described in Fig. 7. The 2D-material-under-test was first deposited to cover half of a substrate. A Cu layer ( $\sim 80$  nm in this example) was then deposited on the entire sample. A 3M Scotch<sup>®</sup> tape was attached on the sample and then detached. A qualified liner needs to prevent Cu from being peeled off by the tape during the detaching process. As summarized in Table I, among the 2D materials that are tested, only  $\text{TaS}_2$  passes the tape test and proceeds to be compared with Ta (standard liner) using an industrial-standard method,<sup>50</sup> i.e., a 4-point bending test.<sup>51–53</sup> The measurement setup is roughly illustrated in Fig. 8(a), and details can be found in other works.<sup>51,52</sup> Load-displacement curves obtained from measurements



**FIG. 7.** Adhesion test using the tape method. 2D-material-under-test ( $\text{TaS}_2$  as the example) is first deposited on half of a  $\text{SiO}_2$  substrate.  $\sim 80$  nm Cu is then deposited on the entire sample, followed by the tape attachment. After detaching the tape, only Cu on  $\text{TaS}_2$  remains, indicating that  $\text{TaS}_2$  is a qualified liner given that it provides sufficient adhesion to Cu and the dielectric underneath. Reproduced with permission from Lo *et al.*, *Adv. Mater.* **31**, 1902397 (2019). Copyright 2019 Wiley.

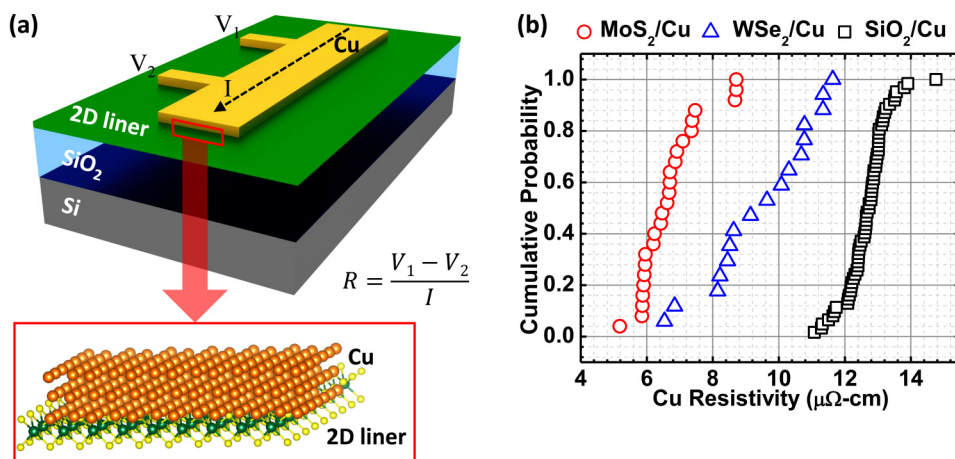


**FIG. 8.** Adhesion test using a four-probe bending method. (a) The material stack adopted for the test. Forces are applied to bend the sample. After a certain point, delamination occurs at the interface of Cu and liner-under-test. (b) Load-displacement curve with distinct behaviors before and after the delamination for both Ta and TaS<sub>2</sub>. The behavior of TaS<sub>2</sub> can be attributed to a not-optimized-yet interface, as also observed in another work.<sup>51</sup> (c) Adhesion energies of Ta and TaS<sub>2</sub> extracted from (b). TaS<sub>2</sub> shows an adhesion property similar to Ta. Reproduced with permission from Lo et al., in *IEEE International Interconnect Technology Conference* (IEEE, 2019). Copyright 2019 IEEE.

are shown in Fig. 8(b). At the early stage, the load increases linearly with the increasing displacement due to bending of the sample. Beyond a certain point, the load will drop abruptly, indicating the occurrence of delamination. By using the values of load and displacement at the delamination point, the adhesion energy or the strain energy release rate (G) can be obtained. Details of the theory and more examples can be found in the literature.<sup>52,53</sup> It is calculated that the G values of Ta and TaS<sub>2</sub> are similar, as shown in Fig. 8(c), confirming the strong adhesion of TaS<sub>2</sub> with the Cu and SiO<sub>2</sub> substrate.

In addition to the wetting and adhesion properties, researchers have found that 2D materials can reduce Cu resistivity in ultra-scaled dimensions and attributed that to reduced inelastic surface/interface scattering at 2D/Cu interfaces.<sup>54,55</sup> It is well known that Cu resistivity

increases as its dimensions are reduced, mainly due to increased grain boundary scattering and inelastic surface/interface scattering.<sup>56,57</sup> Especially in an ultra-scaled interconnect, much more pronounced inelastic surface/interface scattering is the main factor responsible for the deteriorated Cu resistivity. It has been discovered that the perturbing localized interfacial states at the Ta/Cu interface cause more inelastic scattering of electrons in Cu.<sup>58,59</sup> On the other hand, experimental observation of improved Cu resistivity when its surface is passivated by graphene<sup>54</sup> leads to follow-up experimental and theoretical studies on other 2D materials,<sup>55,60</sup> which all conclude that the weak interaction between Cu and 2D materials can result in reduced interface scattering. In Ref. 55, the experimental test structure consists of a Cu thin film deposited on a 2D liner-under-test, as illustrated in Fig. 9(a). The reason of using thin Cu (~15 nm) is to



**FIG. 9.** (a) Cu thin film deposited on different liners/under-test. Contribution from surface/interface scattering at Cu/liner is enlarged by using thin Cu. Resistance is measured accurately using the Kelvin structure. (b) Cu resistivity of devices without a liner (Cu on SiO<sub>2</sub>) and with MoS<sub>2</sub> and WSe<sub>2</sub> as the liners. The results indicate that 2D materials can reduce inelastic surface/interface scattering and improve Cu conductivity. Reproduced with permission from ACS Appl. Mater. Interfaces 11, 28345. Copyright 2019 American Chemical Society.



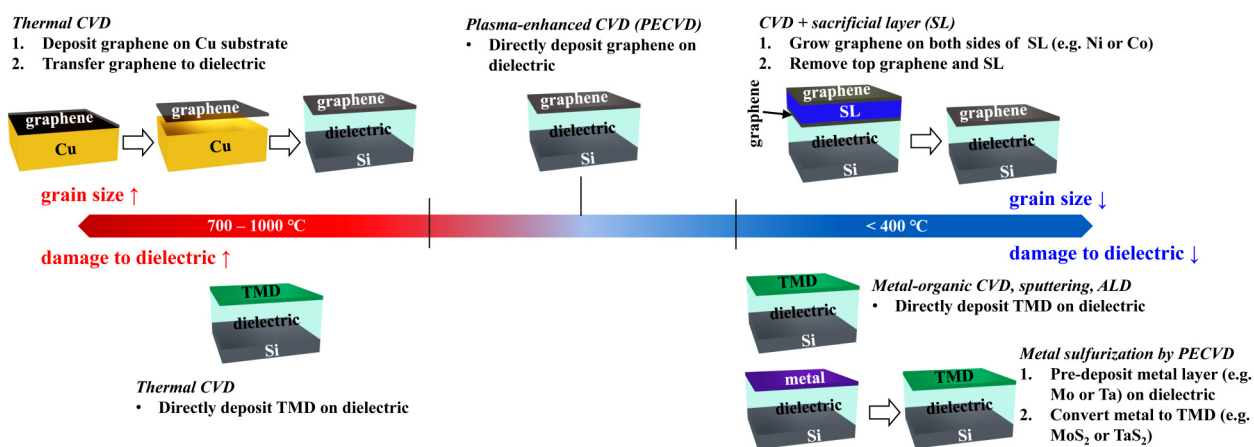
enhance the scattering contribution from the interface. The Cu thin film is patterned into the so-called Kelvin structure to obtain an accurate resistance measurement. After carefully measuring the dimensions, including length, width, and thickness of the patterned Cu thin film, Cu resistivity can be calculated. The results are shown in Fig. 9(b), where each point represents the value obtained from a single test structure. As observed, when MoS<sub>2</sub> and WSe<sub>2</sub> are used as the liner, Cu resistivity is obviously reduced, suggesting 2D liners are able to reduce inelastic interface scattering. Note that even though the values from Ta/Cu are not shown here, it is known that Cu resistivity is even higher in the case of Cu on Ta, as compared to Cu on oxides.<sup>59</sup> More details can be found in the work of Shen *et al.*<sup>55</sup> Other 2D materials including TaS<sub>2</sub><sup>27</sup> have also shown a similar benefit. Comparison of diffusion barrier and liner properties of various 2D materials is summarized in Table I. It is important to note that all evaluations and comparisons here are based on the materials synthesized in respective references. Further research and effort on materials to improve the quality of materials can certainly change the outcome.

#### IV. DEPOSITION ON DIELECTRICS

In the state-of-the-art BEOL processes, barrier and liner are deposited on low-*k* dielectrics before the deposition of Cu. The differences between conventional TaN/Ta deposition and current 2D material synthesis will require major design and process modifications. Physical vapor deposition (PVD), more specifically, sputtering has been used to deposit TaN and Ta.<sup>64,65</sup> On the other hand, large area 2D materials are typically synthesized by chemical vapor deposition (CVD).<sup>66</sup> The key differences between PVD and CVD are the substrate preference and process temperature. First, successful film deposition by PVD is less dependent on the targeted substrate. Although different substrates can result in different crystallinity, surface morphology, and so on, formation of a certain

type of film is guaranteed.<sup>7</sup> However, in the case of CVD for 2D materials, choice of substrates is crucial since the film might not be grown at all on certain substrates. For example, it is well known that graphene prefers to grow on Cu rather than on dielectrics.<sup>67</sup> Using the same growth conditions, replacing Cu by dielectric as the substrate may result in a complete absence of film formation.<sup>67</sup> Therefore, it is important to identify synthesis approaches that can successfully deposit uniform 2D materials directly on dielectric substrates. In early works where graphene was investigated as a diffusion barrier,<sup>12–15</sup> graphene was first grown on Cu foils at 1000 °C, followed by a wet process to be transferred onto dielectrics for diffusion barrier property testing, as depicted in the top-left part of Fig. 10. Although this method is suitable for preliminary evaluations of unexplored materials, transferring these atomically thin films at the wafer scale appears to be a major challenge for BEOL applications. Therefore, efforts have been made to directly grow graphene on dielectric substrates to avoid the transfer process.<sup>12–15</sup> On the other hand, transition-metal dichalcogenides (TMDs) favor to be grown on dielectrics (the bottom-left part of Fig. 10), as shown by many early TMD works.<sup>66</sup> Nevertheless, the growth temperature for 2D material synthesis remains to be a concern, as discussed below.

In BEOL, the process temperature must be close or below 400 °C. Otherwise, both the low-*k* dielectric and previously deposited Cu at lower levels can be damaged.<sup>17</sup> However, the temperature for conventional CVD growth of 2D materials is normally above 700 °C due to the requirement of thermal energy to dissociate the precursors. These types of CVD are also known as the “thermal CVD.” To reduce the growth temperature, plasma-enhanced CVD (PECVD) has been adopted since plasma can assist in dissociating the bonds of precursors, hence reduce the demand of high thermal energy. Graphene directly grown on dielectrics at 550 °C has been demonstrated by Mehta *et al.* using PECVD,<sup>16</sup> as illustrated in the top-middle part of Fig. 10. However, to further bring down the

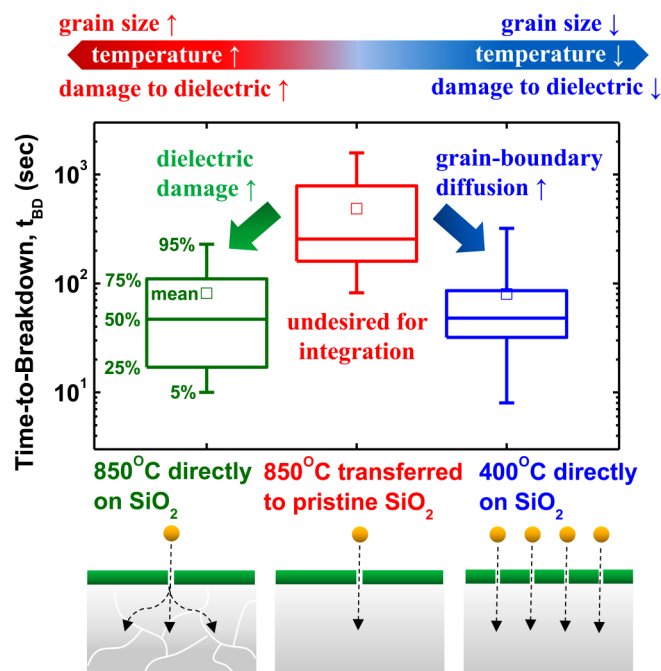


**FIG. 10.** Various synthesis methods of 2D materials. Graphene prefers to grow on metal surfaces, while TMDs can be deposited on dielectrics at similar temperatures. Conventional “thermal CVD” is not suitable for BEOL due to the high temperature requirement. Therefore, PECVD is adopted to lower the growth temperature. A sacrificial layer (SL), together with PECVD, are utilized for depositing graphene on dielectrics at BEOL-compatible temperatures. Sulfurization of pre-deposited metals, MOCVD, sputtering, and ALD have all been used for low-temperature TMD growth.

temperature to be BEOL-compatible, a sacrificial layer (SL) needs to be employed for graphene growth on dielectrics.<sup>61,68,69</sup> In this approach, a metal sacrificial layer with high solubility of carbon (normally Ni or Co) is first deposited on dielectric. Since graphene prefers to grow on metals, a layer is formed on the top of the metal surface. In the meantime, carbon atoms can diffuse into the metal due to the high solubility and arrive at the interface between the sacrificial metal and the dielectric. Finally, carbon atoms accumulated at the interface form graphene layers underneath the metal. The SL and the top graphene layer are then removed, leaving the bottom graphene film directly on the dielectric. The procedure is briefly illustrated in the top-right part of Fig. 10. Detailed mechanisms are nicely described in the work of Kwak *et al.*<sup>68</sup> In the case of TMDs, successful growth at BEOL-compatible temperatures has been demonstrated using PECVD.<sup>27,70,71</sup> Metal layers can be first deposited on dielectrics, followed by a conversion step by a PECVD process. For example, Mo and Ta thin films can be sulfurized by H<sub>2</sub>S gas through a PECVD process and get converted into MoS<sub>2</sub><sup>70,71</sup> and TaS<sub>2</sub>,<sup>27</sup> respectively, at BEOL-compatible temperatures. In addition to PECVD, metal-organic CVD (MOCVD) has also been adopted for a direct deposition of MoS<sub>2</sub> on dielectrics at 400–450 °C.<sup>31,62</sup> Methods for BEOL-compatible TMD growth are depicted in the bottom-right part of Fig. 10.

The importance of lower growth temperatures is highlighted in Fig. 11. The high temperature damage to dielectric can be observed by comparing the time-to-breakdown between two processes (green and red boxes). The green box represents the statistics of  $t_{BD}$  from devices with direct-deposited MoS<sub>2</sub> barriers at 850 °C.<sup>30,72</sup> When the same MoS<sub>2</sub> is transferred to a substrate that has not gone through the high temperature process,  $t_{BD}$  of devices increases obviously, as shown in the red box. Since the qualities of two MoS<sub>2</sub> films should be nearly identical, the enhanced  $t_{BD}$  indicates a better quality of the latter dielectric, as a more defective dielectric will facilitate more Cu diffusion.<sup>34,37</sup>

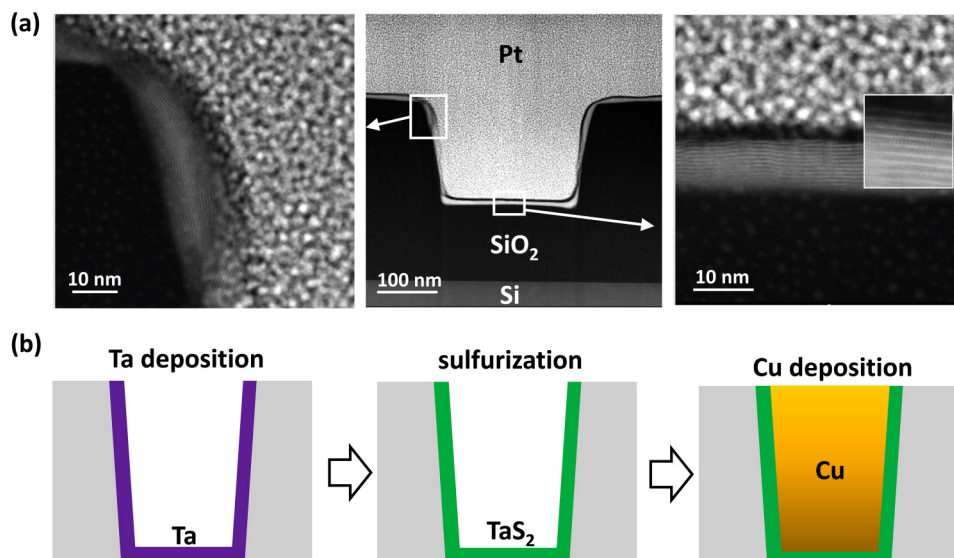
Although low-temperature synthesis can be realized by the above-mentioned approaches, growth at lower temperatures normally results in films with smaller grain sizes. Since grain boundaries are the main diffusion paths for Cu,<sup>22</sup> barriers with smaller grain sizes will have inferior performance. For instance, with high-temperature CVD growth, the grain size is normally on the order of a few to tens of micrometers,<sup>30,72</sup> whereas grain sizes of tens of nanometers are often found in low-temperature-grown 2D materials.<sup>31</sup> The compromised diffusion barrier property of low-temperature MoS<sub>2</sub> barrier can be noticed by comparing the red and blue boxes in Fig. 11. Since the dielectric is hardly damaged,<sup>31</sup> the degraded performance is attributed to the smaller grain sizes or more grain boundaries, which facilitate more Cu diffusion. Nevertheless, the grain sizes of the 2D materials are still comparable to sputtered TaN and Ta whose grain sizes are also in the range to tens of nanometers.<sup>20</sup> In fact, the columnar structure in TaN/Ta<sup>20,64,73</sup> can possibly make grain boundary diffusion more severe than in 2D materials. In addition, although the grain size is limited by current CVD techniques, achieving single-layer 2D materials with a large grain size is fundamentally possible due to the material nature. This could be one of the future research focuses in this area. On the other hand, TaN/Ta would already be discontinued at the same atomic thickness due to their 3D natures.



**FIG. 11.** Comparison of diffusion barrier properties among 2D materials grown at different temperatures, with MoS<sub>2</sub> as the example. The green box represents  $t_{BD}$  of multiple devices with directly deposited MoS<sub>2</sub> at 850 °C, while the red box is from  $t_{BD}$  values of devices with the same MoS<sub>2</sub> but transferred onto a pristine SiO<sub>2</sub>. Although high-temperature synthesis leads to a better film quality, the dielectric would be severely damaged, as can be observed by comparing the green and red boxes. The blue box represents  $t_{BD}$  values of devices with a 400 °C-grown MoS<sub>2</sub>. The inferior barrier property of a low-temperature synthesized barrier can be noticed by comparing the red and blue boxes, which is attributed to a smaller grain size. Reproduced with permission from Lo *et al.*, npj 2D Mater. Appl. 1, 42 (2017). Copyright 2017 Author(s), licensed under a Creative Commons Attribution License; IEEE Electron Device Lett. 39, 6 (2018). Copyright 2018 IEEE.

Other growth methods, such as sputtering<sup>74,75</sup> and atomic-layer deposition (ALD),<sup>76</sup> have also been demonstrated to carry out 2D material synthesis at even lower temperatures ( $\ll 400$  °C). However, without annealing ( $>400$  °C) processes, as-deposited films are nano-crystalline or even amorphous, which leads to an inferior diffusion barrier property, as discussed and shown in Fig. 11. More research needs to be done to grow high-quality 2D materials using these methods. In summary, growth recipes need to be further investigated to improve film quality as well as to reduce dielectric damage. In addition to reducing the thermal damage, it is also important to reduce the damage from other sources, such as plasma power, to minimize potential damages to dielectrics.

Finally, it is also important to investigate whether the synthesis methods can ensure conformal deposition in damascene structures with high aspect ratios. Therefore, efforts must also be made to deposit 2D materials in trench structures.<sup>77,78</sup> In principle, two methodologies have been utilized. In the MoS<sub>2</sub> work of Martella *et al.*,<sup>78</sup> ALD MoO<sub>x</sub> layers were first deposited, followed by



**FIG. 12.** (a) Deposition of  $\text{MoS}_2$  along a trench structure using thermal-CVD. Layered structures can be observed. However, conformity still needs to be improved. More conformal and thinner 2D films deposited at a BEOL-compatible temperature is the goal to pursue. (b) Proposed method for a BEOL-compatible  $\text{TaS}_2$  deposited in the trench. Since conformal deposition of Ta (and TaN) has been well developed by the industry, a conformal  $\text{TaS}_2$  could be realized by sulfurizing the Ta (or TaN) film using the BEOL-compatible PECVD process in Ref. 27.

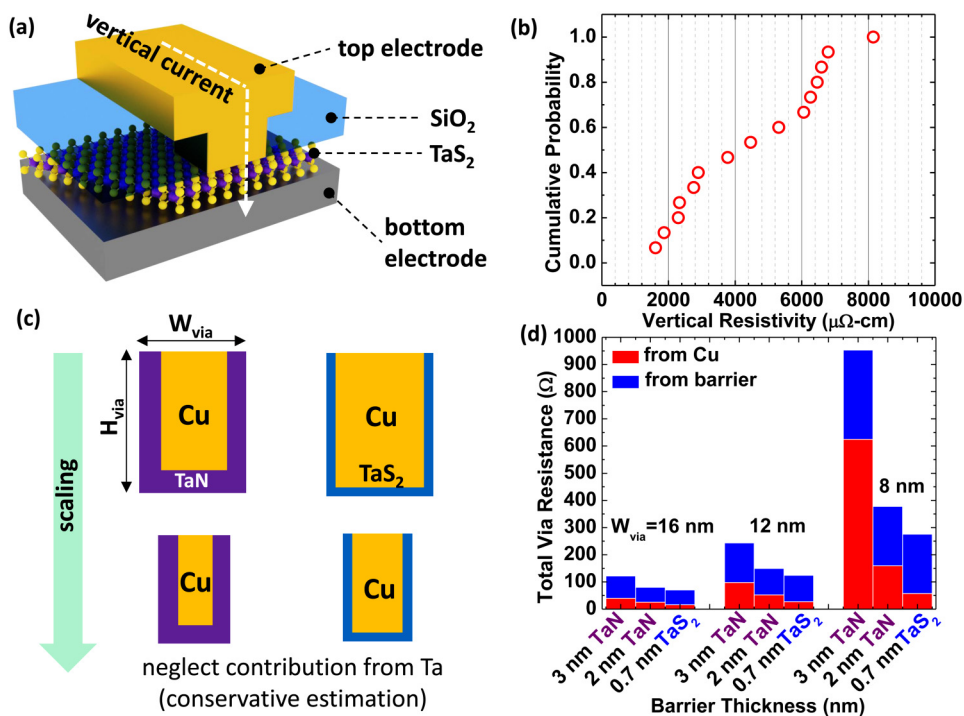
sulfurization; whereas Jin *et al.* directly deposited  $\text{MoS}_2$  and  $\text{WS}_2$  using MOCVD.<sup>77</sup> Here, we also demonstrate direct deposition of  $\text{MoS}_2$  in trench structures using thermal CVD at a high temperature (just to explore the conformability), as shown in Fig. 12(a). Thick films are deposited for preliminary investigations with the focus on conformability at some critical positions in the trench. It is found that trench edges and sidewalls are much harder to cover compared to the bottom surface. Note that none of the works mentioned above is BEOL-compatible up to date. Therefore, lower growth temperatures, more conformal deposition, and thinner films are the goals to achieve for trench deposition. Since conformal deposition of Ta (and TaN) has already been developed by the industry, we believe that converting pre-deposited TaN/Ta into uniform  $\text{TaS}_2$  in damascene through the PECVD sulfurization process<sup>27</sup> discussed above is potentially feasible, as illustrated in Fig. 12(b).

## V. VERTICAL CONDUCTION (VIA RESISTANCE) THROUGH 2D MATERIALS

“Via” is a connection between interconnects from different levels, as sketched in Fig. 1. Via resistance has been one of the major bottlenecks for overall interconnect performance at advanced technology nodes. Since the selective deposition of barrier/liner only on the sidewalls rather than on the vias should be avoided due to electromigration concerns,<sup>79,80</sup> when current flows from an upper level Cu wire, through a via, to a lower-level wire, it has to go across the highly resistive Ta/TaN layer at the bottom of the via. As mentioned above, since the thickness of the barrier/liner stack cannot be scaled proportionally, the via resistance becomes even larger with the via width (area) scaling. Although the ultra-thin 2D barrier/liner has the advantage of enlarging the Cu cross-sectional area, the vertical current conduction across these novel materials has seldomly been discussed. Among the few 2D materials that

have been investigated for BEOL applications,  $\text{TaS}_2$  is chosen for the study here since it has been evaluated more thoroughly from various aspects and benchmarked with conventional materials, as described in Secs. II–IV. Early works have shown that in-plane room temperature resistivities of 1T- $\text{TaS}_2$  and 2H- $\text{TaS}_2$  are  $\sim 300 \mu\Omega \text{ cm}$  and  $150 \mu\Omega \text{ cm}$ , respectively,<sup>81–83</sup> both of which are lower than that of TaN ( $\sim 700 \mu\Omega \text{ cm}$ ).<sup>84</sup> However, unlike TaN or Ta, the conduction in 2D materials is anisotropic, meaning that the out-of-plane (vertical) resistivity of  $\text{TaS}_2$  could be very different from their in-plane counterparts. In fact, the out-of-plane resistivity of 2H- $\text{TaS}_2$  is as high as  $\sim 5000 \mu\Omega \text{ cm}$ ,<sup>82</sup> while it reaches  $7 \times 10^5 \mu\Omega \text{ cm}$  in 1T- $\text{TaS}_2$ .<sup>83</sup> Despite the high vertical resistivity of  $\text{TaS}_2$ , the overall resistance of  $\text{TaS}_2/\text{Cu}$  via could still outperform the conventional structure of TaN/Ta/Cu since (i) the required thickness of  $\text{TaS}_2$  can be thinner and (ii) the enlarged Cu volume by 2D barrier/liner becomes even more obvious in ultra-scaled dimensions, both of which will be elaborated in the following discussions.

To understand intrinsic properties and avoid deteriorated characteristics due to imperfect material synthesis at the current stage, we exfoliated  $\text{TaS}_2$  films from commercially purchased crystals (2D Semiconductors) and performed electrical measurements on 2H- $\text{TaS}_2$  because of its lower out-of-plane resistivity<sup>82</sup> and potentially lower growth temperatures as opposed to 1T- $\text{TaS}_2$ .<sup>24</sup> Precautions were taken for the test structure design and fabrication since the vertical conduction can be affected by many subtle imperfections, such as surface oxidation of  $\text{TaS}_2$  and electrodes or any process contamination. The device structure is shown in Fig. 13(a). A  $\text{SiO}_2$  (60 nm) layer was deposited by an e-beam evaporator to isolate the top and bottom electrodes. A window was then opened in the  $\text{SiO}_2$  layer to guide the current to flow through  $\text{TaS}_2$  vertically, followed by the top electrode formation. The choice of the electrodes is critical since both oxidation and poor adhesion could severely affect the vertical conduction. Therefore, the bottom electrode is chosen to be Ti/Au (5 nm/25 nm) to avoid oxidation



**FIG. 13.** (a) A test device structure to measure the vertical resistivity of 2D materials. A  $\text{SiO}_2$  layer is adopted as the isolation and to define the area of vertical conduction. (b) Values of vertical resistivity of 2H-TaS<sub>2</sub> from multiple devices. (c) Comparison of via scaling in the cases of using TaN and TaS<sub>2</sub> as the barrier. (d) Comparison of total via resistance using different TaN and TaS<sub>2</sub> barriers. Resistance contributions from the Cu segment and barrier are labeled by red and blue colors, respectively. Cu resistance escalates as the via is more scaled, which makes a 2D barrier advantageous.

before exfoliating TaS<sub>2</sub> on it. The top electrode is selected to be Ti/Ni (35 nm/70 nm) to have a better adhesion. Note that since 2H-TaS<sub>2</sub> is metallic in the vertical direction at room temperature,<sup>24,85</sup> the choice of metal work function should be less critical on contact resistances. A set of control devices using the identical design but without TaS<sub>2</sub> flakes between the top and bottom electrodes were also fabricated to subtract parasitic resistances. The results from multiple devices in Fig. 13(b) show that the vertical resistivity can be as low as  $\sim 2000 \mu\Omega \text{ cm}$ .

To estimate the overall via resistance with technology scaling, a semi-empirical model proposed by Ciofi *et al.*<sup>86</sup> was adopted to calculate Cu resistivity by considering its size effect. Contribution from Ta was first neglected for simplicity, which is a conservative assumption. As demonstrated in Fig. 13(d), even with a  $\sim 3\times$  higher resistivity of 2H-TaS<sub>2</sub>, the contribution from TaS<sub>2</sub> is similar to that from TaN since TaS<sub>2</sub> can be thinner. The resistance contribution from Cu tremendously increases in extremely scaled dimensions because TaN occupies a huge portion. On the contrary, when TaS<sub>2</sub> is used, contribution from Cu is much lower due to the much larger Cu percentage. In summary, even with the higher vertical resistivity of TaS<sub>2</sub>, replacing TaN/Ta with TaS<sub>2</sub> is still beneficial for via resistance, which further helps reduce the bottleneck of interconnect scaling.

## VI. OTHER APPLICATIONS

So far, this article has discussed various aspects of using 2D materials as the diffusion barrier and liner for Cu interconnects. Moreover, 2D materials could offer other functions to different

parts of Cu interconnects or even to other types interconnects, which will be briefly introduced in this section.

### A. Electromigration

One of the limiting factors of the lifetime of a metal wire is its resistance to electromigration (EM). EM occurs in metal wires due to the momentum transfer between electrons and metal atoms.<sup>87</sup> Voids in metal wires and vias will eventually appear due to the current induced atom movement, leading to the malfunction of interconnects. According to the International Technology Roadmap for Semiconductors (<http://www.itrs2.net/>), reduced interconnect cross sections and boosted maximum chip operation frequency unavoidably increase the maximum current density ( $J_{\text{max}}$ ) required for targeted performance to be close to or even exceed the current density ( $J_{\text{EM}}$ ) for EM to occur. As a result, EM must be mitigated in order to maintain continuous performance improvement. As depicted in Fig. 1, a Cu wire is surrounded by a barrier/liner on the sidewalls and bottom of the trench. At the top surface, Cu is polished by the CMP process, as briefly mentioned in Sec. III. Studies have shown that this post-CMP surface becomes one of the dominant paths for EM to occur.<sup>47</sup> To alleviate the CMP damage and enhance EM lifetime, various materials, such as Co,<sup>88</sup> CoWP,<sup>47,79</sup> and the related,<sup>79</sup> have been capped on the top surface of Cu along the history of interconnect development. These layers are also referred to as the “capping layers.”

In addition to conventional capping layer materials, graphene has recently been shown to prolong EM lifetime.<sup>89,90</sup> It has been claimed that the Cu EM lifetime can be extended by  $\sim 10\times$  due to the improved interface between graphene and Cu.<sup>89,90</sup>



Conventional capping layers are selectively deposited on the Cu surface. Therefore, graphene can fulfill the requirement quite well since it favors the deposition on Cu than on dielectrics, as discussed in Sec. IV. Although the thickness requirement may not be as critical as a barrier/liner in current and near-future technologies, it is still interesting to have more thorough understanding of impact of 2D materials on EM lifetime. In authors' opinion, a few more tasks must be conducted before concluding graphene is a better EM lifetime enhancer than standard capping materials. First, in order to have a real EM failure instead of a failure from Joule heating, measurements had been performed at lower current densities, ranging from  $0.6 \text{ MA/cm}^2$  to  $3.6 \text{ MA/cm}^2$ .<sup>79,80,88,91</sup> However, due to the limitation of the setups in research facilities, in the graphene works,<sup>89,90</sup> the current density is much higher ( $>20 \text{ MA/cm}^2$ ) to accelerate the failure. In this case, it is difficult to determine whether the failure is mainly due to EM. On the contrary, days,<sup>80,88,91</sup> or even months,<sup>79</sup> of measurement for a single device can be performed in an industrial setup. To solve this issue, the low-frequency-noise method well developed by Beyne *et al.*<sup>92</sup> can be adopted. Second, the depositions of graphene and standard capping layers (e.g., CoWP<sup>89</sup>) could lead to completely different grain structures of the capped Cu due to the distinct deposition methods. To perform a fair comparison, the contribution from Cu needs to be eliminated, meaning that the Cu grain structure must be identical in both cases. If graphene eventually gets adopted by BEOL technologies as the capping layer, prior to the formation of the next-level vias, graphene needs to be selectively removed in the via areas by some unique etching techniques,<sup>93,94</sup> which does not involve  $\text{O}_2$  plasma based conventional graphene etching recipes<sup>95</sup> to avoid Cu oxidation. Finally, the graphene demonstrated so far for EM measurements comes with a relatively thick amorphous carbon layer,<sup>89,90</sup> which certainly compromise the advantages of 2D materials. Thus, it is necessary to eliminate the carbon layer.

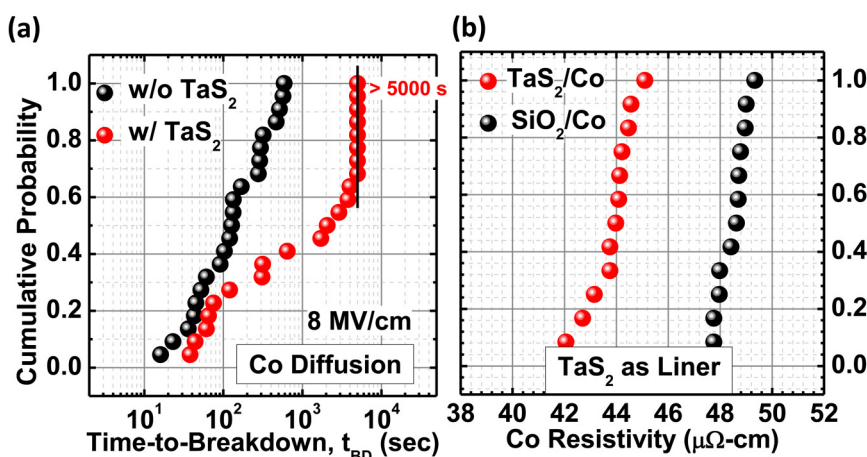
## B. Cobalt interconnect

Cobalt (Co) and ruthenium (Ru) have been extensively investigated in the past few years as the replacement of Cu. Their

promises lie in the possibility to be barrier-free, lower resistivity compared to Cu in extremely scaled dimensions due to a shorter mean free path<sup>96–99</sup> and superior EM lifetime.<sup>92,100,101</sup> Even without the need of a diffusion barrier, an adhesion layer, in analogy to the liner for Cu, is generally required.<sup>96</sup> Therefore, the surface/interface scattering between ultra-scaled Co or Ru and their adhesion layers could play a critical role in their resistivities,<sup>102</sup> as discussed in Sec. III. In addition, despite the early presumption that a barrier would not be necessary, Co and Ru have been found to diffuse into dielectrics under certain conditions.<sup>103,104</sup>  $\text{TaS}_2$  grown at  $400^\circ\text{C}$  was tested to explore whether the benefits for Cu interconnects in terms of blocking diffusion and scattering reduction also apply to Co interconnects.<sup>50</sup> Figure 14(a) shows the test results of Co diffusion using the capacitor structure in Fig. 4(a). It can be observed that with  $\text{TaS}_2$  in-between Co and  $\text{SiO}_2$ ,  $t_{\text{BD}}$  of devices increases in general, indicating the suppression of Co diffusion. In addition, when thin Co ( $\sim 12 \text{ nm}$ ) is patterned in the Kelvin structure shown in Fig. 9(a) and is deposited on  $\text{TaS}_2$ , it is found in Fig. 14(b) that Co resistivity is reduced, indicating a more elastic surface/interface scattering facilitated by  $\text{TaS}_2$ . In short,  $\text{TaS}_2$  provides desired barrier and liner properties for Co interconnects, which might be useful for future interconnect technologies.

## C. Radio-frequency (RF) transmission line

With the emergence of 5G communication and increased interest in millimeter-wave (mm-wave) applications, much effort has been made to increase the maximum frequency of RF circuits and systems. This not only requires active devices with higher cut-off frequencies, but also requires passive components, such as transmission lines, to operate at higher frequencies. At higher frequencies, the RF power loss along typical metal transmission lines can increase drastically, limiting operational bandwidth of the entire circuit. Conventionally, RF transmission lines are designed on the top layers of interconnects since thicker and wider transmission lines exhibit lower power losses.<sup>105</sup> Recently, with the increased interest in the monolithic integration of mm-wave capabilities with CMOS technology, high bandwidth transmission lines with dimensions in the range of tens of nanometers are required to be



**FIG. 14.** (a) TDDb measurements for Co diffusion. Devices with  $\text{TaS}_2$  barriers have longer  $t_{\text{BD}}$ , indicating the suppression of Co diffusion. (b) When  $\text{TaS}_2$  is used as the liner for Co interconnects, Co resistivity decreases, which is attributed to the mitigation of inelastic surface/interface scattering. Reproduced with permission from Lo *et al.*, in *IEEE International Interconnect Technology Conference* (IEEE, 2019). Copyright 2019 IEEE.

comparable to the dimensions of low level interconnects in standard CMOS structures.<sup>106,107</sup> This highlights the need for RF “nano-transmission” lines in the recent years,<sup>108–111</sup> explored here using 2D layered materials.

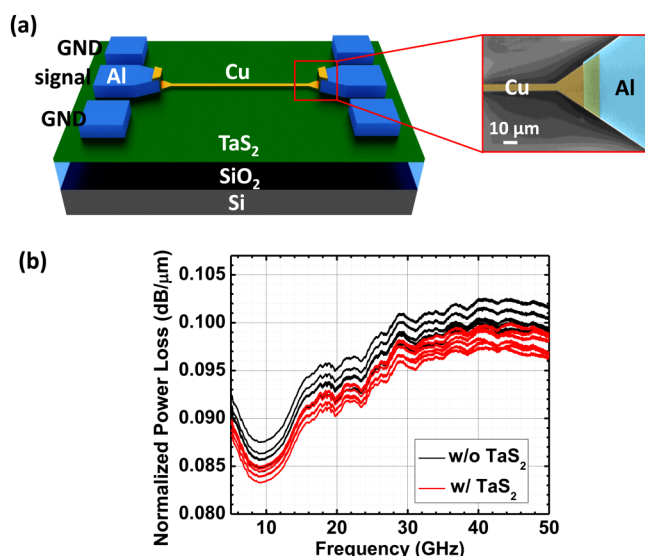
The reason of integrating 2D layered materials with RF transmission lines lies in the fact that 2D materials can reduce inelastic surface/interface scattering of Cu wires and hence reduce Cu resistivity, as discussed in Sec. III. Reducing the line resistance directly translates to reduction of transmission line power loss.

In our experiments, we used our PECVD grown, large area TaS<sub>2</sub> films for initial prototype testing. The structure of the transmission line is shown in Fig. 15(a). 2-nm TaS<sub>2</sub> was first deposited on top of 1.5- $\mu$ m SiO<sub>2</sub>. Thick SiO<sub>2</sub> was selected to minimize the electrical feedthrough in the Si substrate during RF measurement. A 500-nm Al layer was then deposited and patterned to form electrodes for probing. Finally, 15-nm-thick/5- $\mu$ m-wide Cu transmission line was deposited and patterned to connect the two Al electrodes. Such a thin Cu layer was chosen to enlarge surface/interface scattering, as discussed in Sec. III. In addition to the transmission line structure, “open” and “short” structures were also fabricated for the de-embedding process. “Open” structures have no Cu line between the two Al electrodes, while “short” structures connect Al signal pads directly to adjacent ground (GND) pads. RF characterization was performed using a standard two-port S-parameter measurement, with RF input power being set at -10 dBm. The measured information from the “open” and “short”

features was used to de-embed the parasitic capacitance and inductance from the metal electrodes and electrical routing. Thus, the results after the de-embedding procedure reflect the behavior of the isolated Cu transmission line. Note that the conduction through the TaS<sub>2</sub> film is negligible here since the resistivity of TaS<sub>2</sub> ( $\sim 10^7 \mu\Omega \text{ cm}$ ) is orders of magnitude higher than Cu ( $\sim 10 \mu\Omega \text{ cm}$  with this dimension). The measured results of different devices with and without TaS<sub>2</sub> are shown in Fig. 15(b). It can be clearly observed that with the presence of TaS<sub>2</sub>, the power loss of transmission lines is reduced, even when taking the device-to-device variation originated from the fabrication into account. The reduction of power loss is attributed to the reduction in Cu resistivity. In the DC regime, as shown in Ref. 27, the reduction in Cu resistivity is around 10%, while an average reduction of around 2% is obtained in the RF regime. Further power loss reduction can be achieved through quality improvement of the 2D films since we have observed a much larger resistivity reduction ( $\sim 45\%$ ) by using exfoliated, high quality MoS<sub>2</sub> films.<sup>72</sup> Nevertheless, our results provide the initial validation that the benefits of 2D materials in the DC regime to reduce Cu resistivity can be translated to the RF regime to mitigate power loss.

## VII. CONCLUSION

To enable continued scaling of interconnect technology, 2D materials, owing to their atomic-thin-body nature, have been proposed and explored as the candidates for replacing conventional diffusion barriers and liners. This article has reviewed and summarized works on 2D materials such as Cu diffusion barrier and liner alternatives. DFT calculations have predicted that many 2D materials have the potential of being used as diffusion barriers. Experimental verifications of diffusion barrier properties using various techniques, including TVS, CV, and TDDB methods, have demonstrated that many 2D materials, including graphene, h-BN, MoS<sub>2</sub>, and TaS<sub>2</sub>, are suitable candidates. Since these techniques rely on large-area and continuous films, evaluations on many other 2D materials can be expected when their syntheses become more mature. In addition to diffusion barrier properties, liner properties are also critical when determining the potentials of 2D materials. Therefore, the tests of liner properties have been conducted in different aspects, including wettability, adhesion, and surface/interface scattering. Despite promising results in wettability and reduced surface scattering for many 2D materials, only TaS<sub>2</sub> has been shown to provide desirable adhesion with Cu up to date. Furthermore, the requirements and challenges of synthesizing 2D materials on dielectrics have also been discussed. One of the main challenges is the temperature required to realize high-quality films. Although BEOL compatible, low-temperature syntheses have been demonstrated and film quality could be compromised at low temperatures. Additionally, damage from plasma growth processes have to be mitigated to prevent quality degradation of low- $k$  dielectrics. Finally, conformal deposition of ultra-thin 2D materials over damascene structures has to be carried out at BEOL compatible temperatures. In the aspect of circuit performance, since via resistance has become one of the bottlenecks, vertical conduction across these novel materials has to be studied. TaS<sub>2</sub> has been adopted as an example of conducting the study. In addition to



**FIG. 15.** (a) Device structure for RF transmission line measurements. Thicker Al is first deposited as the electrodes. A thin (to enlarge surface/interface scattering) Cu transmission line is then deposited. An “open” structure with no Cu line in-between two Al signal lines and a “short” structure with two Al signal lines directly connected are also fabricated for the de-embedding process. (b) Normalized RF power loss of devices with and without TaS<sub>2</sub>. It is shown that TaS<sub>2</sub> can reduce the power loss, which can be attributed to the reduction of Cu resistivity/resistance.

serving as the barrier and liner for metal interconnects, 2D materials also possess promises in other applications, including eliminating electromigration and enhancing RF transmission line performance. The results have been demonstrated in the hope of encouraging more relevant research in the future. In summary, both the great potential and challenges of adopting 2D materials in BEOL have been extensively discussed throughout the article. Possible solutions for the remaining challenges and routes for future development have also been proposed.

## VIII. METHODS

### A. Density functional theory

The geometry optimization minimum potential energy surfaces for Cu diffusion across TMDs were carried out using DFT as implemented in the Vienna *ab initio* simulation package (VASP).<sup>112,113</sup> Projector-augmented-wave (PAW) potentials<sup>114,115</sup> were used to account for the electron-ion interactions, and the electron exchange-correlation potential was calculated using the generalized gradient approximation (GGA) within the Perdew-Burke-Ernzerhof (PBE)<sup>116</sup> scheme using real-space projections. Since long-range dispersion interactions are not captured by the GGA functional, we employed Grimme's DFT-D3 energy correction scheme to account for these interactions.<sup>117</sup> In the DFT-D3 scheme, the Kohn-Sham DFT energy is corrected by adding a pairwise term that depends on the local environment of each atom. The kinetic energy cutoff for all calculations was set to 500 eV, and, due to the relatively large simulation size, a gamma-centered  $4 \times 4 \times 1$  mesh was used for the k-space sampling. A Gaussian smearing of 0.05 eV and an electronic relaxation tolerance of  $1 \times 10^{-5}$  eV was used for all calculations.

### B. Nudged elastic band

We used the climbing image nudged elastic band (NEB) method as implemented in VASP<sup>118</sup> to determine the minimum potential energy surface and diffusion paths between known initial and final geometries with the Cu atom at local minima (on top of a metal atom for the 2H structures and opposite a chalcogen atom for the 1T structures) on either side of a  $4 \times 4$  monolayer TMD with  $\sim 19$ – $20$  Å of vacuum between out-of-plane periodic images. The minima were obtained by structural relaxations using a conjugate gradient (CG) algorithm with a force tolerance of 0.01 eV/Å. The NEB calculations were initialized from a set of geometries interpolating between initial and final structures; then, the ionic positions of the different geometries are iteratively optimized using only the ionic-force components perpendicular to the hypervector. The energy along the diffusion path was determined by spline interpolation based on the total energy of the individual geometries. Additional details regarding the NEB relaxations can be found in Subsection VIII C.

### C. NEB relaxations

The NEB structural relaxations were carried out using either the damped molecular dynamics or quasi-Newton algorithms. If the NEB forces could not be converged to 0.01 eV/Å under “normal” precision (the VASP input specification `PREC = Normal`), the

precision was increased (`PREC = Accurate`). If convergence could still not be achieved, the density of the FFT grid was increased (`ADDGRID = True`). Only 2H-TaS<sub>2</sub> could not be converged to 0.01 eV/Å and was instead converged to 0.05 eV/Å.

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## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## REFERENCES

- <sup>1</sup>R. Rosenberg, D. C. Edelstein, C.-K. Hu, and K. P. Rodbell, *Annu. Rev. Mater. Sci.* **30**, 229 (2000).
- <sup>2</sup>P. C. Andricacos, *Electrochem. Soc. Interface* **8**, 32 (1999).
- <sup>3</sup>Y. Shacham-diamand, T. Osaka, M. Datta, and T. Ohba, *Advanced Nanoscale ULSI Interconnects* (Springer US, 2009).
- <sup>4</sup>J. R. Lloyd, C. E. Murray, S. Ponoht, S. Cohen, and E. Liniger, *Microelectron. Reliab.* **46**, 1643 (2006).
- <sup>5</sup>R. Tsu, J. W. McPherson, and W. R. McKee, in *IEEE International Reliability Physics Symposium Proceedings* (IEEE, 2000), pp. 348–353.
- <sup>6</sup>T. K. S. Wong, *Materials* **5**, 1602 (2012).
- <sup>7</sup>D. Edelstein, C. Uzoh, C. Cabral, P. DeHaven, P. Buchwalter, A. Simon, E. Cooney, S. Malhotra, D. Klaus, H. Rathore, B. Agarwala, and D. Nguyen, in *Proceedings of IEEE International Interconnect Technology Conference* (IEEE, 2001), pp. 9–11.
- <sup>8</sup>W.-L. Wang, C.-T. Wang, W.-C. Chen, K.-T. Peng, M.-H. Yeh, H.-C. Kuo, H.-J. Chien, J.-C. Chuang, and T.-H. Ying, *J. Nanomater.* **2015**, 1–6.
- <sup>9</sup>C. Witt, K. B. Yeap, A. Leśniewska, D. Wan, N. Jordan, I. Ciofi, C. Wu, and Z. Tókei, in *IEEE International Interconnect Technology Conference* (IEEE, 2018), pp. 54–56.
- <sup>10</sup>Z. Wu, R. Li, X. Xie, W. Suen, J. Tseng, N. Bekiaris, R. Vinnakota, K. Kashefzadeh, and M. Naik, in *IEEE International Interconnect Technology Conference* (IEEE, 2018), pp. 149–151.
- <sup>11</sup>C. J. Shearer, A. D. Slattery, A. J. Stapleton, J. G. Shapter, and C. T. Gibson, *Nanotechnology* **27**, 125704 (2016).
- <sup>12</sup>B. S. Nguyen, J.-F. Lin, and D.-C. Perng, *Appl. Phys. Lett.* **104**, 082105 (2014).
- <sup>13</sup>J. Hong, S. Lee, S. Lee, H. Han, C. Mahata, H.-W. Yeon, B. Koo, S.-I. Kim, T. Nam, K. Byun, B.-W. Min, Y.-W. Kim, H. Kim, Y.-C. Joo, and T. Lee, *Nanoscale* **6**, 7503 (2014).
- <sup>14</sup>J. H. Bong, S. J. Yoon, A. Yoon, W. S. Hwang, and B. J. Cho, *Appl. Phys. Lett.* **106**, 063112 (2015).
- <sup>15</sup>L. Li, X. Chen, C.-H. Wang, S. Lee, J. Cao, S. S. Roy, M. S. Arnold, and H.-S. P. Wong, in *Symposium on VLSI Technology* (IEEE, 2015), pp. T122–T123.
- <sup>16</sup>R. Mehta, S. Chugh, and Z. Chen, *Nanoscale* **9**, 1827 (2017).
- <sup>17</sup>R. J. O. M. Hoofman, G. J. A. M. Verheijden, J. Michelon, F. Iacopi, Y. Travaly, M. R. Baklanov, Z. Tokei, and G. P. Beyer, *Microelectron. Eng.* **80**, 337 (2005).
- <sup>18</sup>B. A. Helfrecht, D. M. Guzman, N. Onofrio, and A. H. Strachan, *Phys. Rev. Mater.* **1**, 034001 (2017).

- <sup>19</sup>H. Wang, A. Tiwari, X. Zhang, A. Kvit, and J. Narayan, *Appl. Phys. Lett.* **81**, 1453 (2002).
- <sup>20</sup>J. Nazon, B. Fraisse, J. Sarradin, S. G. Fries, J. C. Tedenac, and N. Fréty, *Appl. Surf. Sci.* **254**, 5670 (2008).
- <sup>21</sup>J.-C. Lin and C. Lee, *J. Electrochem. Soc.* **146**, 3466 (1999).
- <sup>22</sup>Y. Zhao, Z. Liu, T. Sun, L. Zhang, W. Jie, X. Wang, Y. Xie, Y. H. Tsang, H. Long, and Y. Chai, *ACS Nano* **8**, 12601 (2014).
- <sup>23</sup>N. Onofrio, D. Guzman, and A. Strachan, *J. Appl. Phys.* **122**, 185102 (2017).
- <sup>24</sup>R. Zhao, B. Grisafe, R. K. Ghosh, S. Holoviak, B. Wang, K. Wang, N. Briggs, A. Haque, S. Datta, and J. Robinson, *2D Mater.* **5**, 025001 (2018).
- <sup>25</sup>T. Oku, E. Kawakami, M. Uekubo, K. Takahiro, S. Yamaguchi, and M. Murakami, *Appl. Surf. Sci.* **99**, 265 (1996).
- <sup>26</sup>S. W. Loh, D. H. Zhang, C. Y. Li, R. Liu, and A. T. S. Wee, *Thin Solid Films* **462–463**, 240 (2004).
- <sup>27</sup>C. Lo, M. Catalano, A. Khosravi, W. Ge, Y. Ji, D. Y. Zemlyanov, L. Wang, R. Addou, Y. Liu, R. M. Wallace, M. J. Kim, and Z. Chen, *Adv. Mater.* **31**, 1902397 (2019).
- <sup>28</sup>I. Fisher and M. Eizenberg, *Thin Solid Films* **516**, 4111 (2008).
- <sup>29</sup>N. J. Chou, *J. Electrochem. Soc.* **118**, 601 (1971).
- <sup>30</sup>C.-L. Lo, M. Catalano, K. K. H. Smithe, L. Wang, S. Zhang, E. Pop, M. J. Kim, and Z. Chen, *npj 2D Mater. Appl.* **1**, 42 (2017).
- <sup>31</sup>C. L. Lo, K. Zhang, R. Scott Smith, K. Shah, J. A. Robinson, and Z. Chen, *IEEE Electron Device Lett.* **39**, 6 (2018).
- <sup>32</sup>J. W. McPherson, *Microelectron. Reliab.* **52**, 1753 (2012).
- <sup>33</sup>L. Zhao, Z. Tokei, K. Croes, C. J. Wilson, M. Baklanov, G. P. Beyer, and C. Claeys, *Appl. Phys. Lett.* **98**, 032107 (2011).
- <sup>34</sup>N. Suzumura, S. Yamamoto, D. Kodama, K. Makabe, J. Komori, E. Murakami, S. Maegawa, and K. Kubota, in *IEEE International Reliability Physics Symposium* (IEEE, 2006), pp. 484–489.
- <sup>35</sup>K. Croes, M. Pantouvakis, L. Carbonell, L. Zhao, G. P. Beyer, and Z. Tokei, in *IEEE International Reliability Physics Symposium* (IEEE, 2011), pp. 142–148.
- <sup>36</sup>L. Zhao, Z. Tokei, G. G. Gischia, H. Volders, and G. Beyer, in *IEEE International Interconnect Technology Conference* (IEEE, 2009), pp. 206–208.
- <sup>37</sup>F. Chen, O. Bravo, K. Chanda, P. McLaughlin, T. Sullivan, J. Gill, J. Lloyd, R. Kontra, and J. Aitken, in *IEEE International Reliability Physics Symposium* (IEEE, 2006), pp. 46–53.
- <sup>38</sup>J. Noguchi, *IEEE Trans. Electron Devices* **52**, 1743 (2005).
- <sup>39</sup>K. Croes and Z. Tókei, in *IEEE International Reliability Physics Symposium* (IEEE, 2010), pp. 543–548.
- <sup>40</sup>M. A. Alam, R. K. Smith, B. E. Weir, and P. J. Silverman, *Nature* **420**, 378 (2002).
- <sup>41</sup>M. A. Alam, R. K. Smith, B. E. Weir, and P. J. Silverman, in *Digest. International Electron Devices Meeting* (IEEE, 2002), pp. 151–154.
- <sup>42</sup>E. T. Ogawa, J. Kim, G. S. Haase, H. C. Mogul, and J. W. McPherson, in *IEEE International Reliability Physics Symposium* (IEEE, 2003), pp. 166–172.
- <sup>43</sup>M. Topsakal, H. Sahin, and S. Ciraci, *Phys. Rev. B* **85**, 155445 (2012).
- <sup>44</sup>H. S. Sen, H. Sahin, F. M. Peeters, and E. Durgun, *J. Appl. Phys.* **116**, 083508 (2014).
- <sup>45</sup>S. Chen, L. Brown, M. Levendorf, W. Cai, S. Ju, J. Edgeworth, X. Li, C. W. Magnuson, A. Velamakanni, R. D. Piner, J. Kang, J. Park, and R. S. Ruoff, *ACS Nano* **5**, 1321 (2011).
- <sup>46</sup>L. Shi, R. Wang, H. Zhai, Y. Liu, L. Gao, and J. Sun, *Phys. Chem. Chem. Phys.* **17**, 4231 (2015).
- <sup>47</sup>M. W. Lane, E. G. Liniger, and J. R. Lloyd, *J. Appl. Phys.* **93**, 1417 (2003).
- <sup>48</sup>R. Chan, T. N. Arunagiri, Y. Zhang, O. Chyan, R. M. Wallace, M. J. Kim, and T. Q. Hurd, *Electrochem. Solid-State Lett.* **7**, G154 (2004).
- <sup>49</sup>S. Shingubara, T. Wang, T. Ida, H. Sakaue, and T. Takahagi, in *IEEE International Interconnect Technology Conference* (IEEE, 2002), p. 176.
- <sup>50</sup>C. Lo, H. Li, W. Ge, C. H. Naylor, X. Zhao, Y. Liu, K. L. Lin, and Z. Chen, in *IEEE International Interconnect Technology Conference* (IEEE, 2019).
- <sup>51</sup>H. Li, A. Iqbal, and J. D. Brooks, *J. Mater. Res.* **30**, 3065 (2015).
- <sup>52</sup>H. Li, T. Y. Tsui, and J. J. Vlassak, *J. Appl. Phys.* **106**, 033503 (2009).
- <sup>53</sup>B. Wang and T. Sigmund, *Microelectron. Eng.* **85**, 477 (2008).
- <sup>54</sup>R. Mehta, S. Chugh, and Z. Chen, *Nano Lett.* **15**, 2024 (2015).
- <sup>55</sup>T. Shen, D. Valencia, Q. Wang, K. Wang, M. Povolotskiy, M. J. Kim, G. Klimeck, Z. Chen, and J. Appenzeller, *ACS Appl. Mater. Interfaces* **11**, 28345 (2019).
- <sup>56</sup>R. L. Graham, G. B. Alers, T. Mountsier, N. Shamma, S. Dhuey, S. Cabrini, R. H. Geiss, D. T. Read, and S. Peddeti, *Appl. Phys. Lett.* **96**, 042116 (2010).
- <sup>57</sup>W. Steinhilg, G. Schindler, G. Steinlesberger, and M. Engelhardt, *Phys. Rev. B* **66**, 075414 (2002).
- <sup>58</sup>F. Zahid, Y. Ke, D. Gall, and H. Guo, *Phys. Rev. B* **81**, 045406 (2010).
- <sup>59</sup>S. M. Rossnagel and T. S. Kuan, *J. Vac. Sci. Technol. B* **22**, 240 (2004).
- <sup>60</sup>N. T. Cuong and S. Okada, *Appl. Phys. Lett.* **110**, 131601 (2017).
- <sup>61</sup>C. L. Lo, S. Zhang, T. Shen, J. Appenzeller, and Z. Chen, in *Device Research Conference* (IEEE, 2017).
- <sup>62</sup>R. Zhao, C. Lo, F. Zhang, R. K. Ghosh, T. Knobloch, M. Terrones, Z. Chen, and J. Robinson, *Adv. Mater. Interfaces* **6**, 1901055 (2019).
- <sup>63</sup>C. Lo, K. Zhang, J. A. Robinson, and Z. Chen, in *International Symposium on VLSI-TSA* (IEEE, 2018).
- <sup>64</sup>G. S. Chen, P. Y. Lee, and S. T. Chen, *Thin Solid Films* **353**, 264 (1999).
- <sup>65</sup>H.-C. Chung and C.-P. Liu, *Surf. Coat. Technol.* **200**, 3122 (2006).
- <sup>66</sup>Y. Shi, H. Li, and L.-J. Li, *Chem. Soc. Rev.* **44**, 2744 (2015).
- <sup>67</sup>S. Chugh, R. Mehta, N. Lu, F. D. Dios, M. J. Kim, and Z. Chen, *Carbon* **93**, 393 (2015).
- <sup>68</sup>J. Kwak, J. H. Chu, J.-K. Choi, S.-D. Park, H. Go, S. Y. Kim, K. Park, S.-D. Kim, Y.-W. Kim, E. Yoon, S. Kodambaka, and S.-Y. Kwon, *Nat. Commun.* **3**, 645 (2012).
- <sup>69</sup>C. S. Lee, C. S. Cojocaru, W. Moujahid, B. Lebental, M. Chaigneau, M. Châtelet, F. Le Normand, and J. L. Maurice, *Nanotechnology* **23**, 265603 (2012).
- <sup>70</sup>C. Ahn, J. Lee, H. U. Kim, H. Bark, M. Jeon, G. H. Ryu, Z. Lee, G. Y. Yeom, K. Kim, J. Jung, Y. Kim, C. Lee, and T. Kim, *Adv. Mater.* **27**, 5223 (2015).
- <sup>71</sup>C. J. Perini, M. J. Muller, B. K. Wagner, and E. M. Vogel, *J. Vac. Sci. Technol. B* **36**, 031201 (2018).
- <sup>72</sup>K. K. H. Smithe, C. D. English, S. V. Suryavanshi, and E. Pop, *2D Mater.* **4**, 011009 (2017).
- <sup>73</sup>A. E. Kaloyeros and E. Eisenbraun, *Annu. Rev. Mater. Sci.* **30**, 363 (2000).
- <sup>74</sup>J. Tao, J. Chai, X. Lu, L. M. Wong, T. I. Wong, J. Pan, Q. Xiong, D. Chi, and S. Wang, *Nanoscale* **7**, 2497 (2015).
- <sup>75</sup>J.-H. Huang, K.-Y. Deng, P.-S. Liu, C.-T. Wu, C.-T. Chou, W.-H. Chang, Y.-J. Lee, and T.-H. Hou, *Adv. Mater. Interfaces* **4**, 1700157 (2017).
- <sup>76</sup>L. K. Tan, B. Liu, J. H. Teng, S. Guo, H. Y. Low, and K. P. Loh, *Nanoscale* **6**, 10584 (2014).
- <sup>77</sup>G. Jin, C.-S. Lee, X. Liao, J. Kim, Z. Wang, O. Francis, N. Okello, B. Park, J. Park, C. Han, H. Heo, J. Kim, S. H. Oh, S.-Y. Choi, H. Park, and M.-H. Jo, *Sci. Adv.* **5**, 1 (2019).
- <sup>78</sup>C. Martella, L. Ortolani, E. Cianci, A. Lamperti, V. Morandi, and A. Molle, *Nano Res.* **12**, 1851 (2019).
- <sup>79</sup>C.-K. Hu, L. Gignac, R. Rosenberg, E. Liniger, J. Rubino, C. Sambucetti, A. Domenicucci, X. Chen, and A. K. Stamper, *Appl. Phys. Lett.* **81**, 1782 (2002).
- <sup>80</sup>C.-K. Hu, L. Gignac, E. Liniger, B. Herbst, D. L. Rath, S. T. Chen, S. Kaldor, A. Simon, and W.-T. Tseng, *Appl. Phys. Lett.* **83**, 869 (2003).
- <sup>81</sup>J. P. Tidman, and R. F. Frindt, *Can. J. Phys.* **54**, 2306 (1976).
- <sup>82</sup>J. P. Tidman, O. Singh, A. E. Curzon, and R. F. Frindt, *Philos. Mag.* **30**, 1191 (1974).
- <sup>83</sup>D. Svetin, I. Vaskivskiy, S. Brazovskii, and D. Mihailovic, *Sci. Rep.* **7**, 46048 (2017).
- <sup>84</sup>S. M. Rossnagel, *J. Vac. Sci. Technol. B* **20**, 2328 (2002).
- <sup>85</sup>L. F. Mattheiss, *Phys. Rev. B* **8**, 3719 (1973).
- <sup>86</sup>I. Ciofi, A. Contino, P. J. Roussel, R. Baert, V.-H. Vega-Gonzalez, K. Croes, M. Badaroglu, C. J. Wilson, P. Raghavan, A. Mercha, D. Verkest, G. Groeseneken, D. Mocuta, and A. Thean, *IEEE Trans. Electron Devices* **63**, 2488 (2016).
- <sup>87</sup>J. Lienig and M. Thiele, *Fundamentals of Electromigration-Aware Integrated Circuit Design* (Springer, 2018).



- <sup>88</sup>C.-C. Yang, F. Baumann, P.-C. Wang, S. Lee, P. Ma, J. Aubuchon, and D. Edelstein, *IEEE Electron Device Lett.* **32**, 560 (2011).
- <sup>89</sup>L. Li, Z. Zhu, T. Wang, J. A. Currivan-Incorvia, A. Yoon, and H. S. P. Wong, in *International Electron Devices Meeting* (IEEE, 2016), pp. 9.5.1–9.5.4.
- <sup>90</sup>L. Li, Z. Zhu, A. Yoon, and H. P. Wong, *IEEE Electron Device Lett.* **40**, 815 (2019).
- <sup>91</sup>P.-C. Wang and R. G. Filippi, *Appl. Phys. Lett.* **78**, 3598 (2001).
- <sup>92</sup>S. Beyne, O. V. Pedreira, H. Oprins, I. De Wolf, Z. Tokei, and K. Croes, *IEEE Trans. Electron Devices* **66**, 5278 (2019).
- <sup>93</sup>T. Z. Lin, B. T. Kang, M. H. Jeon, C. Huffman, J. H. Jeon, S. J. Lee, W. Han, J. Y. Lee, S. H. Lee, G. Y. Yeom, and K. N. Kim, *ACS Appl. Mater. Interfaces* **7**, 15892 (2015).
- <sup>94</sup>Y. Sha, S. Xiao, X. Zhang, F. Qin, and X. Gu, *Appl. Surf. Sci.* **411**, 182 (2017).
- <sup>95</sup>L. S. Hui, E. Whiteway, M. Hilke, and A. Turak, *Carbon* **125**, 500 (2017).
- <sup>96</sup>N. Bekiaris, Z. Wu, H. Ren, M. Naik, J. H. Park, M. Lee, T. H. Ha, W. Hou, J. R. Bakke, M. Gage, Y. Wang, and J. Tang, in *IEEE International Interconnect Technology Conference* (IEEE, 2017).
- <sup>97</sup>H. Ren, Z. Wu, N. Bekiaris, J. Tseng, G. How, X. Xie, W. Lei, R. Tao, R. Shaviv, J. J. Lee, R. Vinnakota, K. Kashefzadeh, M. Gage, and M. Naik, in *IEEE International Interconnect Technology Conference* (IEEE, 2018), pp. 166–168.
- <sup>98</sup>M. H. Van Der Veen, N. Heylen, O. V. Pedreira, I. Ciofi, S. Decoster, V. V. Gonzalez, N. Jourdan, H. Struyf, K. Croes, C. J. Wilson, and Z. Tókei, in *IEEE International Interconnect Technology Conference* (IEEE, 2018), pp. 172–174.
- <sup>99</sup>C. Adelman, K. Sankaran, S. Dutta, A. Gupta, S. Kundu, G. Jamieson, K. Moors, N. Pinna, I. Ciofi, S. Van Elshocht, J. Bömmels, G. Boccardi, C. J. Wilson, G. Pourtois, and Z. Tókei, in *IEEE International Interconnect Technology Conference* (IEEE, 2018), pp. 154–156.
- <sup>100</sup>C.-K. Hu, J. Kelly, J. H.-C. Chen, H. Huang, Y. Ostrovski, R. Patlolla, B. Peethala, P. Adusumilli, T. Spooner, L. M. Gignac, J. Bruley, C. Breslin, S. A. Cohen, G. Lian, M. Ali, R. Long, Jr., G. Hornicek, T. Kane, V. Kamineni, X. Zhang, F. Mont, and S. Siddiqui, in *IEEE International Interconnect Technology Conference* (IEEE, 2017).
- <sup>101</sup>S. Dutta, S. Kundu, L. Wen, G. Jamieson, K. Croes, A. Gupta, J. Bömmels, C. J. Wilson, C. Adelman, and Z. Tokei, in *IEEE International Interconnect Technology Conference* (IEEE, 2017).
- <sup>102</sup>X. Zhang, H. Huang, R. Patlolla, F. W. Mont, X. Lin, M. Raymond, C. Labelle, T. Ryan, D. Canaperi, T. E. Standaert, T. Spooner, G. Bonilla, and D. Edelstein, in *IEEE International Interconnect Technology Conference* (IEEE, 2017).
- <sup>103</sup>O. V. Pedreira, K. Croes, A. Leśniewska, C. Wu, M. H. van der Veen, J. de Messemacker, K. Vandersmissen, N. Jourdan, L. G. Wen, C. Adelman, B. Briggs, V. V. Gonzalez, J. Bömmels, and Z. Tókei, in *IEEE International Reliability Physics Symposium Proceedings* (IEEE, 2017), pp. 6B-2.1–6B-2.8.
- <sup>104</sup>D. Tierno, O. V. Pedreira, C. Wu, N. Jourdan, L. Kljucar, Z. Tókei, and K. Croes, *Microelectron. Reliab.* **100–101**, 113407 (2019).
- <sup>105</sup>P. Benech, C.-L. Hsu, G. Ardila, P. Sarafis, and A. G. Nassiopoulou, *Beyond-CMOS Nanodevices 1* (Wiley, 2014), p. 419.
- <sup>106</sup>V. Deshpande, V. Djara, E. O'Connor, P. Hashemi, K. Balakrishnan, M. Sousa, D. Caimi, A. Olziersky, L. Czornomaz, and J. Fompeyrine, in *IEEE International Electron Devices Meeting* (IEEE, 2015), pp. 8.8.1–8.8.4.
- <sup>107</sup>T. E. Kazior, R. Chelakara, W. Hoke, J. Bettencourt, T. Palacios, and H. S. Lee, in *IEEE Compound Semiconductor Integrated Circuit Symposium* (IEEE, 2011).
- <sup>108</sup>P. Sarafis, C.-L. Hsu, P. Benech, and A. G. Nassiopoulou, *IEEE Trans. Electron Devices* **62**, 1537 (2015).
- <sup>109</sup>C.-L. Hsu, G. Ardila, and P. Benech, *Eur. Phys. J. Appl. Phys.* **63**, 14406 (2013).
- <sup>110</sup>C.-L. Hsu, G. Ardila, and P. Benech, in *7th European Microwave Integrated Circuits Conference* (IEEE, 2012), pp. 488–491.
- <sup>111</sup>T. Quémerais, L. Moquillon, J. M. Fournier, and P. Benech, *IEEE Trans. Microwave Theory Tech.* **58**, 2426 (2010).
- <sup>112</sup>G. Kresse and J. Furthmüller, *Comput. Mater. Sci.* **6**, 15 (1996).
- <sup>113</sup>G. Kresse and J. Furthmüller, *Phys. Rev. B* **54**, 11169 (1996).
- <sup>114</sup>G. Kresse and D. Joubert, *Phys. Rev. B* **59**, 1758 (1999).
- <sup>115</sup>P. E. Blochl, *Phys. Rev. B* **50**, 17953 (1994).
- <sup>116</sup>J. P. Perdew, K. Burke, and M. Ernzerhof, *Phys. Rev. Lett.* **77**, 3865 (1996).
- <sup>117</sup>S. Grimme, *J. Comput. Chem.* **27**, 1787 (2006).
- <sup>118</sup>G. Henkelman, B. P. Uberuaga, and H. Jo, *J. Chem. Phys.* **113**, 9901 (2000).