On the Effects of Voltage Loop in Paralleled Converters Under Master-Slave Current Sharing

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***Abstract*— This paper studies the effects of the presence of voltage loops in parallel connected buck switching converters under master-slave current sharing scheme. The system employs a typical proportional-integral (PI) controller for regulation. Comparisons are made for the cases where the slave modules are controlled with and without a voltage loop. Generally, we find that the voltage loop in the slave is helpful in widening the stability range though it is theoretically redundant for the purpose of controlling the output voltage in the small-signal sense. Such a loop provides stable current reference for the slave modules. Effectively, each slave module is under current-mode control by virtue of the current sharing loop, making it a current source. Simulation results under different control configurations are presented to demonstrate the phenomenon.**

I. Introduction

Power supplies based on paralleling switching converters offer a few advantages over a single, high-power, centralized power supply. They enjoy low component stresses, increased reliability, ease of maintenance and repair, improved thermal management, etc. [1], [2]. Paralleling of standardized converters is an approach used widely in distributed power systems for both front-end and load converters. Since current sharing has to be maintained among the paralleled converters, some form of control has to be used to equalize the individual currents in the converters. One widely used method for balancing currents is the *master-slave current sharing* method [3], [4].

For paralleled converters, we have to control the current distribution as well as the output voltage. Typically, it contains a main voltage loop and a current sharing loop in voltage mode control; alternatively there may be a main voltage loop, a current loop and a current sharing loop in current mode control. The dynamic behavior becomes complex in N-paralleled converters because of the interaction between these loops. Intuitively, the main voltage loop is necessary for regulating the output voltage as in a stand-alone converter. The current sharing loop helps to regulate the reference voltage to get the expected output [4], [5], [6], [7]. However, all outputs of the converters are connected to one node (the load side). From circuit theory, paralleled branches should behave like current sources with large output impedance in order to ensure stable operation [8], [9]. Consequently, one voltage loop is enough to control the output voltage for the paralleled system. In the master-slave current sharing system, the master will control the output voltage and the slaves are required to follow the current of the master.

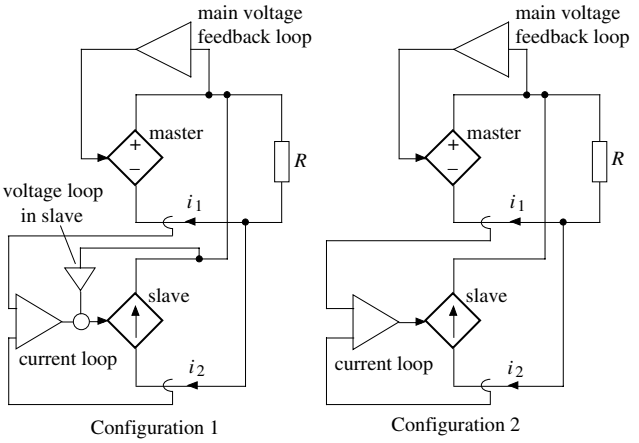

Fig. 1. Master-slave parallel system. Configuration 1: voltage loop in slave. Configuration 2: no voltage loop in slave

For simplicity, the system under study in this paper is a parallel connected system of two buck converters. Under the master-slave scheme, one of the converters is the master and the other is the slave. The master has a main feedback loop consisting of a typical proportional-integral (PI) control, to regulate the output voltage. The slave basically sets its current to equal that of the master via an active loop involving comparison of the currents of the two converters.

In this paper, we will study the effects of the slave's voltage loop and compare the stability boundaries of feedback parameters with and without the voltage loop in the slave converter. We find that the stable region in the parameter space can be larger when the slave converter contains a voltage loop. The voltage loop in the slave converter is therefore useful. The role of it is not to control the output voltage directly, but to provide a stable current reference for the slave. Furthermore, we confirm that as the slave converter is under current mode control with current sharing feedback, it behaves effectively as a current source.

II. System Description and Operation

Figure 1 shows the circuit model of two paralleled buck converters under master-slave control. Configuration 1 incorporates an additional voltage loop in the slave, whereas Configuration has no such a loop. Figure 2 (a) is the converter circuit, Figs 2 (b) and (c) form the control circuit for

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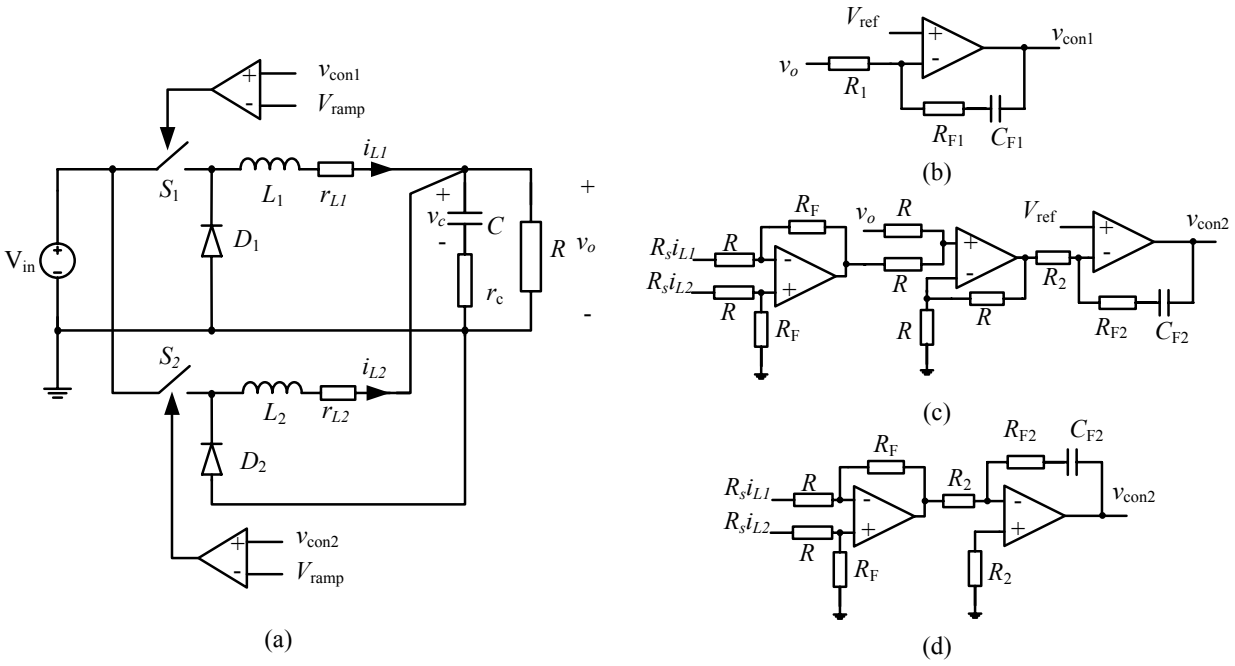


Fig. 2. Paralleled buck converters under master-slave current sharing and PI control. (a) Power stage; (b) controller for the master; (c) controller for the slave with voltage loop; (d) controller for the slave without voltage loop.

Configuration 1, and Figs. 2 (b) and (d) form the control circuit for Configuration 2.

In this circuit, S_1 and S_2 are switches, which are controlled by a standard pulse-width modulator consisting of a comparator comparing a control signal and a ramp signal. The ramp signal is given by [10]

$$V_{\rm ramp} = V_L + (V_U - V_L)\left(\frac{t}{T_s} \bmod 1\right) \tag{1}$$

where V_L and V_U are the lower and upper thresholds of the ramp, respectively, and T_s is the switching period. Basically, switch S_i $(i = 1, 2)$ is closed if $v_{{\rm con}i} > V_{\rm ramp}$ and is open otherwise.

The control signals $v_{\rm con1}$ and $v_{\rm con2}$ are derived from the feedback compensator, as shown in Figs. 2 (b) and (c). Here the compensator is a PI controller, i.e.,

$$\frac{V_{\rm con1}(s)}{E(s)} = -K_p\left(1 + \frac{1}{T_i s}\right) \tag{2}$$

where $V_{\rm con1}(s)$ and $E(s)$ are the Laplace transforms of $v_{\rm con1}(t)$ and $e(t)$; $e(t)$ is the error between reference and output; K_p and T_i are the control parameters. With respect to the slave, an extra current sharing signal is included. We can likewise derive the equation.

We assume that the converter operates in continuous conduction mode (CCM) and diodes D_1 and D_2 are always in complementary state to S_1 and S_2. Consequently, the state equations of the converter stage of Fig. 2 are

$$\begin{cases} \dot{x}_1 = -\frac{1}{L1}[(r_{L1} + \frac{Rr_c}{R+r_c})x_1 + \frac{Rr_c}{R+r_c}x_2 + \frac{R}{R+r_c}x_3 - q_1 V_{in}] \\ \dot{x}_2 = -\frac{1}{L2}[\frac{Rr_c}{R+r_c}x_1 + (r_{L2} + \frac{Rr_c}{R+r_c})x_2 + \frac{R}{R+r_c}x_3 - q_2 V_{in}] \\ \dot{x}_3 = \frac{1}{C(R+r_c)}(Rx_1 + Rx_2 - x_3) \end{cases} \tag{3}$$

where x_1, x_2, x_3 are the converter state variables defined as

$$[x_1 \;\; x_2 \;\; x_3] = [i_{L1} \;\; i_{L2} \;\; v_c] \tag{4}$$

and q_1 and q_2 are the switching function decided by the controllers. They are time varying functions given by

$$q_i(t) = \begin{cases} 1, & \text{if } v_{{\rm con}i} \geq V_{\rm ramp}, \\ 0, & \text{if } v_{{\rm con}i} < V_{\rm ramp}. \end{cases} \tag{5}$$

According to the feedback circuit in Figs. 2 (b), (c) and (d), we can derive the control equations. For Configuration 1, we have

$$\frac{dv_{\rm con1}}{dt} = -K_1\frac{dv_o}{dt} - \frac{K_1}{\tau_{F1}}v_o + \frac{K_1}{\tau_{F1}}V_{\rm ref} \tag{6}$$

$$\frac{dv_{\rm con2}}{dt} = -K_2\frac{dv_o}{dt} - \frac{K_2}{\tau_{F2}}v_o + K_2K_i(\frac{di_{L1}}{dt} - \frac{di_{L2}}{dt}) + \frac{K_2K_i}{\tau_{F2}}(i_{L1} - i_{L2}) + \frac{K_2}{\tau_{F2}}V_{\rm ref} \tag{7}$$

and for Configuration 2, we have

$$\frac{dv_{\rm con1}}{dt} = -K_1\frac{dv_o}{dt} - \frac{K_1}{\tau_{F1}}v_o + \frac{K_1}{\tau_{F1}}V_{\rm ref} \tag{8}$$

$$\frac{dv_{\rm con2}}{dt} = K_2K_i(\frac{di_{L1}}{dt} - \frac{di_{L2}}{dt}) + \frac{K_2K_i}{\tau_{F2}}(i_{L1} - i_{L2}). \tag{9}$$

Also, v_o can be written as

$$v_o = v_c + r_c i_c = v_c + r_c(i_{L1} + i_{L2} - \frac{v_o}{R}) \qquad (10)$$

where K_1 and K_2 are the proportional gains, τ_{F1} and τ_{F2} are the integral coefficients, K_i is the current sharing gain, and V_{ref} is the reference voltage (expected output voltage). In circuit terms, $K_1 = R_{F1}/R_1$, $\tau_{F1} = R_{F1}C_{F1}$, $K_2 = R_{F2}/R_2$, $\tau_{F2} = R_{F2}C_{F2}$, $K_i = R_F R_s/R$, where R_s is the current sensing resistance. Equations (6) and (7), together with (3), form the complete set of state equations for Configuration 1 and equations (8), (9) and (3) for Configuration 2.

III. Simulation Results

The simulations performed using the state equations derived in the foregoing section and hence are exact cycle-by-cycle simulations. We are primarily concerned with the system stability in relation to the feedback parameters of the PI controller, i.e., K_1, K_2, τ_{F1}, τ_{F2}. We assume that the inductances in the converters are generally different and fix the current sharing parameter at $K_i = 1$. The circuit parameters and component values are listed in Table I.

TABLE I
Component Values Used in Simulations

Circuit Components	Values
Switching Period T_s	10 μs
Input Voltage V_{in}	12 V
Reference Voltage V_{ref}	5 V
Ramp Voltage V_L,V_U	0 V, 2 V
Inductance L_1, ESR r_{L1}	55 μH, 0.01 Ω
Inductance L_2, ESR r_{L2}	110 μH, 0.05 Ω
Capacitance C, ESR r_c	126 μF, 0.01 Ω
Load Resistance R	0.5 Ω
Current sensing Resistance R_s	0.01 Ω

Firstly, we fix the control parameters of the master, K_1 and $1/\tau_{F1}$, and identify the stable region in the space of K_2 and $1/\tau_{F2}$. Figure 3 shows the stability boundary in the space of K_2 and $1/\tau_{F2}$ for different values of K_1 and $1/\tau_{F1}$. Then, we fix the control parameters of the slave, K_2 and $1/\tau_{F2}$, and identify the stability boundary in the space of K_1 and $1/\tau_{F1}$. Figure 4 shows the stability boundary in the space of K_1 and $1/\tau_{F1}$.

From Fig. 3, we may conclude that when the master is fixed, the maximum stable value of K_2 is more or less unchanged regardless of variation of $1/\tau_{F2}$ for both Configurations 1 and 2. Moreover, the maximum values of K_2 are unaffected by the parameters of the master when it operates in a stable region. In a previous publication [11], it has been shown that for stand-alone converters, the stable range of proportional gain K diminishes rapidly as the integral time constant parameter $1/\tau_F$ increases in the voltage mode control, which is clearly different from the results shown in Fig. 3. We can explain this phenomenon in terms of the characteristic of current-mode control. When under average current-mode control, the buck converter shows a single-pole

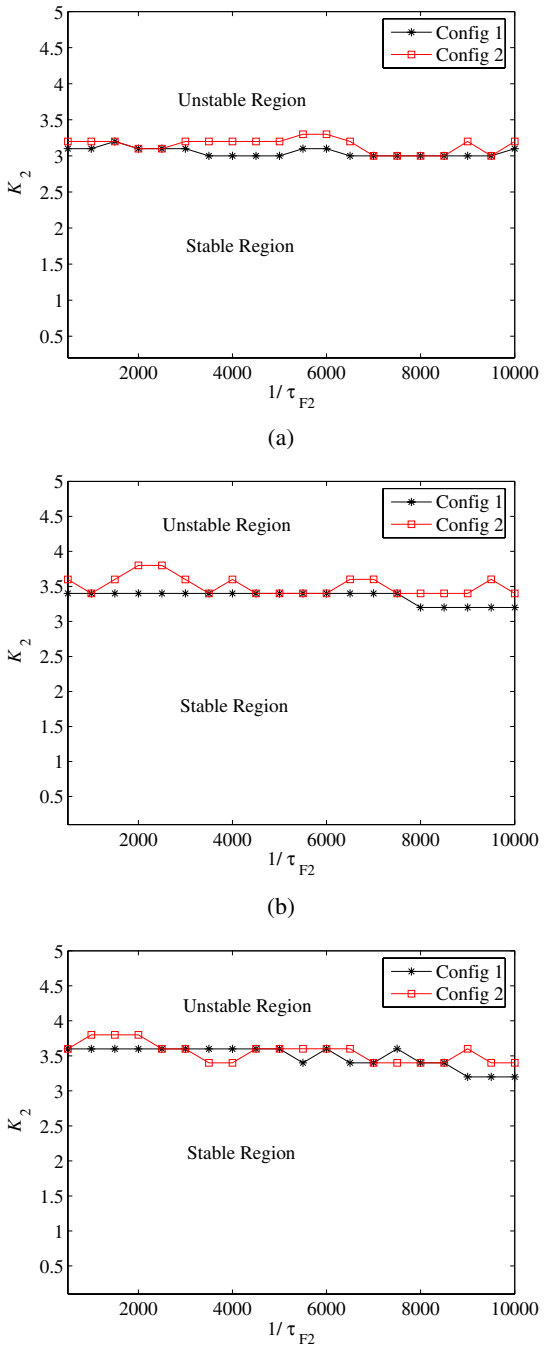
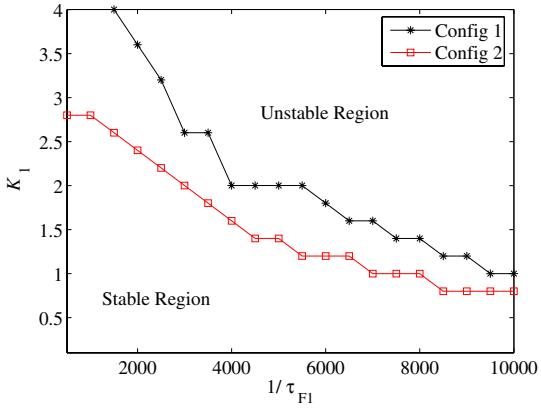
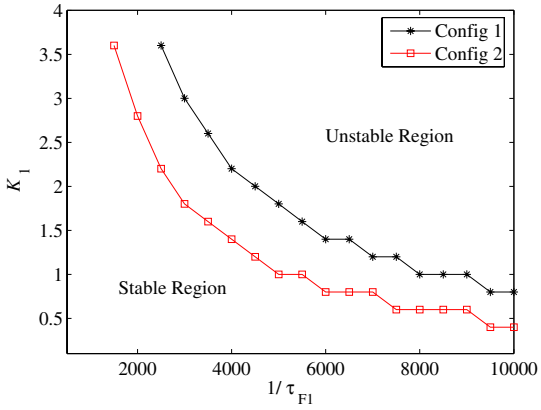


Fig. 3. Stability boundaries of feedback parameters for Configuration 1 and Configuration 2. (a) $K_1 = 1, 1/\tau_{F1} = 1000$; (b) $K_1 = 0.2, 1/\tau_{F1} = 1000$; (c) $K_1 = 0.2, 1/\tau_{F1} = 10000$.

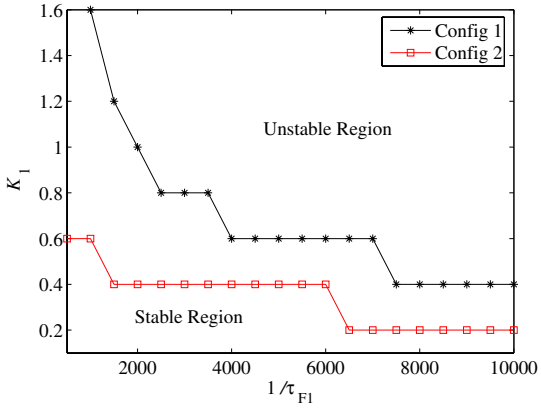
behavior since the inductor has been controlled by the current feedback. The unstable behavior is caused by saturation, i.e., the control signal overruns the range of the ramp signal. In the paralleled system, since the slave is effectively under current-mode control, the stable range of proportional control gain K_2 will not be affected by the variation of $1/\tau_{F2}$. The current sharing feedback makes the slave a current source in both



(a)



(b)

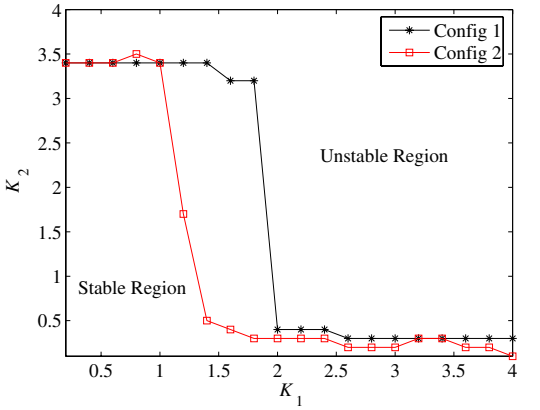


(c)

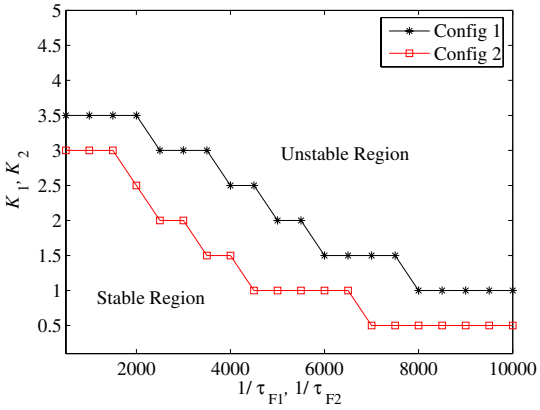
Fig. 4. Stability boundaries of feedback parameters for Configuration 1 and Configuration 2. (a) $K_2 = 3, 1/\tau_{F2} = 5000$; (b) $K_2 = 0.3, 1/\tau_{F2} = 5000$; (c) $K_2 = 0.3, 1/\tau_{F2} = 20000$.

Configurations 1 and 2 when the master is fixed.

From Fig. 4, we observe that the stable range of K_1 decreases greatly as the value of $1/\tau_{F1}$ increases, which is consistent with the characteristic of voltage-mode controlled buck converters, for both Configurations 1 and 2 when the slave is fixed. And the stability boundary in Configuration 1 is always larger than that in Configuration 2. Moreover, K_2



(a)



(b)

Fig. 5. Stability boundaries of feedback parameters for Configuration 1 and Configuration 2. (a) $1/\tau_{F1} = 1/\tau_{F2} = 2000$; (b) $K_1 = K_2, 1/\tau_{F1} = 1/\tau_{F2}$.

and $1/\tau_{F2}$ affect the stable region in the plane of K_1–$1/\tau_{F1}$, as shown in Figs. 4 (a), (b) and (c). The larger K_2 and $1/\tau_{F2}$ are, the smaller the stable region.

Figure 5 (a) shows the stability boundary of K_1 versus K_2 for $1/\tau_{F1} = 1/\tau_{F2} = 2000$. When K_1 is small, K_2 has a large stable range, but when it becomes large, the stable range of K_2 falls rapidly. Figure 5 (b) shows the stability boundary when the feedback parameters of the master and slave are changed simultaneously. Again, the stable region for Configuration 2 is smaller than that for Configuration 1.

Based on the stability boundaries of the feedback parameters, we can identify the parameter range for stable operation. Also, we want to know the relationship between the input voltage and feedback parameters. Figure 6 shows the input voltage range for different values of K_1 and K_2. We observe that when K_1 is small (e.g. $K_1 = 0.2$), the stability boundaries are almost identical in the plane of K_2–V_{in} for Configurations 1 and 2, as shown in Fig. 6 (b) and (c). Also, the stable region diminishes greatly in the plane of K_1–V_{in} as K_2 increases from Fig. 6 (d) and (e). Furthermore, if K_1 and K_2 change simultaneously, the system can be operated under

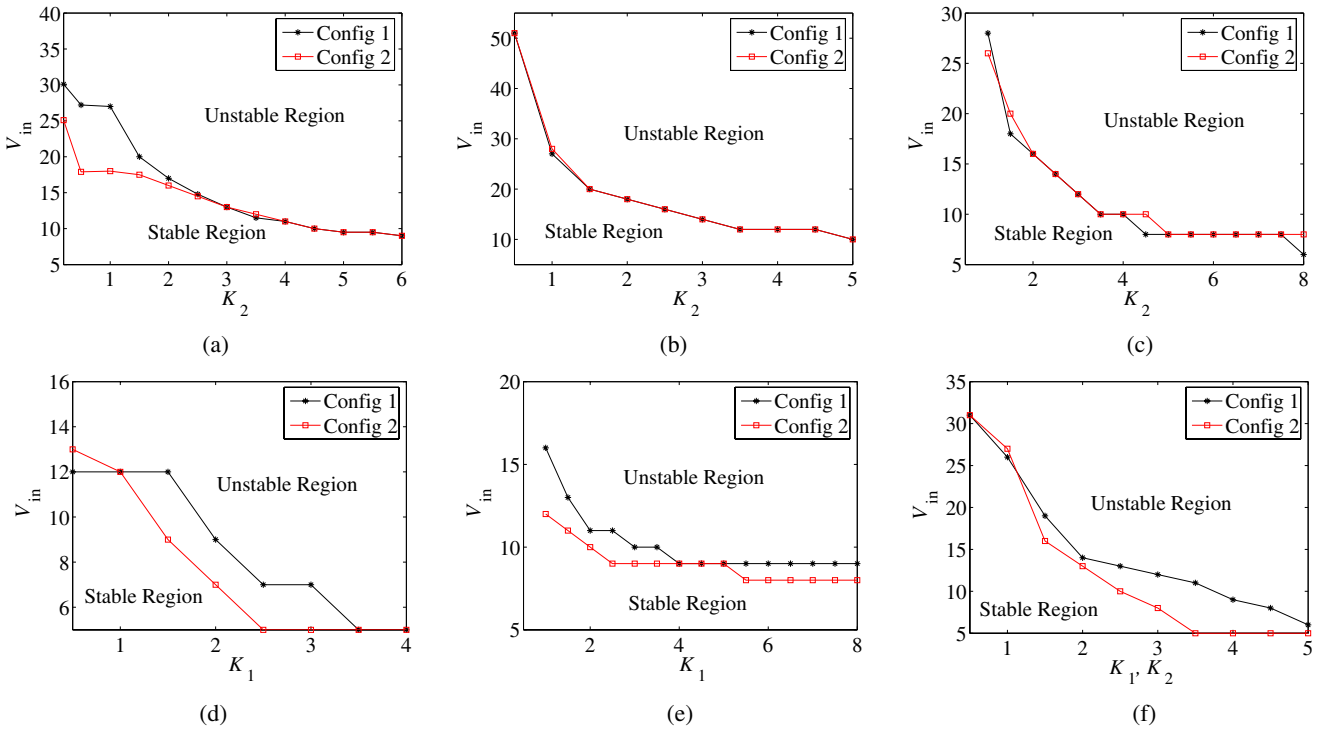


Fig. 6. Stability boundaries of $V_{\rm in}$ versus feedback parameters for Configuration 1 and Configuration 2. (a) $K_1 = 2, 1/\tau_{F1} = 1/\tau_{F2} = 1000$; (b) $K_1 = 0.2, 1/\tau_{F1} = 1000, 1/\tau_{F2} = 2000$; (c) $K_1 = 0.2, 1/\tau_{F1} = 1000, 1/\tau_{F2} = 10000$; (d) $K_2 = 3, 1/\tau_{F1} = 1/\tau_{F2} = 5000$; (e) $K_2 = 0.3, 1/\tau_{F1} = 1/\tau_{F2} = 5000$; (f) $1/\tau_{F1} = 1/\tau_{F2} = 2000$.

a wide range of input voltage when K_1 and K_2 are small. Comparing the stability boundaries in Fig. 6, we know that the stable input voltage range for Configuration 2 is smaller than that for Configuration 1.

IV. Conclusion

In the paper, we study the effects of feedback parameters in paralleled buck converters under a master-slave current sharing control. In particular we consider the effects of the inclusion of a voltage feedback loop in the control of the slave in addition to the current sharing loop. In general, we find that the system's stability range is wider with a voltage loop in the slave. Therefore, we may conclude that the voltage feedback in the slave converter is useful in enlarging the stable operation range. However, the role of this voltage loop is not to control the output voltage directly, but to provide a better regulated current reference for the slave. In brief, the slave gets a more stable current reference under a wider parameter range. Furthermore, we note that the slave converter is under current-mode control with the current sharing feedback, behaving effectively as a current source which should be expected in paralleled converters.

Acknowledgment

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