Time-dependent transport characteristics of graphene tuned by ferroelectric polarization and interface charge trapping

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ABSTRACT: Graphene-based field effect transistors (FETs) were fabricated by employing ferroelectric $Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ (PMN-PT) as a gate insulator. The co-existing effects of ferroelectric gating and interface charge trapping on the transport properties of graphene were investigated with respect to the FET structure. The sheet resistance (R_s) of graphene shows a slight decay under a small applied voltage, which is much less than the coercive voltage of the ferroelectric PMN-PT, suggesting non-negligible charge trapping effects. Moreover, when the applied voltage is increased up to a value larger than the coercive voltage, R_s exhibits three states: an initial rapid change, followed by a slow nearly exponential evolution, and finally a saturated state either during the applied voltage is retained or after it is released. In particular, a high-resistance state is finally reached due to the ferroelectric gating, implying that ferroelectric effects dominate this process. The underlying physical mechanism was fully investigated to effectively address the observed evolution of time-dependent R_s. Such a finding provides us an opportunity to understand the co-existing effects of ferroelectric gating and charge trapping and tune the transport properties of graphene through the interface effects.

KEYWORDS: graphene, PMN-PT, ferroelectric, polarization, transport properties

INTRODUCTION

Graphene, as a new generation material, has been extensively studied based on the field effect transistor (FET) structures by integrating it with traditional SiO_2, HfO_2, Al_2O_3 and some other high-k dielectrics.[1–3] Among them, ferroelectric materials not only possess a high dielectric constant but also exhibit nonlinear and non-volatile polarization.[4] Consequently, graphene has been widely reported to combine with ferroelectric materials in order to achieve attractive properties and realize non-volatile memory device operations.[5–11] For example, previous studies on graphene/ferroelectric heterostructures have showed that large-area chemical-vapor-deposited (CVD) graphene could reach a high carrier doping level by organic ferroelectric poly(vinylidene fluoride-co-trifluoroethylene) (PVDF-TrFE) gating,[12,13] making graphene show potential for applications in flexible and transparent electrodes to substitute traditional conductive indium tin oxide (ITO). In addition, graphene-based ferroelectric FETs (GFeFETs) by lead zirconate titanate (PZT) gating demonstrated a mobility in excess of 1.5×10^5 cm^2 V^{-1} s^{-1},[9] and a complete conversion of a p-type graphene into n-type through ferroelectric polarization reversal.[14] Moreover, a graphene/ferroelectric tunneling junction with ferroelectric $BiFeO_3$ ultra-thin film as a tunnel layer was reported in our recent study to achieve a ultra-high on/off ratio in graphene based FETs.[15] Furthermore, the ferroelectric nonvolatility and nonlinear polarization can effectively tune the transport properties of the graphene layer and dramatically improve the performance of fabricated devices, such as the non-volatile behaviors used in information storing and hysteresis behaviors in the transport properties.[5,16,17] Actually, the interface charge trapping also can induce the hysteresis in the transport behaviors of FETs, not only for graphene but also other two-dimensional (2D) materials, such as MoS_2.[18–23] Based on some previous studies, there are primarily two factors, which can affect the transport properties of graphene as well as induce

the hysteresis in the transport properties of GFeFETs. First, the ferroelectric polarization can manipulate and dramatically tune the transport properties of graphene through the strong interaction between graphene and the ferroelectric gate.[23–25] The second factor is the charge trapping and de-trapping at the interface between graphene and gate materials, which can induce large hysteresis in the transport curves and tune the performance of the GFeFETs.[25–27] Moreover, the surface adsorbates (*e.g.*, the contaminations, water and oxygen molecules) are found to contribute to the inverse resistance hysteresis, *i.e.*, anti-hysteresis, in the transport properties of GFeFETs. Although some studies have been conducted to separate the intrinsic ferroelectric contributions from the external interaction of surface and/or interface charging and adsorbed molecules,[25,26] it appears to be difficult to exclude the effects of such external factors. The behaviors of graphene are not only tuned by the underlying ferroelectric gating but also affected by the interface charge trapping. Hence, it is essential to understand the coupling mechanism between graphene and the ferroelectric gate, as well as the interface charge trapping effects. The charge trapping and de-trapping processes and the impact of such trapped charges on the transport properties of graphene are intrinsically slow evolutions, which can show an appreciable time-dependent profile. However, the time-dependent transport properties of graphene by ferroelectric gating are rarely reported.[14,28] Very recently, Lipatov et al. reported a detailed analysis of interplay between the ferroelectric polarization and the interfacial charge traps as well as time-dependent measurements in graphene/PZT FETs.[29] However, their study focused on investigating the ferroelectric polarization-dependent electronic transport properties of graphene by minimizing the effect of charge traps. In this study, we employed CVD-grown graphene and ferroelectric $Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ (PMN-PT) to investigate the co-existing effects of ferroelectric polarization and charge traps, in contrast to ruling out or minimizing the charge

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trapping reported in previous studies by other groups. Furthermore, under a gate voltage either smaller or larger than the coercive voltage of the ferroelectric PMN-PT, the time-dependent transport properties exihibted different evolution profiles, suggesting the dominating effects of charge trapping or ferroelectric gating based on our fabricated heterostructures. The strategy of exploring the time-dependent transport properties in this study provides an approach to investigate the co-existing effects of both ferroelectric polarization and charge traps simultaneously.

RESULTS AND DISCUSSION

To fabricate GFeFETs, a monolayer of CVD-grown graphene is transferred onto single-crystal ferroelectric PMN-PT substrate. Fig. 1a shows a typical Raman spectrum of a monolayer of CVD-grown graphene with the feature peaks of G and 2D. The peak position and intensity can be achieved by fitting the specific peak with a single-peak Lorentz function. The 2D band exhibits a symmetrical sharp peak with full-width-at-half maximum (FWHM) of about 40 cm^{-1}. The 2D (centered at about 2700 cm^{-1}) band exhibits approximately 2 times the intensity of the G peak (located at about 1580 cm^{-1}), implying that the CVD-grown graphene is a single-layer.[30,31] In addition to the two feature bands, there are some rough and broad peaks arising from the underlying PMN-PT substrate. Furthermore, Fig. 1b shows the Raman mapping image of G and 2D bands of the graphene over an area of 4 μm × 4 μm. The mapping image reveals that a uniform and continuous graphene layer has been well transferred onto the PMN-PT substrate. Moreover, the defect-related D peak (located at about 1350 cm^{-1}) is not observed either in the Raman spectrum or in the mapping image, indicating the absence of significant defects and the good quality of the transferred graphene. Then, the source and drain electrodes were prepared by thermal evaporation for the following transport measurements as schematically shown in the

inset of Fig. 1a. The device fabrication and characterization are discussed in the Experimental section. Furthermore, monolayer graphene sheets were transferred onto SiO_2/Si substrates and graphene/SiO_2 FETs are fabricated for comparison.
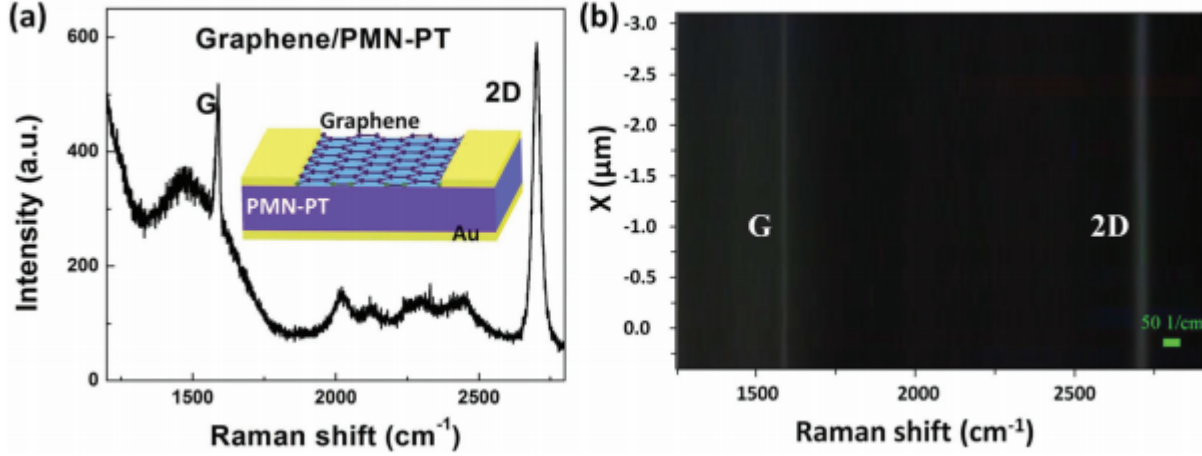

Fig. 1 (a) Raman spectrum of graphene on PMN-PT substrate. The inset shows the schematic of graphene/PMN-PT heterostructure. (b) Raman mapping image of the graphene on PMN-PT substrate with the x axis of Raman shift, y axis of Raman mapping scale X and vertical axis of the Raman spectra intensity.

Then, the transport characteristics of the graphene were systematically studied in the GFeFETs by PMN-PT gating. The sheet resistance (R_s) of graphene is calculated by measuring the drain current (I_{ds}) when a source–drain voltage (V_{ds}) of 0.5 V is biased. Fig. 2 shows the R_s of graphene as a function of the gate voltage (V_g). It is observed that the range of applied V_g is gradually increased from 50 to 100 to 150 V as shown in Fig. 2a, b and c, respectively. From Fig. 2a, it is clear that the R_s decreases with backward sweeping V_g, while it increases with forward sweeping, suggesting that the CVD-grown graphene is p-type in air at room-temperature.

Moreover, a slight hysteresis loop is observed in the resistance curves. Similar p-type characteristics with an on/off ratio of about 3 can be observed for graphene layers on both PMN-PT and SiO$_2$ when the range of V_g increases up to 100 V as shown in Fig. 2b and d, respectively. A relatively large hysteresis loop is observed in graphene on PMN-PT compared to that on SiO$_2$. It should be pointed out that the charge concentration and resistivity of graphene primarily depend on the dielectric gate materials. To be more specific, the doping concentration is proportional to the dielectric constant of the gating insulator, while varying in inverse ratio to its thickness under the same V_g. Although the room-temperature dielectric constant of PMN-PT (~5000) is over 3 orders-of-magnitude higher than that of SiO$_2$ (~3.9), the thickness of PMN-PT (0.5 mm) is over 1000 times higher than that of SiO$_2$ (300 nm). Therefore, it is understandable that the E doping effects on graphene by PMN-PT or SiO$_2$ gating are comparable under identical V_g. Accordingly, R_s of graphene on the PMN-PT is slightly smaller than that on SiO$_2$. For the V_g range up to 150 V, graphene on SiO$_2$ still shows similar transport behaviors. In our experiments, the transport properties of graphene were measured at room-temperature in air ambient. The fabricated FETs exposed to the laboratory environment were always found to be initially p-type due to the adsorbed molecules in air ambient.[32] The Dirac point, located at about 130 V, can be observed in graphene/SiO$_2$ FETs when the gate voltage is increased to 150 V as shown in the inset of Fig. 2d. However, for graphene on PMN-PT, the backward and forward scans of R_s show the typical ferroelectric butterfly-shape hysteresis loop when the V_g range is up to 150 V as shown in Fig. 2c. The ferroelectric polarization field in PMN-PT can contribute to the adjacent graphene layer with electrons or holes depending on the applied V_g or polarization direction. As a consequence, the hysteresis in ferroelectric polarization can offset the Dirac point and induce the butterfly-shape hysteresis in R_s of graphene with backward and forward sweeping V_g. Although

the fabricated GFeFETs exhibit asymmetry in the hysteresis, reproducible and consistent behaviors are achieved as illustrated in Fig. 2c. This can be caused by some additional doping of water and oxygen from the air as aforementioned. Moreover, in the transport measurements, the V_g was swept from the positive maximum to the negative minimum, and then followed by forward sweeping with a time gap between the backward and forward sweeping. There could be a slight difference in the resistance for backward and forward sweeping due to the nonvolatile ferroelectric polarization; also, the charge trapped at the interface could induce the slight difference in the carrier density as well as the resistance of graphene when V_g is swept in a different direction. Thus, the transport curves are not closed (Fig. 2).
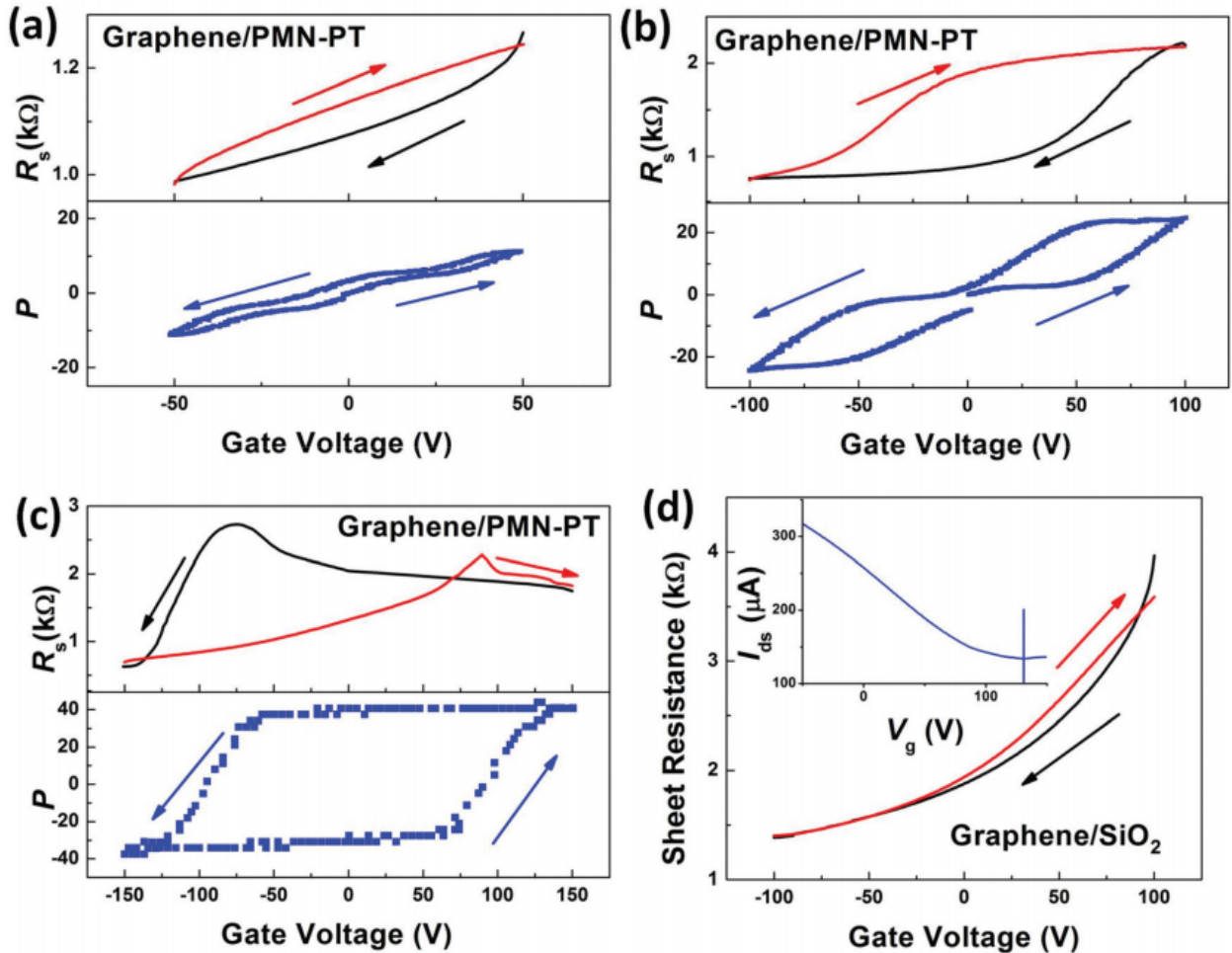
Fig. 2 Sheet resistance of graphene (top panel) on PMN-PT and polarization of PMN-PT crystal (bottom panel) as a function of the gate voltage with the range of (a) 50 V; (b) 100 V; (c) 150 V. (d) Sheet resistance of graphene on SiO_2 as a function of the gate voltage with the range of 100 V. The inset shows the transport properties of graphene on SiO_2 substrate with the gate voltage up to 150 V.

To further understand the correlation between the transport properties of graphene and ferroelectric polarization of PMN-PT, we measured the hysteresis loop of the polarization (P) versus E from the PMN-PT single crystal with graphene serving as top electrode and Au acting as bottom electrode as shown in Fig. 3a. The P of PMN-PT begins changing at about 75 V (E = 1.5 kV cm^{-1}) and saturates at about 150 V with forward sweeping, while the P remains almost constant until −75 V and saturates at −150 V for backward sweeping with the coercive voltage (V_c) of about ±100 V (coercive field, E_c = 2 kV cm^{-1}). To better understand the measured R_s (Fig. 2), we combined P and R_s dependences on V_g for different V_g scale as shown in Fig. 2a, b and c. In graphene/PMN-PT heterostructure, the ferroelectric P of PMN-PT gradually changes depending on V_g with a slight hysteresis loop. The ferroelectric gating modulates the transport properties of graphene as a conventional dielectric of SiO_2 within the V_g regions, where the spontaneous polarization does not reverse, *i.e.*, V_g is less than V_c. The ferroelectric polarization could not be reversed in the V_g range of 50 and 100 V. Herein, the resistance of graphene shows a gradual change when V_g is smaller than the coercive voltage as shown in Fig. 2a and b. As a consequence, the hysteresis loops observed for both devices by PMN-PT or SiO_2 gating are primarily a result of the charge trapping at the interface.[21,33] Moreover, when V_g exceeds V_c, the polarization can be switched. The simultaneous rise in resistance with the reversal of

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ferroelectric polarization is expected at V_c (about 100 V), inducing the hysteresis loop in the resistance behaviors when sweeping V_g in forward and backward directions. It is observed that R_s in graphene shows a consistent hysteresis loop with the polarization loop when V_g is beyond V_c. Furthermore, the Hall effect measurement has been performed for the graphene sample on the PMN-PT substrate. The carrier type and density of graphene on PMN-PT substrates under different gate voltage can be obtained as shown in Fig. 3b. The gate voltages in the range of −200 to 200 V with step of 50 V are applied during the measurements. The black circles represent holes, while the blue circles indicate electrons. The red circles stand for the Dirac points. The green arrows stand for the ramping direction of the gate voltage. The CVD-grown monolayer graphene samples exposed to laboratory environment are initially p-type. The excess hole concentration of graphene on PMN-PT under zero gate is measured to be about 5×10^{12} cm^{-2}, which is slightly larger than that of graphene on SiO_2 (about 2×10^{12} cm^{-2}). The carrier type is changed into electron when the gate voltage is in excess of 100 V. Similar to the ferroelectric hysteresis in the resistance curve (Fig. 2c), there is a hysteresis in the carrier density of graphene when swithching the gate voltage forward and backward.

Furthermore, it should be noted that the hysteresis direction with the V_g range of 150 V is reversed compared to those with V_g ranges of 50 and 100 V as well as graphene on the SiO_2 substrate. Since the interface charge trapping effect dominates the ferroelectric polarization effect, anti-hysteresis can be observed in the transport properties of GFeFETs.[14,26,29] Similar transport properties caused by the charge trapping effect have been previously observed even in graphene on conventional dielectric materials, which do not exhibit a spontaneous polarization.[21,33] Efforts have been made to eliminate the effect of charge traps on the transport properties of GFeFETs, such as improving the crystalline qualities of the ferroelectric materials

or heating the ferroelectric substrates,[26] avoiding exposure of GFeFETs to air during the transfer and measurement process,[14] or measuring the transport properties after removing the gate voltage.[29] In this study, the reverse of anti-hysteresis was realized by the pre-poling the PMN-PT crystal with V_g of -250 V for 10 min prior to the resistance measurements, resulting in the downward polarization state, *i.e.*, the electric dipole moments in the PMN-PT pointing away from the graphene sheet. Then, the anti-hysteresis behaviors can be reversed when the sweeping V_g was larger than the coercive voltage of PMN-PT. This can be caused by the sharp transition of ferroelectric switching of the PMN-PT crystal. The reversed hysteresis suggests that the ferroelectric polarization can dominate the transport properties of graphene under high gate voltage. Moreover, the extrinsic charge trapping effects also can modify the transport properties of graphene. The evidence is that the Dirac points for forward and backward sweeping shift closer to each other when the sweeping rate is changed from 1 to 10 V s^{-1}. Fig. 3b presents the normalized R_s as a function of V_g with different sweeping rates from 1 to 10 V s^{-1}. For fast ramping, the charge trapping effect should be less significant, hence gating should be more effective. The sweeping rate dependent Dirac point shifts are caused from the time-dependent charge trapping or charge distribution effects at the interface. Therefore, the transport behaviors of graphene gating by ferroelectric PMN-PT are tuned by both the underlying ferroelectric polarization and the interface charge trapping. Clearly, the ferroelectric doping is dominated in the transport behaviors of graphene when the V_g range is in excess of the V_c of PMN-PT. Moreover, it should be mentioned that the Dirac points show little variation at the sweeping speeds below 1 V s^{-1} (not shown here). Actually, not only the Dirac points remain constant but also the transport curves remain unchanged when the sweeping speeds are below 1 V s^{-1}.
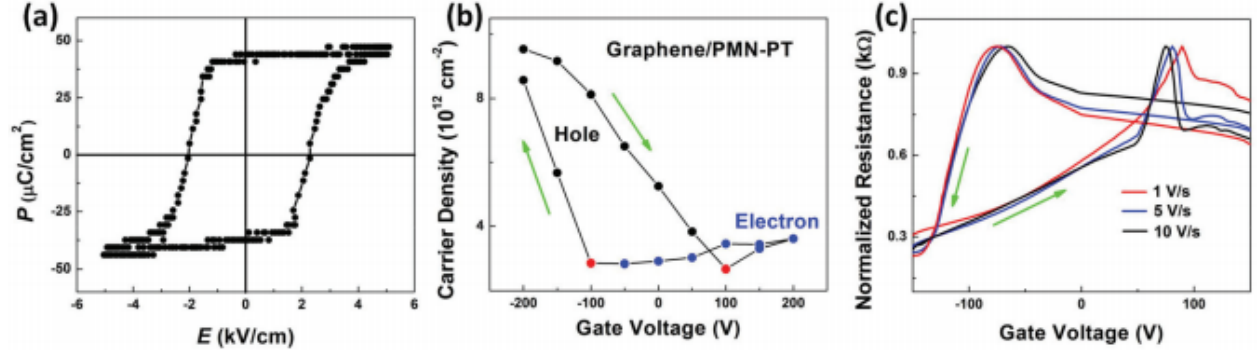
Fig. 3 (a) Polarization versus electric field hysteresis loop of PMN-PT. (b) Charge carrier density of graphene on PMN-PT as a function of the gate voltage. The black circles represent hole while blue circles means electron. The red circles mean the Dirac points. The green arrows stand for the ramping direction of gate voltage. (c) Normalized sheet resistance of graphene as a function of gate voltage with different sweeping rates from 1 to 10 V s^{-1}. The green arrows stand for the ramping direction of gate voltage.

To further explore the co-existing effects of ferroelectric polarization and charge trapping, time-dependent R_s was measured under V_g, which is smaller than V_c. In general, the R_s of graphene should remain invariable under a constant E, while graphene on PMN-PT substrate exhibits time-dependent behaviors as shown in Fig. 4a. The pulse signals with the peak-to-peak voltage of 10 V, *i.e.*, from −5 V to +5 V, are used to serve as the V_g. For comparison, we also measured the resistance response of graphene in graphene/SiO$_2$ heterostructures. Both graphene layers are zero biased for more than 1 h until their resistances reach a stable state. Then, gate pulses were applied and the resistances were measured accordingly. Both resistances were modulated at the same frequency as that of the driving signals (10 mHz), and the positive V_g gives rise to the rapid increase of resistance corresponding to the decrease of carrier

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concentration, while the negative V_g leads to the dramatic decrease in resistance. The observed characteristics are in accordance with the p-type transport properties of graphene. Moreover, there is a slight and negligible change in the resistance during the retention of both positive and negative gate voltages for graphene/SiO$_2$ system caused by the time-dependent interface charge trapping effect. However, the resistance for graphene on PMN-PT shows a gradual evolution under the small V_g, which is much less than V_c. To understand the unique behaviors for graphene on PMN-PT, the surface morphology of the PMN-PT substrate and the as-fabricated graphene were characterized using an atomic force microscope (AFM) (Fig. 4b). It is known that single-crystal PMN-PT possesses a rhombohedral structure and its spontaneous polarization points to the (111)-direction in the pseudo-cubic unit cell.[34,35] Thus, some structural kinks inevitably exist at the domain walls, inducing some contrast patterns on the surface of (100)-oriented PMN-PT as shown in the inset of Fig. 4b. Such kinks are also observed in the AFM image of graphene on the top surface of the PMN-PT substrate due to the ultra-thin graphene layer. It was reported that the uneven surface morphology could enhance the charge trapping effects at the interface between the graphene layer and the underlying ferroelectric materials.[26] Typically, the charge traps can be divided into two types. One is the surface defects related "intrinsic" traps and the other is the adsorbates related "external" traps. Uneven surface morphology would not only induce more surface defects for the underlying ferroelectric materials but also provide more locations for adsorbates. Thus, we believe that the surface morphology can affect the charge traps at the interface of graphene/PMN-PT. At the rising edge of the gate pulse, R_s increases instantly due to the hole density decrease in graphene caused by the electron accumulation at the interface. R_s then decreases gradually when V_g is maintained at +5 V. In this process, the accumulated electrons at the interface are trapped by the trapping states. As a consequence, the graphene layer

gets less gate potential from the underlying ferroelectric gate of PMN-PT. At the falling edge of the gate pulse, R_s decreases rapidly due to the increase in carrier density of holes caused by the hole accumulation at the interface. R_s increases quite slowly during the period of the negative voltage due to the de-trapping process of the trapped electrons. Thus, the carrier density of holes decreases and the resistance increases accordingly.[19] By considering that magnitude of the applied gate pulses is much smaller than the coercive voltage, the spontaneous polarization of PMN-PT cannot be switched during the entire process. Herein, the time-dependent behaviors of graphene/PMN-PT are dominated by the charge trapping and de-trapping at the interface when the V_g is much smaller than V_c.

Moreover, it should be mentioned that single-crystal PMN-PT is also a piezoelectric material possessing a large converse piezoelectric response.[36,37] Thus, the V_g not only provides E but also induces in-plane strain, and such strain could be potentially delivered to the above graphene layer.[31,38,39] Thus, there could be two possible co-existing tuning mechanisms, $i.e.$, field effect and strain effect with regards to employing PMN-PT as a gate dielectric. The strain provided by the PMN-PT can be calculated according to the change in lattice constant under external E. Actually, the strain is much smaller, typically less than 0.1% for V_g of 500 V.[31] However, at least 0.5% strain is required to access the strain dependent resistance.[40,41] In addition, typically, a large strain in excess of 20% is needed to induce a band gap in graphene.[42,43] Moreover, ohmic contact can be formed between graphene and the electrodes and can be retained even when V_g is up to ±200 V. Accordingly, the effect of piezoelectric strain on the contact resistance can be ignored in our experiments. Therefore, the small piezoelectric strain is negligible in our sample and the strain effects on our GFeFETs can be ruled out, while the ferroelectric field effects and the charge trapping effects are dominant in the transport properties.
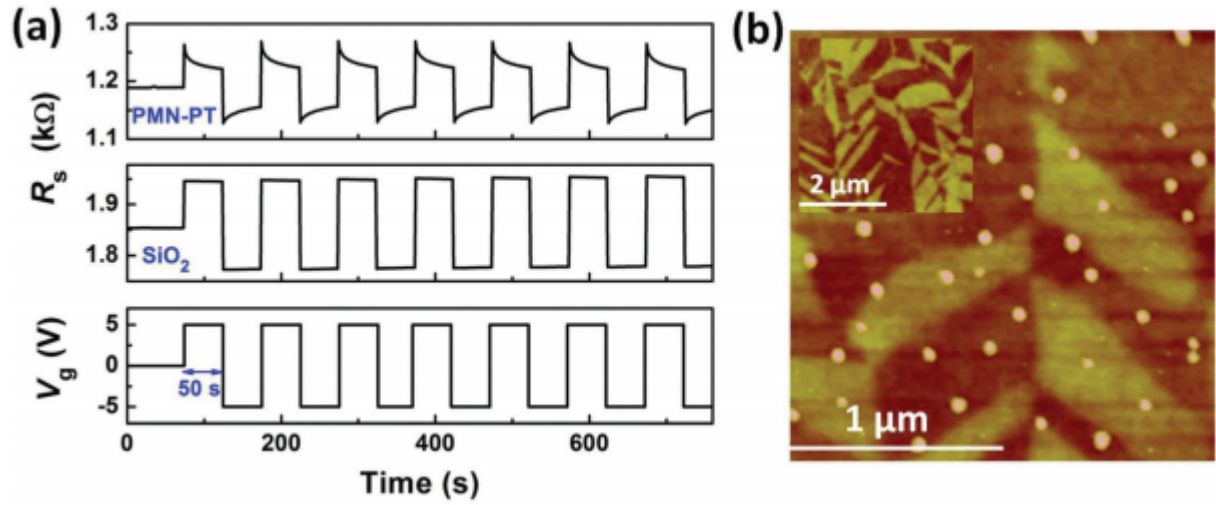
Fig. 4 (a) Sheet resistance of graphene on PMN-PT during the retention of the pulse gate voltages. For reference, sheet resistance of graphene on SiO_2 is also shown in the middle panel. Pulse voltages are shown in the bottom panel. (b) AFM image of graphene on PMN-PT. The inset shows the surface morphology of the PMN-PT substrate before graphene transferring.

By considering that both the reversal of ferroelectric polarization and interface charge trapping can contribute to the observed transport properties in GFeFETs, a large V_g capable of switching the spontaneous polarization in PMN-PT is used in the measurement of time evolution of R_s as illustrated in Fig. 5a. R_s is recorded as a function of time during the retention of a V_g of 200 V, which is sufficiently large to ensure complete switching of the polarization. The time-dependent R_s exhibits three distinct steps when V_g is applied. The initial rapid sharp rise of R_s is followed by a slow exponential increase, and finally, R_s reaches saturation and remains unchanged in the high resistance state after a period of about 100 s. The observed high-resistance state at 200 V can be understood from the initial low-resistance state of p-type properties. Graphene is actually p-doped at zero gated by adsorbates of molecules in air. The ferroelectric

spontaneous polarization can further enhance the p-doping properties and contribute to the initial low resistance state. The applied V_g of 200 V is large enough to align the polarization in PMN-PT in the upward direction. By considering the Dirac point located at about 100 V for graphene on PMN-PT, the gate voltage of 200 V can generate electron doping in graphene and the generated electrons can act as current carriers. Moreover, the generated electrons normally "screen" the charge carriers resulting in a weaker "trapping" effect. Due to the time-dependent charge trapping and de-trapping at the interface, a steady exponential increase in resistance is actually observed. When R_s reaches a steady high resistance state, the V_g voltage is removed, and R_s is recorded as a function of time as shown in Fig. 5b. The R_s decreases gradually and reaches a saturation regime after 5000 s. The inset of Fig. 5b shows the log scale data of $R(t) - R_h$, where $R(t)$ is the time-dependent R_s and R_h stands for R_s at the finally saturated high-resistance state. By considering the unique non-volatility in ferroelectric PMN-PT, the ferroelectric polarization should be retained even when the external field is removed.[44] The PMN-PT would finally reach the state with remnant polarization, which can contribute to the high resistance in graphene regardless of the slightly shifted dipoles in PMN-PT. The log scale curve fits well with the red dash line, presenting a linear relationship with time as shown in the inset of Fig. 5b. This presents the exponential decay R_s over time. The initial non-linear or non-exponential change can result from a gradual decrease in the ferroelectric polarization of PMN-PT, while the exponential decay suggests the time-dependent charge injection and trapping at the interface between graphene and PMN-PT. Herein, we can conclude that the R_s evolution exhibits three states, namely an initial rapid change, followed by a slow nearly exponential evolution, and finally a saturated state no matter when the large V_g is retained or after it is released. During the entire process, the transport properties of graphene are tuned by multiple factors, including ferroelectric

polarization, non-volatility and charge trapping. However, graphene initially reaches a high-resistance state due to the ferroelectric doping and finally reaches a steady high-resistance state due to the ferroelectric non-volatility from initial retention and subsequent release of V_g. Therefore, the ferroelectric effects are dominated in this process when V_g is larger than V_c.
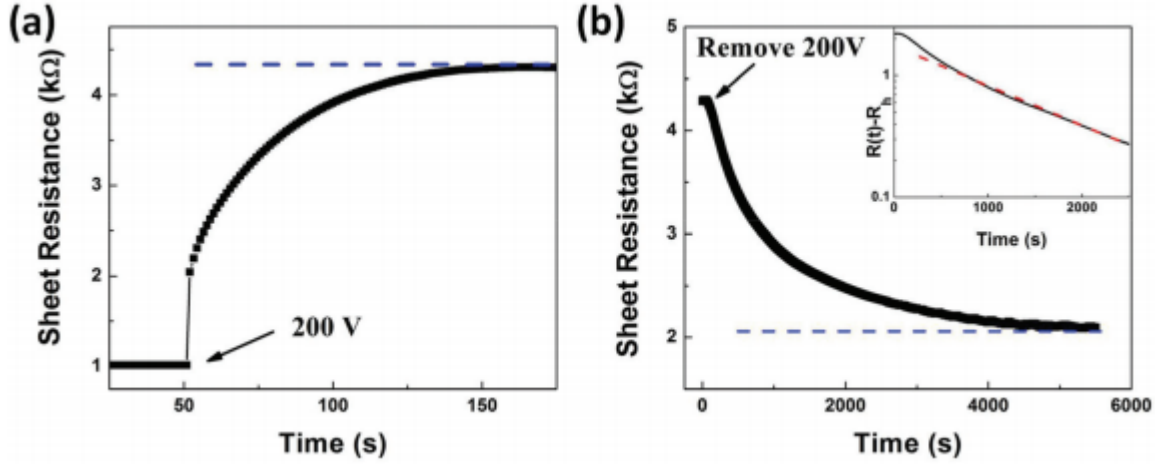

Fig. 5 (a) Time-dependent sheet resistance during the retention of a bias voltage of 200 V. (b) Time-dependent sheet resistance after the bias voltage of 200 V is removed. The inset shows the log scale data of $R(t) - R_h$, where $R(t)$ is the time-dependent sheet resistance and R_h is the final saturated resistance. The log scale curve fits well with the red dash linear line.

CONCLUSIONS

The co-existing effects of ferroelectric and charge trapping were investigated in graphene/PMN-PT FETs during the retention of V_g and after removing it. It is proposed that the transport properties of graphene are tuned by multiple factors, including ferroelectric polarization, non-volatility and charge trapping during the entire process, in which V_g is retained and subsequently

released. Through systematical analysis of the time-dependent transport properties of graphene, we can conclude that R_s shows a slight decay if $V_g < V_c$ due to the charge trapping at the interface. Moreover, if $V_g > V_c$, R_s evolution exhibits three states: an initial rapid change, followed by a slow nearly exponential evolution and then a saturated state no matter when the large V_g is retained or after it is released. In particular, graphene initially reaches a high-resistance state due to the ferroelectric doping and finally reaches a steady high-resistance state due to the ferroelectric non-volatility. Therefore, the ferroelectric effects are dominated in this process when V_g is larger than V_c.

EXPERIMENTAL SECTION

Fabrication of graphene/PMN-PT GFeFETs: monolayer graphene samples were prepared by CVD method on copper foils and then transferred onto PMN-PT substrates. The detailed growth and transferring methods can be referred to our earlier study.[45] After transferring graphene, source and drain electrodes were prepared through a well-designed mask. In our experiments, the electrodes were prepared by first depositing about 15 nm Ti, followed by depositing about 150 nm Au thin films. The Ti buffer layer was used to improve the contact properties between graphene and Au. Good ohmic contact was formed between graphene and the electrodes. Then, Au gate electrodes were directly prepared on the bottom surface of the PMN-PT substrate by sputtering technique. For reference, FETs using traditional SiO_2 as gate dielectric were prepared by transferring graphene onto silicon wafers coated with 300 nm thick SiO_2.

Characterizations：Raman spectroscopy (HORIBA JOBIN YVON, HR800) was employed to examine the CVD-grown monolayer graphene. In the Raman system, the excitation wavelength was 488 nm and 100× objective lens with numerical aperture of 0.9 was provided for the

measurements. Atomic force microscopy (AFM, DI Nanocope 8) was used to characterize the surface morphology of the PMN-PT substrate and CVD-grown monolayer graphene after transferring onto the PMN-PT. The carrier density was confirmed by the Hall effect measurement system (Ecopia HMS-3000). The ferroelectric hysteresis loops were measured by the materials measuring system (Premier II, Radiant Technologies Inc., USA). A four-probe technique was employed to measure the transport properties of graphene. In this system, a Keithley 2400 SourceMeter was used to provide a bias voltage of 0.5 V and measure the resistance of graphene. Moreover, a Keithley 2410 was employed to provide the large voltages and a Keithley 3390 Arbitrary Waveform/Function generator was used for the pulse voltage signals. All the above measurements were performed in air at room temperature.

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