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Improved interfacial and electrical properties of Ge MOS capacitor with ZrON/TaON multilayer composite gate dielectric by using fluorinated Si passivation layer

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A Ge metal-oxide-semiconductor capacitor with a composite gate dielectric composed of a ZrON/TaON multilayer and a Si passivation layer treated with fluorine plasma is fabricated. Its interfacial and electrical properties are compared with those of its counterparts without the Si passivation layer or the fluorine-plasma treatment. Experimental results show that the device with the fluorinated Si passivation layer exhibits excellent interfacial and electrical performances: low interface-state density (2.0×10^{11} cm^2 eV^{-1} at midgap), small flatband voltage (0.17 V), low gate leakage current (2.04×10^{-6} A/cm^2 at $V_g = V_{fb} + 1$ V), and high equivalent dielectric constant (22.6). The involved mechanism lies in the fact that the TaSiON interlayer formed by mixing of TaON and Si passivation layers can effectively suppress the growth of unstable Ge oxides to reduce the defective states at/near the TaSiON/Ge interface. Moreover, the fluorine-plasma treatment can passivate the oxygen vacancies and conduce to the blocking of elemental inter-diffusions, thus largely improving the interfacial quality to achieve excellent electrical properties for the device. *Published by AIP Publishing*. [http://dx.doi.org/10.1063/1.4996722]

Ge-based MOSFETs with a high-k (dielectric constant) gate dielectric have become one attractive approach that has been widely studied due to their higher electron and hole mobilities than their Si counterparts.[1] However, many issues still need to be addressed before Ge can be implemented in high-performance MOSFET devices. One of the key issues is to achieve a high-quality interfacial layer, which would not lead to substantial drive-current degradation in both low equivalent oxide thickness and short channel regimes.[2] So, different surface passivation layers such as GeON,[3] Al_2O_3,[4] and AlON[5] have been investigated, and the interfacial properties between the high-k dielectric and the Ge substrate were improved to different extents. However, unstable GeO_x could grow at the Ge surface during the high-k deposition and so has to be suppressed. Several monolayers of Si were deposited on a cleaned Ge substrate using remote plasma chemical vapor deposition,[6] resulting in an improved gate stack quality with an interface-state density (D_{it}) of $\sim 5 \times 10^{11}$ cm^{-2}eV^{-1}. Moreover, a RF-sputtered Si passivating layer has been demonstrated to provide excellent interface quality with GaAs[7] because it could prevent the oxygen in the high-k dielectric from diffusing into the GaAs substrate by consuming the oxygen. Based on the same mechanism, it is expected to obtain good high-k/Ge interface quality by depositing a Si passivation layer on the Ge substrate. However, depositing the Si layer on Ge should meet two strict criteria:[8] (1) the Si passivation layer must completely cover the Ge surface free of GeO_x; and (2) the Si passivation layer should be thin enough and consumed during the subsequent processing. To readily satisfy these requirements, a good way is to deposit another interlayer on the Si passivation layer to consume Si through chemical reaction. TaON can be considered as a good candidate because it easily forms TaSi with Si and also has been used as an interfacial passivation interlayer (IPL) in Ge MOSFETs with excellent electrical and reliability properties.[9,10] On the other hand, it was reported that the TaO-TiO multilayer as a gate dielectric on a Si substrate had excellent electrical properties,[11] and zirconium dioxide (ZrO_2) with a high k value (~20) and a large bandgap (5.8 eV) has been used as a high-k gate dielectric for Si,[12] SiGe,[13] and GaAs[14] MOS devices with good interfacial and electrical properties. Therefore, in this work, by alternate sputtering of Zr and Ta targets, a Ge MOS device with the ZrON/TaON multilayer composite gate dielectric and Si passivation interlayer is proposed and fabricated. Moreover, a fluorine-plasma treatment is used to further improve the interface and bulk properties of the device because fluorine incorporation was reported to be capable of passivating the oxygen vacancies in high-k materials.[15,16]

Ge MOS capacitors were fabricated on n-type (100) Ge wafers with a resistivity of 0.02–0.10 Ω cm. The wafers were cleaned using ethanol, acetone, and trichloroethylene, followed by dipping in diluted HF (1:50) for 30 s, and then rinsed with deionized water several times to remove the native oxide. After N_2 drying, the wafers were immediately transferred to the vacuum chamber of a Denton Vacuum

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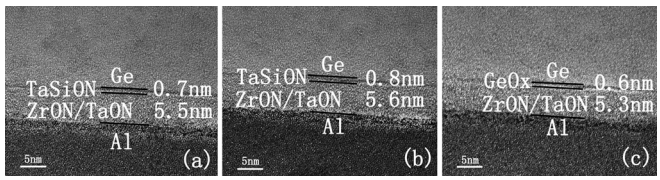

FIG. 1. Cross-sectional TEM image: (a) ZrON/TaON/Si + F sample, (b) ZrON/TaON/Si sample, and (c) ZrON/TaON sample.

Discovery Deposition System. A thin Si film (~1 nm) was deposited by sputtering a Si target at room temperature in an Ar ambient, and then, a high-k composite gate dielectric (~6 nm) composed of alternate ZrN/TaN (12 layers, ~0.5 nm per layer) was deposited by alternate sputtering of Zr and Ta targets in an Ar/N_2 (24 sccm/12 sccm) ambient at room temperature. Next, a sample received a fluorine-plasma treatment in an ambient of $CHF_3/O_2 = 10/1$ for 5 min. For comparison, another sample without the Si film was prepared under the same conditions as above. Subsequently, post-deposition annealing (PDA) was carried out at 500 °C for 300 s in N_2 (500 sccm) + O_2 (50 sccm) to transform ZrN/TaN to ZrON/TaON. So, the samples can be divided into three groups: samples with the Si passivation layer with or without fluorine-plasma treatment (denoted as ZrON/TaON/Si + F or ZrON/TaON/Si) and sample without the Si passivation layer (denoted as ZrON/TaON). Finally, Al was thermally evaporated and patterned as a gate electrode with an area of 7.85×10^{-5} cm^2, followed by a forming-gas (95% N_2 + 5% H_2) annealing at 300 °C for 20 min.

High-frequency (HF) capacitance-voltage (C-V) and gate leakage current-voltage (J_g-V_g) measurements were performed using a HP4284A precision LCR meter and a HP4156A semiconductor parameter analyzer, respectively. The physical thickness of the gate dielectrics was determined by spectroscopic ellipsometry.

Figure 1 shows the TEM images of all the samples. As can be seen from Fig. 1(a), a TaSiON interlayer (0.7 nm) is formed between the Ge substrate and the ZrON/TaON gate dielectric (5.5 nm) with a clear TaSiON/Ge interface and a total physical thickness of 6.2 nm for the ZrON/TaON/Si + F sample. However, for the ZrON/TaON/Si sample in Fig. 1(b), a slightly thicker TaSiON interlayer (0.8 nm) is formed, and also the TaSiON/Ge interface is not too sharp. For the ZrON/TaON sample in Fig. 1(c), a GeO_x interlayer with a blurred interface is formed. These TEM images confirm the formation of the proposed gate stack structure and indicate that the ZrON/TaON/Si + F sample has better interface quality than the ZrON/TaON/Si and ZrON/TaON samples.

Figure 2 shows the typical HF C-V curves of the three samples. Obviously, the ZrON/TaON sample has a much smaller accumulation capacitance than the other two samples, implying that a low-k GeO_x interlayer exists in the former, as shown in Fig. 1(c), and is greatly suppressed in the latter two samples due to the effective blocking role of the TaSiON interlayer [see Figs. 1(a) and 1(b)] against the in-diffusion of oxygen and out-diffusion of germanium.[17] As a result, a stretch out of the C-V curve and a small kink in the depletion region are observed for the ZrON/TaON sample, indicating a high interface-state density. As for the two

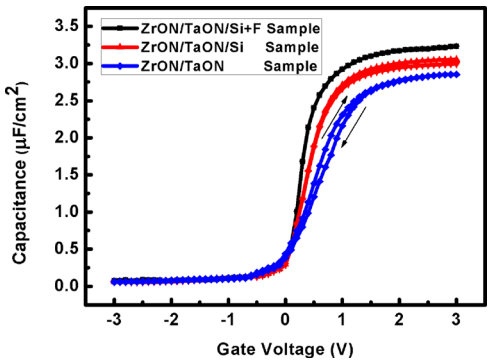

FIG. 2. HF (1-MHz) C-V curve of the samples.

samples with Si passivation layer, no such distortion occurs and a larger slope of the C-V curve from depletion to accumulation is obtained, implying a high-quality TaSiON/Ge interface. Furthermore, a much smaller C-V hysteresis for the ZrON/TaON/Si + F sample (15 mV) and ZrON/TaON/Si sample (25 mV) than for the ZrON/TaON sample (90 mV) is observed in Fig. 2, indicating less slow states or deep-level traps in the former two samples (especially, for the ZrON/TaON/Si + F sample). The flatband voltage (V_{fb}) of the samples is determined from their flatband capacitance,[18] and equivalent oxide-charge density (Q_{ox}), mainly including interface trapped charge (Q_{it}), border trapped charge (Q_{bt}), oxide trapped charge (Q_{ot}), and fixed oxide charge (Q_f), is calculated as $-C_{ox}(V_{fb} - \varphi_{ms})/q$, with φ_{ms} being the work-function difference between Al and Ge and C_{ox} being the accumulation capacitance (oxide capacitance) per unit area. The interface-state density near midgap (D_{it}) is extracted from the 1-MHz C-V curve using Terman's method[19] for the purpose of comparison, as listed in Table I.

Obviously, the ZrON/TaON/Si + F and ZrON/TaON/Si samples have smaller V_{fb} and D_{it} than the ZrON/TaON sample, with the smallest for the ZrON/TaON/Si + F sample ($V_{fb} = 0.17$ V and $D_{it} = 2.0 \times 10^{11}$ eV^{-1} cm^{-2}), which should be attributed to the fact that the TaSiON interlayer can block the out-diffusion of Ge and in-diffusion of oxygen at the TaSiON/Ge and high-k/TaSiON interfaces, and the F incorporated in the Si layer by the F plasma treatment can effectively occupy the oxygen vacancies in the TaSiON passivation layer and ZrON/TaON stack dielectric and passivate the traps at/near the TaSiON/Ge interface and in the dielectric bulk,[20,21] resulting in a reduction of defect traps in the dielectric bulk and at/near the TaSiON/Ge interface.

TABLE I. Electrical and physical parameters of samples extracted from HF C-V curves.

Sample	ZrON/TaON/Si + F	ZrON/TaON/Si	ZrON/TaON
C_{ox} ($\mu F/cm^2$)	3.23	3.05	2.85
V_{fb} (V)	0.17	0.22	0.26
D_{it} (cm^{-2} eV^{-1})	2.0×10^{11}	2.9×10^{11}	5.4×10^{11}
Q_{ox} (cm^{-2})	-2.95×10^{12}	-3.39×10^{12}	-4.16×10^{12}
t_{ox} (nm)	6.2	6.4	5.9
CET (nm)	1.07	1.13	1.21
k	22.6	22.1	19.0

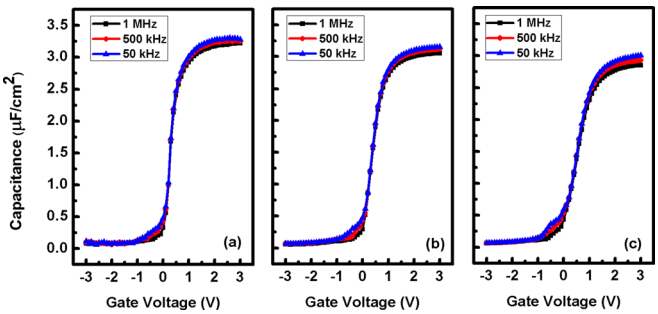

FIG. 3. Frequency dispersion of C-V curves at room temperature: (a) ZrON/TaON/Si + F sample, (b) ZrON/TaON/Si sample, and (c) ZrON/TaON sample.

The excellent interface quality of the ZrON/TaON/Si + F sample is further supported by the small frequency dispersion of its C-V curve and small distortion in the depletion region even at 50 kHz, as shown in Fig. 3. The larger accumulation capacitance of the ZrON/TaON/Si + F sample than the ZrON/TaON/Si sample is also attributed to the F incorporation at/near the (ZrON/TaON)/TaSiON and TaSiON/Ge interfaces, which can further suppress the growth of the low-k GeO_x interlayer to give a higher-quality TaSiON/Ge interface.

The capacitance equivalent thickness (CET) is calculated as $CET = k_0 k_{SiO2}/C_{ox}$, where k_0 and k_{SiO2} are the vacuum permittivity and relative permittivity of SiO_2, and thus the equivalent k value of the gate dielectric can be calculated as $k = k_{SiO2} t_{ox}/CET$, as also listed in Table I. Obviously, the ZrON/TaON/Si + F sample has the smallest CET (1.07 nm) and largest k value (22.6) due to the enhanced suppression of the low-k GeO_x growth, as mentioned above. Also, the smallest Q_{ox} is obtained for the ZrON/TaON/Si + F sample, followed by the ZrON/TaON/Si sample, further indicating the effective blocking role of the TaSiON interlayer (especially, the one with fluorine incorporation) against the inter-diffusion of elements.[22]

The gate leakage properties of the three samples are shown in Fig. 4. The ZrON/TaON/Si + F sample has the lowest gate-leakage current among the three samples (e.g., at $V_g = V_{fb} + 1$ V, $J_g = 2.04 \times 10^{-6}$ A/cm^2, 6.07×10^{-6} A/cm^2, and 2.35×10^{-5} A/cm^2 for the ZrON/TaON/Si + F, ZrON/TaON/Si, and ZrON/TaON samples, respectively), which is closely related to its smallest D_{it} and Q_{ox} due to the absence of the undesirable GeO_x interlayer and the suppression of intermixing between Ge and high-k dielectric.[23,24] Furthermore, a

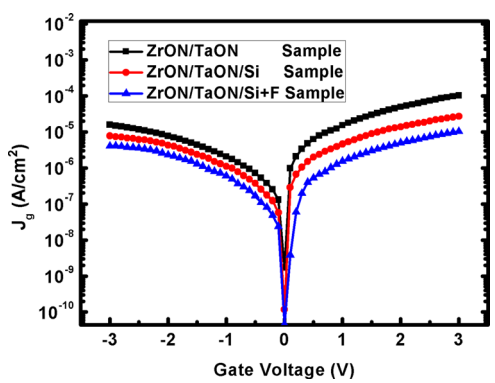

FIG. 4. J_g-V_g characteristics of the samples.

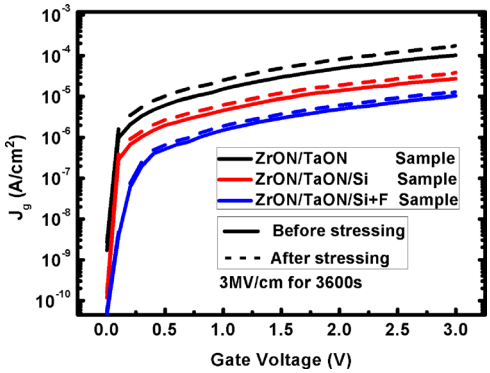

FIG. 5. Gate leakage current density of the samples before and after a high-field stressing at 3 MV/cm for 3600 s.

high-field stress at 3 MV/cm [$=(V_g - V_{fb})/t_{ox}$] for 3600 s is used to examine the reliability of the devices. The J_g-V_g properties are measured before and after the stressing, as shown in Fig. 5. The increase in gate leakage current after the stressing for the three samples is due to the trap-assisted tunneling of electrons from the substrate to the gate via stress-induced interface and near-interface traps. The post-stress increase of the leakage current is the smallest for the ZrON/TaON/Si + F sample, which can be associated with less generation of interface and near-interface traps during the constant-voltage stressing due to negligible unstable GeO_x at/near the TaSiON/Ge interface,[25–27] as confirmed by XPS result below.

To study the composition of the TaSiON IPL and further analyze the effects of TaSiON on the chemical states of the interface between ZrON/TaON and Ge, the ZrON/TaON

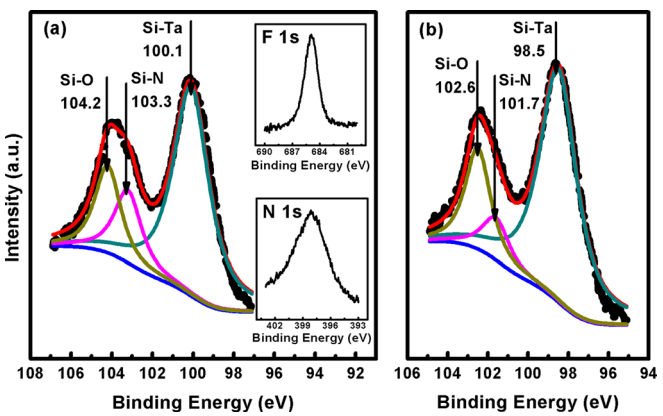

FIG. 6. Si 2p XPS spectrum in the TaON/Si interlayer: (a) ZrON/TaON/Si + F sample, where the insets are its F 1s and N 1s XPS spectra, respectively, and (b) ZrON/TaON/Si sample.

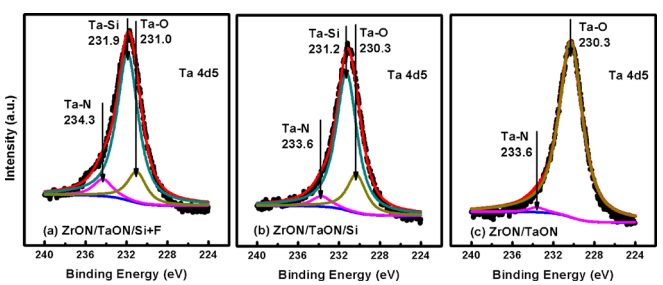

FIG. 7. Ta 4d5 XPS spectrum of the TaON/Si interlayer: (a) ZrON/TaON/Si + F sample, (b) ZrON/TaON/Si sample, and (c) ZrON/TaON sample.

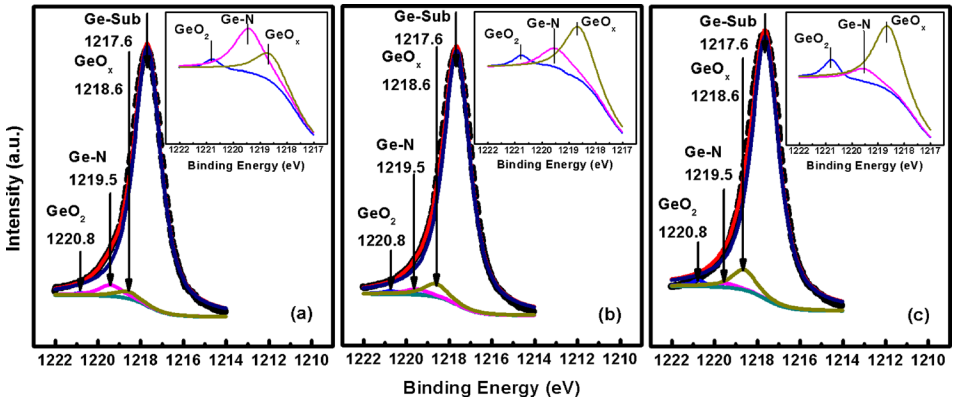

FIG. 8. Ge 2p3 XPS spectrum at/near the high-k/Ge interface: (a) ZrON/TaON/Si + F sample, (b) ZrON/TaON/Si sample, and (c) ZrON/TaON sample. The inset is the enlarged figure of Ge oxides and oxynitride.

film is etched to a distance of ~5 nm from the Ge surface using an *in-situ* Ar^+ ion beam in the XPS chamber. Figures 6(a) and 6(b) show the Si 2p XPS spectrum of the ZrON/TaON/Si + F and ZrON/TaON/Si samples. As compared with the ZrON/TaON/Si sample, the Si 2p peak of the ZrON/TaON/Si + F sample is shifted by an energy of 1.6 eV, which should be attributed to the higher electronegativity of F (4.0) than that of O (3.5). Furthermore, in Fig. 6(a), Si-O, Si-N, and Si-Ta bonds are found at 104.2 eV, 103.3 eV, and 100.1 eV, respectively, but no Si-Si bond at 101.2 eV is observed,[28,29] indicating that the TaSiON IPL has been formed and all Si has been consumed.

Similarly, as shown in Fig. 7(a), the Ta 4d5 peak of the ZrON/TaON/Si + F sample also shifts to higher energy relative to that of the ZrON/TaON/Si sample, and the Ta-N, Ta-Si, and Ta-O bonds are found at 234.3 eV, 231.9 eV, and 231.0 eV, respectively,[30,31] from which the content of the Ta-O bond for the ZrON/TaON/Si + F and ZrON/TaON/Si samples is calculated to be 14.5% and 19.2%, respectively, based on the Ta-O/Ta 4d5 peak-area ratio. This implies that the fluorine incorporation can block the oxygen diffusion from the dielectric layer to the substrate surface. Similarly, the content of the Ta-Si bond for the ZrON/TaON/Si + F and ZrON/TaON/Si samples is extracted to be 77.6% and 71.3%, respectively, based on the Ta-Si/Ta 4d5 peak-area ratio, implying that the silicon passivation layer is consumed during the subsequent high-k deposition and PDA. Furthermore, the obvious F 1s peak in the F 1s spectrum of the ZrON/TaON/Si + F sample [Fig. 6(a)] indicates that fluorine is indeed incorporated in both the gate dielectric and the passivation layer, resulting in effective passivation on the dangling bonds and oxide traps at/near the high-k/Ge interface. This is why the ZrON/TaON/Si + F sample has the best interfacial and thus electrical properties, as shown in Table I.

To further analyze the Ge oxides or oxynitride at/near the interface, the Ge 2p3 spectrum of the three samples is shown in Fig. 8. The peaks of GeO_2, GeON, GeO_x, and Ge-sub are found at 1220.8 eV, 1219.5 eV, 1218.6 eV, and 1217.6 eV, respectively,[32,33] for the three samples, demonstrating that there exist GeO_2, GeON, and GeO_x at/near the TaSiON/Ge interface. For more clearly showing the peaks of Ge oxides and oxynitride, they are enlarged in their respective insets. Obviously, the content of GeO_x or GeO_2 is lower for the ZrON/TaON/Si + F sample (3.2% or 1.1% from the GeO_x/Ge2p3 or GeO_2/Ge2p3 peak-area ratio) than for the ZrON/TaON/Si sample (5.3% or 1.9%) and the ZrON/TaON sample (7.1% or 3.2%), implying that the fluorine incorporation can effectively occupy the oxygen vacancies in the TaSiON IPL and at/near the TaSiON/Ge interface. On the contrary, the content of GeON is higher for the ZrON/TaON/Si + F sample (4.5% from the GeON/Ge2p3 peak-area ratio) than for the ZrON/TaON/Si sample (2.8%) and the ZrON/TaON sample (2.1%), implying more N incorporation in the former than in the latter two samples, which is beneficial for blocking the in-diffusion of oxygen. These results indicate that the fluorine incorporation can further reduce the oxide traps to aid the formation of GeON for blocking the inter-diffusion of elements near the TaSiON/Ge interface, resulting in the best interface quality and thus best electrical properties, as demonstrated by the ZrON/TaON/Si + F sample.

The effects of the Si passivation interlayer and fluorine-plasma treatment on the interfacial and electrical properties of Ge MOS capacitor with the composite gate dielectric deposited by alternate sputtering of ZrON/TaON are investigated. It is demonstrated that the device with the fluorinated Si passivation layer exhibits excellent device performance: low interface state density (2.0×10^{11} cm^2 eV^{-1} at midgap), small flatband voltage (0.17 V), small gate leakage current density (2.04×10^{-6} A/cm^2 at $V_g = V_{fb} + 1$ V), high equivalent k value (22.6), and good high-field reliability. All of these can be attributed to the fact that the TaSiON IPL formed by mixing of the TaON dielectric layer and Si passivation layer can effectively suppress the growth of unstable native oxides at the Ge surface and the fluorine incorporation is conducive to blocking the elemental inter-diffusion and filling the oxygen vacancies, thus reducing the oxide traps at/near the high-k/Ge interface to achieve better electrical properties for the Ge MOS device.

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