Interfacial and Electrical Properties of Ge MOS Capacitor by ZrLaON Passivation Layer and Fluorine Incorporation

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Interfacial and Electrical Properties of Ge MOS Capacitor by ZrLaON Passivation Layer and Fluorine Incorporation

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Abstract. Ge Metal-Oxide-Semiconductor (MOS) capacitor with HfTiON/ZrLaON stacked gate dielectric and fluorine-plasma treatment is fabricated, and its interfacial and electrical properties are compared with its counterparts without the ZrLaON passivation layer or the fluorine-plasma treatment. Experimental results show that the sample exhibits excellent performances: low interface-state density (3.7×10^{11} $cm^{-2}eV^{-1}$), small flatband voltage (0.21 V), good capacitance-voltage behavior, small frequency dispersion and low gate leakage current (4.41×10^{-5} A/cm^2 at $V_g = V_{fb} + 1V$). These should be attributed to the suppressed growth of unstable Ge oxides on the Ge surface during gate-dielectric annealing by the ZrLaON interlayer and fluorine incorporation, thus greatly reducing the defective states at/near the ZrLaON/Ge interface and improving the electrical properties of the device.

1. Introduction

Ge-based MOSFET with high-k gate dielectric has been widely investigated due to its higher carrier mobility [1, 2] and easier integration of Ge on Si than III-V semiconductors on Si. However, the development of Ge MOSFET has been hampered due to the absence of a good thermally-grown oxide on the Ge substrate. In order to overcome the drawback of the unstable and volatile Ge native oxide, a high-quality interface between high-k dielectric and Ge is needed to establish the Ge MOS technology [3]. So introducing an interfacial passivation layer (IPL) becomes very important for improving the performance of Ge MOS devices. But the dielectric constant (k) of many IPL materials, e.g. SiO_2 (~ 3.9) [4], GeON (~ 7) [5], Al_2O_3 (~ 8) [6], AlON (~ 10) [7], is usually not very large, thus limiting further scaling of the devices.

It is well known that Zirconium dioxide (ZrO_2) has a high k value (~ 20), a large bandgap (5.8 eV) and has been used as high-k gate dielectric for Si [8], SiGe [9] and GaAs [10] MOS devices with good

interfacial and electrical properties. However, ZrO_2 may easily crystallize due to its lower crystallization temperature (400 - 500 ℃) [11], thus leading to a large gate leakage current [12]. Luckily, it has been demonstrated that incorporating lanthanum (La) into ZrO_2 can increase the crystallization temperature, and also can suppress the growth of the interfacial layers, thus it can reduce the defects in the dielectric and improve the interface quality [13, 14]. So in this work, La-doped ZrON (ZrLaON) would be used as IPL to improve the interfacial properties of the Ge MOS devices.

As one of the most promising high-k materials, Hf-based oxide/silicate/aluminate are often employed as gate dielectric. However, their moderate dielectric constants limit further device scaling [15]. While it is well known that Ti oxide has much higher k value than Hf oxide, Ti-incorporated Hf oxynitride (HfTiON) can achieve higher k value [16]. So, in this work, the Ge MOS device with ZrLaON as passivation interlayer and HfTiON as high-k layer is proposed and prepared. On the other hand, fluorine incorporation was reported to be another good way for passivating the Ge surface because it is capable of passivating the oxygen vacancies in high-k materials [17, 18]. Therefore, the fluorine-plasma is also used to treat the Ge MOS capacitor with the stacked gate dielectric of HfTiON/ZrLaON in this work, and its electrical and interfacial characteristics are compared with its counterparts without ZrLaON passivation layer or fluorine-plasma treatment.

2. Experiments

Ge MOS capacitors were fabricated on n-type (100) Ge wafers with a resistivity of 0.02 ~ 0.10Ωcm. The wafers were cleaned using ethanol, acetone and trichloroethylene, followed by dipping in diluted HF (1:50) for 30 s, and then rinsed in deionized water for several times to remove the native oxide. After N_2 drying, the wafers were immediately transferred to the vacuum chamber of the Denton Vacuum Discovery Deposition System. A ~ 2-nm ZrLaON film was deposited by co-sputtering Zr and La_2O_3 targets (as IPL) at room temperature in Ar/N_2 (= 24/12) ambient, followed by the in-situ deposition of a ~ 6-nm HfTiN gate dielectric by co-sputtering Hf and Ti targets in the same ambient. Next, a sample received a fluorine-plasma treatment at a flow rate of CHF_3/O_2 = 10/1 for 5 min.

For comparison, a control sample without the ZrLaON interlayer (i.e. HfTiON was directly deposited on Ge) was prepared. So, the samples can be divided into three groups: the sample with ZrLaON passivation layer and fluorine-plasma treatment (denoted as ZrLaON+F), the sample with ZrLaON passivation layer but no fluorine-plasma treatment (denoted as ZrLaON) and the control sample without any passivation layer. Subsequently, post-deposition annealing (PDA) was carried out at 500 ℃ for 300 s in N_2 (500 sccm) + O_2 (50 sccm) to transform HfTiN into HfTiON, respectively. Finally, Al was thermally evaporated and patterned as gate electrode with an area of 7.85×10^{-5} cm^2, followed by a forming-gas (95% N_2 + 5% H_2) annealing at 300 ℃ for 20 min to reduce contact resistance.

High-frequency (HF) capacitance-voltage (C-V) and gate leakage current-voltage (J_g-V_g) measurements were performed using HP4284A precision LCR meter and HP4156A semiconductor parameter analyzer, respectively. Physical thickness of the gate dielectrics was determined by spectroscopic ellipsometry. The chemical structures at/near the high-k/Ge interface were analyzed by X-ray photoelectron spectroscopy (XPS).

3. Results and Discussion

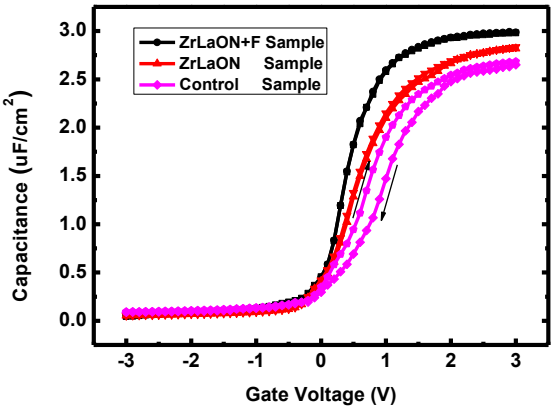

Figure 1. HF (1 MHz) C-V curve of all the samples.

Fig.1 shows the typical HF C-V curves of the three samples. Obviously, the control sample has a much smaller accumulation capacitance than the ZrLaON+F and ZrLaON samples, implying that a low-k GeO_x interlayer exists in the former and is greatly suppressed in the latter due to a blocking role of the ZrLaON interlayer against the in-diffusion of oxygen and out-diffusion of germanium. As a result, a stretch out of the C-V curve as well as a small kink in the depletion region are observed for the control sample in Fig.1, indicating a high interface-state density. While for the ZrLaON+F and ZrLaON samples, no such distortion occurs and a large slope of the C-V curve from depletion to accumulation is obtained, implying a high-quality ZrLaON/Ge interface. Furthermore, a smaller C-V hysteresis for the ZrLaON+F sample (10 mV) and ZrLaON sample (40 mV) than the control sample (220 mV) is observed in Fig. 1, indicating less slow states or deep-level traps in the former (especially for the ZrLaON+F sample) than in the latter. The flatband voltage (V_{fb}) of the samples is determined from their flatband capacitance [19], and equivalent oxide-charge density (Q_{ox}) is calculated as $-C_{ox}(V_{fb} - \varphi_{ms})/q$, with φ_{ms} as the work-function difference between Al and Ge, and C_{ox} as the accumulation capacitance (oxide capacitance) per unit area. The interface-state density near midgap (D_{it}) is estimated from the 1-MHz C-V curve using the Terman's method [20] for the purpose of comparison, as listed in Table 1.

Table 1. Electrical and Physical Parameters Extracted from HF C-V curves

Sample	ZrLaON+F	ZrLaON	Control
C_{ox} ($\mu F/cm^2$)	2.97	2.81	2.63
V_{fb} (V)	0.21	0.29	0.59
D_{it} ($cm^{-2}eV^{-1}$)	3.7×10^{11}	6.3×10^{11}	7.9×10^{12}
Q_{ox} (cm^{-2})	-3.39×10^{12}	-4.75×10^{12}	-9.87×10^{12}
t_{ox} (nm)	6.9	7.1	7.2
CET (nm)	1.16	1.23	1.31
k	23.2	22.5	21.4

Obviously, the ZrLaON+F and ZrLaON samples have smaller V_{fb} and D_{it} than the control sample, with the smallest for the ZrLaON+F sample (V_{fb} = 0.21 V and D_{it} = 3.7×10^{11} $eV^{-1}cm^{-2}$), Which should be attributed to the fact that the ZrLaON interlayer can block the out-diffusion of Ge and in-diffusion of oxygen at the interface, and the F incorporated in the HfTiON/ZrLaON stack dielectric by the F plasma treatment can effectively occupy the oxygen vacancies in the ZrLaON passivation layer and passivate the traps at/near the interface [21, 22], resulting in a reduction of defect traps in the dielectric bulk and at/near the ZrLaON/Ge interface.

This is further supported by the small frequency dispersion of its C-V curves and small distortion in the depletion region even for 50-kHz C-V curve, as shown in Fig. 2. The frequency dispersion in the accumulation region should be attributed to border traps with much larger trapping time constant than the interface traps [23, 24] because they can exchange charges with the conduction band of the semiconductor through tunneling, thus contributing to the total gate capacitance by capturing and emitting charges. As the measurement frequency increases, they are too slow to respond to the applied voltage, thus resulting in lower total gate capacitance [23]. The larger accumulation capacitance of the ZrLaON+F sample than the ZrLaON sample is also attributed to the F incorporation at/near the HfTiON/ZrLaON and ZrLaON/Ge interfaces, which can enhance the suppression of growth of the low-k interlayer and give high-quality ZrLaON/Ge interface.

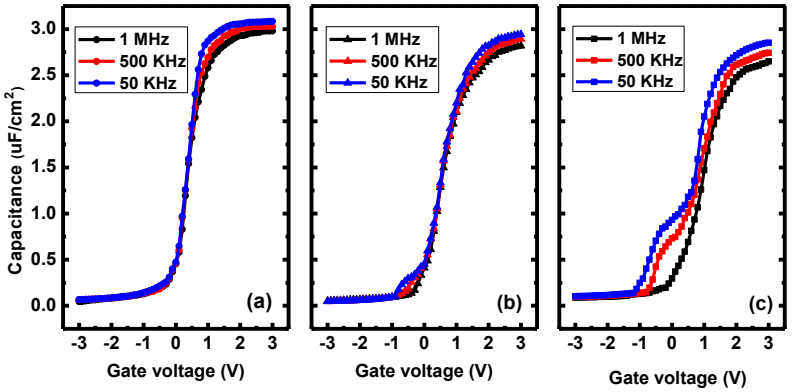

Figure 2. Frequency dispersion of C-V curves at room temperature. (a) ZrLaON+F sample, (b) ZrLaON sample, and (c) control sample.

The capacitance equivalent thickness (CET) is calculated as CET = $k_0 k_{SiO2}/C_{ox}$, where k_0 and k_{SiO2} are the vacuum permittivity and relative permittivity of SiO_2, and thus the equivalent k value of the gate dielectric can be calculated as k = $k_{SiO2} t_{ox}$/CET, as also listed in Table I. Obviously, the ZrLaON+F sample has the smallest CET (1.16 nm) and largest k value (23.2) due to the enhanced suppression of the low-k GeO_x growth, as mentioned above. Also, the smallest Q_{ox} is obtained for the ZrLaON+F sample, followed by the ZrLaON sample, indicating an effective blocking role of the ZrLaON interlayer (especially with Fluorine incorporation) against the inter-diffusion of elements [25].

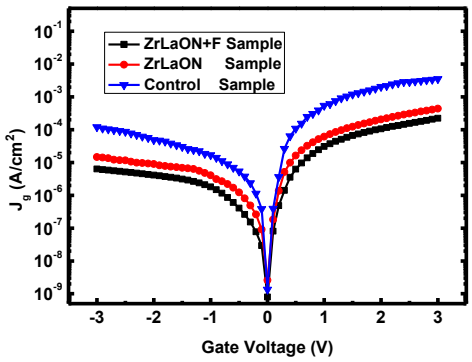

Figure 3. J_g-V_g Characteristics of all the samples.

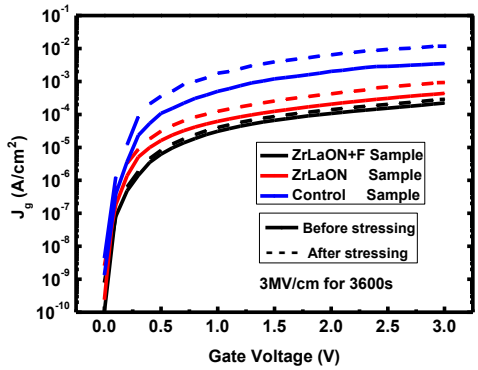

Figure 4. Gate leakage current density of all the samples before and after a high-field stressing at 3 MV/cm for 3600 s.

The gate leakage properties of the three samples are shown in Fig. 3. Obviously, the ZrLaON+F sample has the lowest gate-leakage current among the three samples (e.g. at $V_g = V_{fb} + 1$ V, $J_g = 4.41 \times 10^{-5}$ A/cm^2, 9.69×10^{-5} A/cm^2 and 1.31×10^{-3}A/cm^2 for the ZrLaON+F, ZrLaON and control

samples respectively), which is closely related to its smallest D_{it} and Q_{ox} due to the absence of the undesirable GeO_x interlayer and the suppression of intermixing between Ge and high-k dielectric [26, 27]. Furthermore, a high-field stress at 3 MV/cm [= $(V_g - V_{fb})/t_{ox}$] for 3600 s is used to examine the reliability of the devices. The J_g-V_g properties are measured before and after the stressing, as shown in Fig. 4. The increase in gate leakage current after the stressing for the three samples is due to the trap-assisted tunneling of electrons from the substrate to the gate via newly-generated interface and near-interface traps. Obviously, the post-stressing increase of the leakage current is smallest for the ZrLaON+F sample, which can be associated with less generation of the interface and near-interface traps during the constant-voltage stressing due to very little GeO_x at/near the ZrLaON /Ge interface [28], as confirmed by XPS result below.

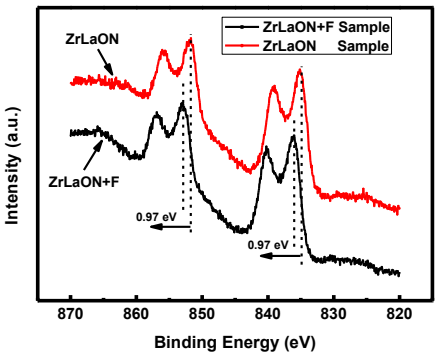

Figure 5. La 3d XPS spectrum at the ZrLaON interlayer of the ZrLaON+F and ZrLaON samples.

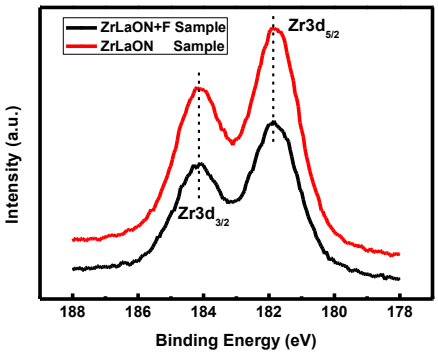

Figure 6. Zr 3d XPS spectrum at the LaTaON interlayer of the ZrLaON+F and ZrLaON samples.

To identify the composition and chemical status of the ZrLaON interlayer, and further analyze their effects on the chemical states of the interface between HfTiON and Ge, the HfTiON film is etched to a distance of ~ 5 nm from the Ge surface using an in-situ Ar+ ion beam in the XPS chamber. Fig. 5 shows the La 3d XPS spectrum of the ZrLaON+F and ZrLaON samples. As compared to the ZrLaON sample, the La 3d peaks of the ZrLaON+F sample exhibit a shift of 0.97 eV towards higher energy, which should be contributed to the higher electronegativity of F (4.0) than that of O (3.5).

Figure 6 shows the Zr 3d XPS spectra of the ZrLaON+F and ZrLaON samples, Two strong peaks at 181.9 eV (Zr 3d 5/2) and 184.1 eV (Zr 3d 3/2) are detected and the spin-orbit splitting energy of 2.2 eV is consistent with the Zr hump [29]. Also, the peak located at 181.9 eV should be from the mixture of major Zr-O bonds (182.0 eV [29]) and minor Zr-N bonds (180.1 eV [30]) (or Zr-O-N bonds at 180.0-182.5 eV [29]).

To further analyze the Ge oxides or oxynitride at/near the interface, the XPS spectrum of Ge 2p for the two samples are shown in Fig. 7, and the energy position and atomic percentage of the species are listed in Table 2.

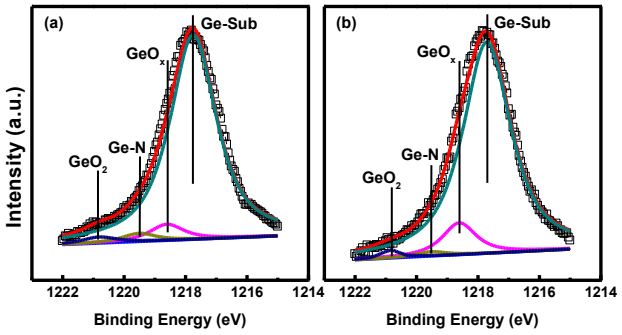

Figure 7. Ge 2p spectrum of (a) ZrLaON+F sample, (b) ZrLaON sample.

Table 2. Energy Position and Atomic Percentage of the Species In Fig. 7

Sample		ZrLaON+F sample	ZrLaON sample
	Energy Position (eV)	Atomic percentage (%)	Atomic percentage (%)
Ge-Sub	1217.7	90.3	86.4
GeO_x	1218.6	5.2	9.3
GeON	1219.5	2.6	1.1
GeO_2	1220.8	1.9	3.2

As can be seen, the GeO_2, GeON, GeO_x and Ge-Sub are found at 1220.8 eV, 1219.5 eV, 1218.6 eV and 1217.7 eV respectively [31, 32] for the two samples, demonstrating that there exist GeO_2, GeON and GeO_x at/near the ZrLaON/Ge interface. However, it is worth noting that the content of GeO_x is obviously lower for the ZrLaON+F sample (5.2% from the GeO_x/Ge2p peak-area ratio) than the ZrLaON sample (9.3%), and similarly, the content of GeO_2 is also lower for the ZrLaON+F sample (1.9% from the GeO_2/Ge3d peak-area ratio) than the ZrLaON sample (3.2%), implying fluorine incorporation can effectively occupy the oxygen vacancies in the ZrLaON passivation layer. On the contrary, the content of GeON is higher for the ZrLaON+F sample (2.6% from the GeON/Ge3d peak-area ratio) than the ZrLaON sample (1.1%). These results indicate that fluorine incorporation can further reduce the oxide traps, beneficial for formation of GeON and block the inter-diffusion of elements near the interface, resulting in the best interface quality and thus electrical properties, as shown for the ZrLaON+F sample above.

4. Conclusion

The effects of ZrLaON passivation interlayer and fluorine-plasma treatment on the interfacial and electrical properties of Ge MOS capacitor with HfTiON gate dielectric are investigated. Experimental results show that the Ge MOS devices with ZrLaON interlayer have less interface states and oxide charges, which can be further reduced by fluorine incorporation. XPS analyses indicate that the ZrLaON passivation layer can effectively suppress the growth of unstable native oxides at the Ge surface, and also fluorine incorporation can suppress the inter-diffusion of elements and reduce the oxide traps at/near the high-k/Ge interface, thus giving good electrical properties of the Ge MOS device. Therefore, the ZrLaON interlayer combined with the fluorine-plasma treatment is a promising way for improving the interface quality and thus obtaining high-performance Ge MOS devices.

Acknowledgments

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