Nonlinear Control of Switched-Capacitor Converter Using Sliding Mode Control Approach

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***Abstract*— Conventional PWM voltage mode or current mode control techniques are commonly used in practice for controlling switched-capacitor converters. However, such control methods are only useful for applications involving small operating regions. This paper discusses the application of nonlinear control in the form of sliding mode control on switched-capacitor converters. The result is an enlarged operating range and hence wider application possibilities. The sliding mode controller adopted in this work is of constant-frequency type that is derived from the indirect sliding mode control technique. The design, analysis, and implementation issues of this controller are detailed in the paper. Experimental results are presented to validate the theoretical design and to illustrate the strength of the proposed controller.**

I. Introduction

With only switches and capacitors in the power stage, the switched-capacitor (SC) converters have the advantages of light weight, small size, and high power density [1], [2]. Such features make them ideal power supplies for mobile electronic systems such as cellular phones, personal digital assistants, and so forth [3]. In fact, the electronic industry is already adopting such converters in various products, and semiconductor companies like Maxim and National Semiconductor are already mass producing them in IC packaged form, e.g. MAX828/829 and LM3351 etc., for commercial applications.

So far, major research activities in the area have been focused on the circuit aspects of the SC converter. The research on its control, which is an important aspect that is limiting its usages, has not received the attention that it deserves. Current industrial practice is relying on conventional PWM voltage or current mode control technique for these converters. As understood, such linear control methods are only useful for operating condition limited to a narrow range. For a wider range of operating condition, the SC converter fails to respond desirably under such control methods. Worse still, the SC converter may possibly become unstable. Hence, to facilitate the applications of SC converters in electronic systems requiring a wide operating condition (e.g. in fuel cell systems) and a fast dynamical response, a nonlinear means of controlling the SC converter is required.

Among the many nonlinear control methods, the sliding mode (SM) control has shown to be highly promising for applications in switching converters as compared to the others for its relative ease of implementation, its excellent robust and stability properties in handling large-signal perturbations and component's uncertainty, and its ability to give a highly consistent dynamic response as pre-determined [4]–[10]. To the authors' knowledge, there is no reported work in the literature on the application of sliding mode control or any nonlinear control methodology on the SC converters.

In view of this, a type of constant-frequency SM controller derived from the indirect SM control technique and implemented in pulsewidth modulation (PWM) form, which offers good large-signal control performances with fast dynamical responses, is proposed for the SC converters in this paper. The various issues concerning the mathematical development and implementation of the controller are reported. Verification and evaluation of this system are conducted through experimental work. Note that the proposed control technique discussed in this paper can be extended to other types of SC converters.

II. Operation and Modeling of Switched-Capacitor Converter

A. Converter Circuit

Fig. 1(a) shows the SC converter circuit considered in this paper. The converter is made up of four externally-controlled switches ($S_1 \sim S_4$), six internally-controlled switches ($D_1 \sim D_6$), four energy transfer capacitors ($C_1 \sim C_4$), and an output filter capacitor C_o that is connected in parallel to the load r_L. The timing diagram for driving the switches is given in Fig. 1(b). Here, u_{S1}, u_{S2}, u_{S3}, and u_{S4} represent the logic states of switches $S_1 \sim S_4$ respectively. The logic 0 and 1 represent respectively the turning off and on of the switches. A more detailed description of this converter can be found in [1]. Briefly, this converter can be viewed in terms of two symmetrical sub-circuits with four topological states per cycle as given in Fig. 2.

With the assumption that all the diodes are ideal, the four topological states can be described as follows.

- State 1: With S_1 on and S_2 off, C_1 and C_2 are connected in series and are being charged up by input voltage source v_i with a current $i_{\mathrm{in}1}$ through resistor $R_{\mathrm{in}1}$. Here, $R_{\mathrm{in}1} = r_{S1} + r_{C1} + r_{C2}$, where r_{S1}, r_{C1}, and r_{C2} are the internal resistances of S_1, C_1, and C_2, respectively. Concurrently, with S_3 off and S_4 on, C_3 and C_4 are discharging their storage energy in parallel to the load r_L and the filter capacitor C_o through the resistances

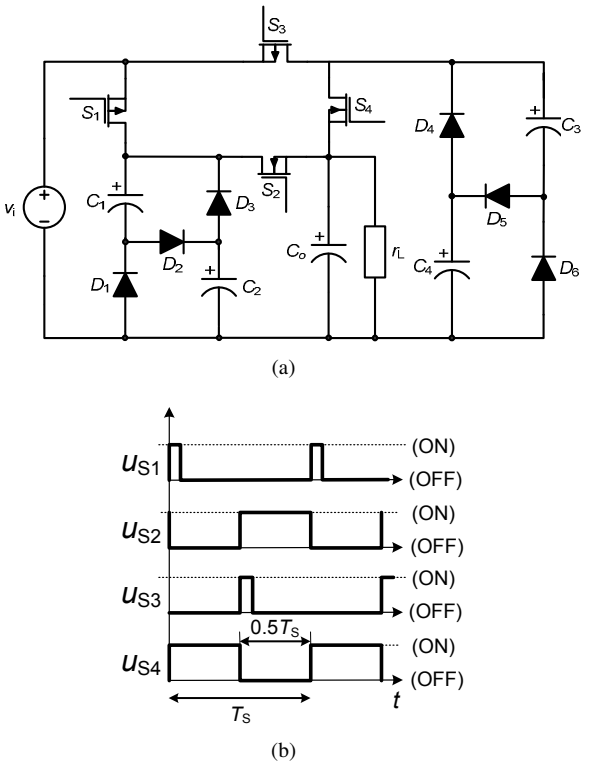


Fig. 1. (a) Switched-capacitor converter and (b) the timing diagram of the converter switches.

R_{C3} and R_{C4}, respectively. Here, the total discharging current i_{out1} from C_3 and C_4 can be equated as $i_{\mathrm{out1}} = -i_{C3} - i_{C4} = i_r + i_{C\mathrm{o}}$, where i_{C3}, i_{C4}, i_r, and $i_{C\mathrm{o}}$ are the currents flowing into C_3, C_4, r_{L}, and C_{o}, respectively. The resistances are $R_{\mathrm{C3}} = 2r_{S4} + r_{C3}$ and $R_{\mathrm{C4}} = 2r_{S4} + r_{C4}$, where r_{S4}, r_{C3} and r_{C4} are the internal resistances of S_4, C_3, and C_4, respectively. v_{C1}, v_{C2}, v_{C3}, and v_{C4} denote the voltages across $C_1 \sim C_4$, respectively; and v_{o} denotes the output voltage of the converter.

- State 2: With S_1 being turned off, the charging up of C_1 and C_2 is halted. However, with S_3 and S_4 still remaining in their previous states, both C_3 and C_4 continue to discharge their storage energy to the load.
- State 3: Similar to State 1 with all switches operating complimentarily to their symmetrical counterparts. With S_3 on and S_4 off, C_3 and C_4 are being charged up in series with a current i_{in2} through resistor R_{in2}. Here, $R_{\mathrm{in2}} = r_{S3} + r_{C3} + r_{C4}$, where r_{S3} is the internal resistance of S_3. Concurrently, with S_1 off and S_2 on, C_1 and C_2 discharge their storage energy in parallel to r_{L} and C_{o} through R_{C1} and R_{C2}, respectively. The total discharging current i_{out2} from C_1 and C_2 can be equated as $i_{\mathrm{out2}} = -i_{C1} - i_{C2} = i_r + i_{C\mathrm{o}}$. Here, $R_{\mathrm{C1}} = 2r_{S2} + r_{C1}$ and $R_{\mathrm{C2}} = 2r_{S2} + r_{C2}$, where r_{S2} is the internal resistance of S_2.
- State 4: Similar to State 2 with all switches operating complimentarily to their symmetrical counterparts. With S_3 being turned off, the charging up of C_3 and C_4 is halted. With S_1 and S_2 still remaining in their previous states, both C_1 and C_2 continue to discharge their storage energy to the load.

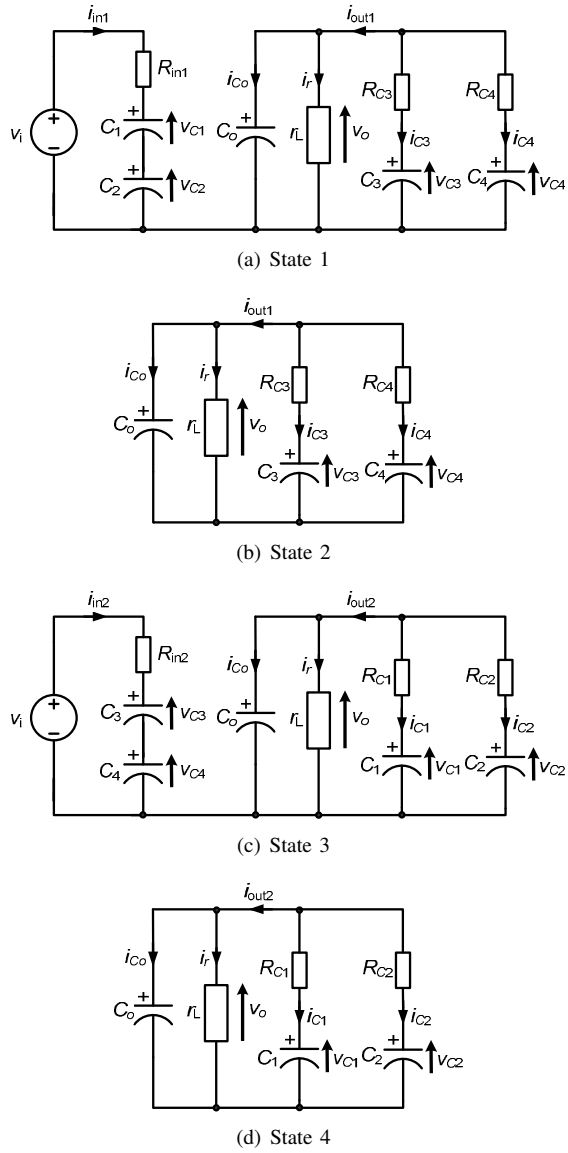


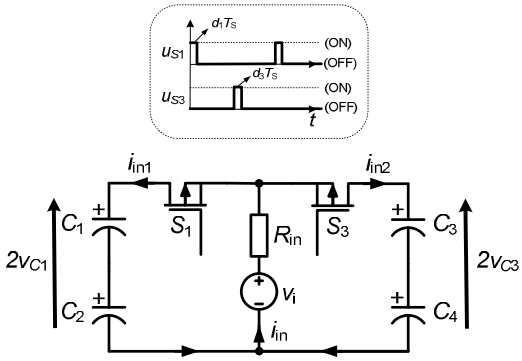
Fig. 2. The four operating states of the switched-capacitor converters.

B. A Simplified Model for Controller Development

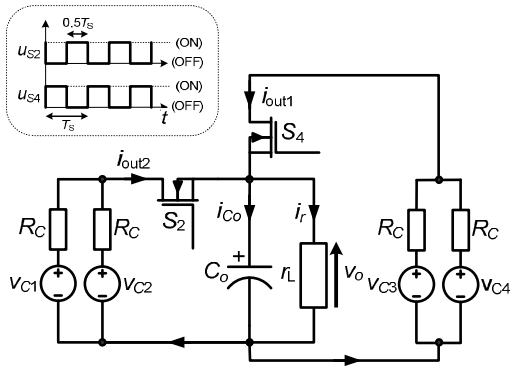
Energy from the input voltage source is alternatively delivered to the series-connected capacitor pairs (C_1, C_2) and (C_3, C_4). The stored energy is then alternatively delivered from the parallel-connected pairs (C_1, C_2) and (C_3, C_4) to the load. Assuming the two circuit phases are symmetrical[1] and that $R_{\mathrm{in}} = R_{\mathrm{in1}} = R_{\mathrm{in2}}$; $R_C = R_{C1} = R_{C2} = R_{C3} = R_{C4}$; $v_{C1} = v_{C2}$; and $v_{C3} = v_{C4}$, the charging and discharging operations can be simplified into the models shown in Figs. 3(a) and 3(b), with $S_1 \sim S_4$ being ideal switches. Note that the charging and discharging operations given in the figures must still be synchronized such that when u_{S1} is 1, u_{S2} must

[1]In the case where the phases are asymmetrical, consideration and development of individual controller for each of the phases can be easily performed following the same procedure.

be 0, and vice versa. Similarly, when u_{S3} is 1, u_{S4} must be 0, and vice versa.



(a) Charging



(b) Discharging

Fig. 3. (a) Charging operation of series-connected capacitors and (b) discharging operation of parallel-connected capacitors.

According to Fig. 3(a), the instantaneous input current flow from the source to the circuits can be expressed as

$$i_{\text{in}} = i_{\text{in1}} u_{S1} + i_{\text{in2}} u_{S3}, \tag{1}$$

where

$$\begin{cases} i_{\text{in1}} = \frac{v_{\text{i}} - 2v_{C1}}{R_{\text{in}}} = C_1 \frac{dv_{C1(\text{C})}}{dt} \\ i_{\text{in2}} = \frac{v_{\text{i}} - 2v_{C3}}{R_{\text{in}}} = C_3 \frac{dv_{C3(\text{C})}}{dt} \end{cases}. \tag{2}$$

From Fig. 3(b), the instantaneous current flowing through the output filter capacitor can be expressed as

$$i_{C\text{o}} = i_{\text{out1}} u_{S4} + i_{\text{out2}} u_{S2} - i_r \tag{3}$$

where

$$\begin{cases} i_{\text{out1}} = 2\frac{v_{C3} - v_{\text{o}}}{R_C} = -2C_3 \frac{dv_{C3(\text{D})}}{dt} \\ i_{\text{out2}} = 2\frac{v_{C1} - v_{\text{o}}}{R_C} = -2C_1 \frac{dv_{C1(\text{D})}}{dt} \end{cases}. \tag{4}$$

Recall that for any lossless capacitor C, the change of energy due to charging and discharging over a fixed time period can be respectively written as $\Delta E_{C(\text{charging})} = \frac{1}{2}C({V_2}^2 - {V_1}^2)$ and $\Delta E_{C(\text{discharging})} = \frac{1}{2}C({V_1}^2 - {V_2}^2)$, where V_1 and V_2 represent the voltage levels of the capacitor after being discharged and charged, respectively. Now, by applying the principle of energy balance to the charging and discharging operations of the capacitor circuit, i.e., $\Delta E_{C(\text{charging})} = -\Delta E_{C(\text{discharging})}$, it is possible to deduce that to achieve energy balance within a switching cycle, the increase of the voltage during the charging operation must be equivalent to the negative drop of the voltage during the discharging operation, i.e.,

$$\Delta v_{C(\text{charging})} = -\Delta v_{C(\text{discharging})}, \tag{5}$$

where $\Delta v_{C(\text{charging})} = V_2 - V_1$ and $\Delta v_{C(\text{discharging})} = V_1 - V_2$ represent the change in capacitor voltage during charging and discharging, respectively. Next, consider only the charging and discharging operations of capacitor C_1 of the proposed SC converter. With the discharging operation of the capacitor occurring for the time period of $0.5T_{\text{S}}$, the change in voltage during discharging can be written as

$$\begin{aligned} \Delta v_{C1(\text{discharging})} &= \int_0^{0.5T_{\text{S}}} \frac{dv_{C1(\text{D})}}{dt} \cdot dt \\ &= \frac{dv_{C1(\text{D})}}{dt}(0.5T_{\text{S}}) \end{aligned} \tag{6}$$

under the assumption that the discharging operation occurs linearly. This is possible since the discharging period is much smaller than the discharging time constant, i.e., $0.5T_{\text{S}} \ll \tau_D = (2r_L + R_C)C_1$. On the other hand, given that the charging operation of C_1 occurs only for the time period d_1T_{S}, the change in voltage during charging is expressed as

$$\Delta v_{C1(\text{charging})} = \int_0^{d_1T_{\text{S}}} \frac{dv_{C1(\text{C})}}{dt} \cdot dt = \frac{dv_{C1(\text{C})}}{dt}(d_1T_{\text{S}}) \tag{7}$$

since the charging operation is assumably linear with the charging period being much smaller than the charging time constant, i.e., $d_1T_{\text{S}} \ll \tau_C = R_{\text{in}}\frac{C_1C_2}{C_1+C_2} = 0.5R_{\text{in}}C_1$. Then, the substitution of (6) and (7) into (5), and then with the consideration of (2), equation (5) can be rearranged as

$$\frac{dv_{C1(\text{D})}}{dt} = -(2d_1)\frac{dv_{C1(\text{C})}}{dt} = \frac{2(2v_{C1} - v_{\text{i}})}{R_{\text{in}}C_1}d_1. \tag{8}$$

Using the same principle, a similar equation can be derived for $\frac{dv_{C3(\text{D})}}{dt}$. Finally, the substitution of these equations into (4) gives the average form of

$$\begin{cases} i_{\text{out1(ave)}} = \frac{4(v_{\text{i}} - 2v_{C3})}{R_{\text{in}}}d_3 \\ i_{\text{out2(ave)}} = \frac{4(v_{\text{i}} - 2v_{C1})}{R_{\text{in}}}d_1 \end{cases} \tag{9}$$

and the state-space form of

$$\begin{cases} i_{\text{out1}} = \frac{4(v_{\text{i}} - 2v_{C3})}{R_{\text{in}}}u_{S3} \\ i_{\text{out2}} = \frac{4(v_{\text{i}} - 2v_{C1})}{R_{\text{in}}}u_{S1} \end{cases}. \tag{10}$$

The above equation gives the relationship between the output current (left-hand side) and the input current (right-hand side) that is formulated using energy balance. What it represents is that for any amount of energy discharged from a capacitor with a current flow $i_{\text{out}n}$, the necessary charging action required to replace the discharged energy to achieve instantaneous energy balance within a switching cycle in the same capacitor, is given as $\frac{4(v_{\text{i}} - 2v_{Cm})}{R_{\text{in}}}d_m$. However, for the case of the SC converters which have operations that are alternative such that while one capacitor-circuit phase is discharging, the other capacitor-circuit phase is charging, equation (10) must be reformulated as

$$\begin{cases} i_{\text{out1}} = \frac{4(v_{\text{i}} - 2v_{C1})}{R_{\text{in}}}u_{S1} \\ i_{\text{out2}} = \frac{4(v_{\text{i}} - 2v_{C3})}{R_{\text{in}}}u_{S3} \end{cases} \tag{11}$$

so that the discharging of C_3 and C_4 with the combined current of i_{out1} will prompt the corresponding charging action for C_1 and C_2 such that immediate energy balance is achieved. This reformulation is also carried out for the case of i_{out2}.

III. Sliding Mode Control of Switched-Capacitor Converter

The switches S_2 and S_4 are complementarily turned on and off for a duty cycle of 50% in each cycle. Therefore, the only controllable actions for the regulation are those that are triggered by S_1 and S_3. Since the converter is phase symmetrical, it is sufficient to consider only one phase when designing the controller. The remaining discussion in this section is focused on the design for switch S_1 in the time period between 0 to $0.5T_{\text{S}}$ with S_2 turned off and S_4 turned on, i.e., State 1 and State 2. During this period, the current flowing through the filter capacitor is given as

$$i_{Co} = i_{\text{out1}} - i_r. \tag{12}$$

Using (11), this equation can be expressed as

$$i_{Co} = \frac{4(v_{\text{i}} - 2v_{C1})}{R_{\text{in}}} u_{S1} - i_r. \tag{13}$$

A. Sliding Surface of Proposed Controller

With a switching function $u_{S1} = \frac{1}{2}(1 + \text{sign}(\sigma_1))$, the sliding function of the proposed controller is chosen to be a proportional-integral (PI) type[2] with linear combination of two state variables, i.e.,

$$\sigma_1 = \alpha_{S1} x_1 + x_2 \tag{14}$$

where α_{S1} represents the sliding coefficient. Here, the adopted controlled state variables are the *voltage error* x_1, and the *integral of the voltage error* x_2, which are expressed as

$$\begin{cases} x_1 = V_{\text{ref}} - v_{\text{o}} \\ x_2 = \int x_1 \, dt = \int (V_{\text{ref}} - v_{\text{o}}) \, dt \end{cases}, \tag{15}$$

where V_{ref} denotes the reference voltage of the controller.

B. Dynamical Model of Proposed Controller/Converter System and Its Equivalent Control

The time differentiation of x_1 and x_2 gives the dynamical model of the proposed SC converter system as

$$\begin{cases} \frac{dx_1}{dt} = \frac{d[V_{\text{ref}} - v_{\text{o}}]}{dt} = -\frac{i_{Co}}{C_{\text{o}}} \\ \frac{dx_2}{dt} = x_1 = V_{\text{ref}} - v_{\text{o}} \end{cases}. \tag{16}$$

The equivalent control signal of switch 1 of the proposed controller, i.e., $u_{S1\text{eq}}$, can be obtained by solving $\frac{d\sigma_1}{dt} = 0$ using (13) and (16), which gives

$$u_{S1\text{eq}} = \frac{i_r + \frac{C_{\text{o}}}{\alpha_{S1}}(V_{\text{ref}} - v_{\text{o}})}{\frac{4(v_{\text{i}} - 2v_{C1})}{R_{\text{in}}}} \tag{17}$$

[2]The decision for choosing a PI sliding surface over the conventionally adopted PID sliding surface is due to a significant increase in complexity with the inclusion of the derivative control. This would be unpractical for circuit implementation.

where $0 \le u_{S1\text{eq}} < 1$. In terms of implementing the controller through the pulsewidth modulator [7]–[9], we can set

$$\begin{cases} v_{\text{C(S1)}} = K\left[i_r + \frac{C_{\text{o}}}{\alpha_{S1}}(V_{\text{ref}} - v_{\text{o}})\right] \\ \hat{v}_{\text{ramp(S1)}} = K\left[\frac{4(v_{\text{i}} - 2v_{C1})}{R_{\text{in}}}\right] \end{cases} \tag{18}$$

where $v_{\text{C(S1)}}$ is the control signal to the pulsewidth modulator and $\hat{v}_{\text{ramp(S1)}}$ is the peak magnitude of the constant frequency ramp signal for generating the control signal u_{S1} for switch S_1. Likewise, for switch S_3, the required control signal u_{S3} can be generated using another pulsewidth modulator with the following inputs:

$$\begin{cases} v_{\text{C(S3)}} = K\left[i_r + \frac{C_{\text{o}}}{\alpha_{S3}}(V_{\text{ref}} - v_{\text{o}})\right] \\ \hat{v}_{\text{ramp(S3)}} = K\left[\frac{4(v_{\text{i}} - 2v_{C3})}{R_{\text{in}}}\right] \end{cases}. \tag{19}$$

C. Architecture of Proposed Controller

Fig. 4 shows an overview of the proposed SM controller for the SC converter with parameters $\gamma = \frac{C_{\text{o}}}{\alpha_{S1}} = \frac{C_{\text{o}}}{\alpha_{S3}}$ and $\eta = \frac{4}{R_{\text{in}}}$. The construction of control signals $v_{\text{C(S1)}}$ and $v_{\text{C(S3)}}$ is common and employs the same circuit. Two ramp generator circuits that have varying peak voltage with the change of input voltage or capacitor voltage are required for the nonlinear compensation. Note that the frequency of the ramp signal must be synchronized to the switching signals u_{S2} and u_{S4}, which are basically 50% duty cycle pulses complementing one another. The output of the respective pulsewidth modulators are multiplied with the logic states of u_{S4} and u_{S2} using a logic AND operator.

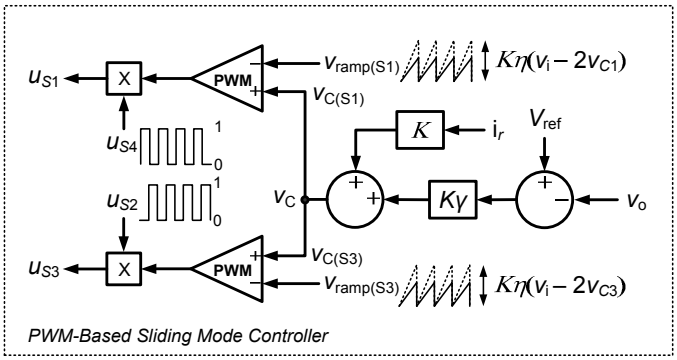


Fig. 4. Proposed SM controller for the SC converter.

D. Existence Condition

By inspecting the local reachability condition $\lim_{\sigma_1 \to 0} \sigma_1 \cdot \frac{d\sigma_1}{dt} < 0$, the existence condition is derived as

$$\begin{cases} \frac{v_{\text{o(SS)}}}{r_{\text{L(min)}}} < \frac{4(v_{\text{i(min)}} - 2v_{C1(\text{max})})}{R_{\text{in}}} \\ \alpha_{S1} > 0 \end{cases} \tag{20}$$

and

$$\begin{cases} \frac{v_{\text{o(SS)}}}{r_{\text{L(min)}}} < \frac{4(v_{\text{i(min)}} - 2v_{C3(\text{max})})}{R_{\text{in}}} \\ \alpha_{S3} > 0 \end{cases}, \tag{21}$$

where $v_{\text{o(SS)}}$ denotes the expected steady-state output voltage (i.e. V_{ref}); $r_{\text{L(min)}}$ denotes the minimum output load resistance; $v_{\text{i(min)}}$ denotes the minimum input voltage; and

$v_{C1(\max)}$ and $v_{C3(\max)}$ denote the expected maximum voltage across capacitors C_1 and C_3 when the converter is operating at full-load condition. The selection of the controller's gain parameters α_{S1} and α_{S3} and the design of the converter must comply with these inequalities. This assures the existence of the SM operation at least in the small region of the origin for all operating conditions up to full load.

E. Stability Condition

With the proposed system, the linearized ideal sliding dynamics can obtained as

$$\begin{cases} \frac{d\tilde{v}_{C1}}{dt} = a_{11}\tilde{v}_{C1} + a_{12}\tilde{v}_{C3} + a_{13}\tilde{v}_{\mathrm{o}} \\ \frac{d\tilde{v}_{C3}}{dt} = a_{21}\tilde{v}_{C1} + a_{22}\tilde{v}_{C3} + a_{23}\tilde{v}_{\mathrm{o}} \\ \frac{d\tilde{v}_{\mathrm{o}}}{dt} = a_{31}\tilde{v}_{C1} + a_{32}\tilde{v}_{C3} + a_{33}\tilde{v}_{\mathrm{o}} \end{cases} \tag{22}$$

where

$$a_{11} = -\frac{1}{2R_C C_1}; \quad a_{12} = 0;$$
$$a_{13} = \frac{1}{4C_1}\left(\frac{1}{R_{\mathrm{L}}} + \frac{2}{R_{\mathrm{C}}} - \frac{C_{\mathrm{o}}}{\alpha_{S1}}\right); \quad a_{21} = 0;$$
$$a_{22} = -\frac{1}{2R_C C_3}; \quad a_{23} = \frac{1}{4C_3}\left(\frac{1}{R_{\mathrm{L}}} + \frac{2}{R_{\mathrm{C}}} - \frac{C_{\mathrm{o}}}{\alpha_{S3}}\right);$$
$$a_{31} = a_{32} = \frac{1}{R_C C_{\mathrm{o}}}; \quad a_{33} = -\left(\frac{2}{R_C} + \frac{1}{R_L}\right)\frac{1}{C_{\mathrm{o}}}. \tag{23}$$

The derivation is performed with the adoption of the following static equilibrium conditions, $R_{\mathrm{L}} = r_{\mathrm{L}}$ and $V_{\mathrm{ref}} - V_{\mathrm{o}} = 0$.

Next, by applying Routh criterium to the characteristic equation of equation (23), it can be shown that the system will be stable if $p_1 > 0$, $p_2 > \frac{p_3}{p_1}$, and $p_3 > 0$ where

$$\begin{cases} p_1 = a_{33} - a_{11} - a_{22} \\ p_2 = a_{11}a_{22} + a_{11}a_{33} + a_{22}a_{33} - a_{13}a_{31} - a_{23}a_{32} \\ p_3 = a_{11}a_{23}a_{32} + a_{13}a_{22}a_{31} - a_{11}a_{22}a_{33} \end{cases}. \tag{24}$$

IV. Experimental Results and Discussions

A. Steady-State Performance

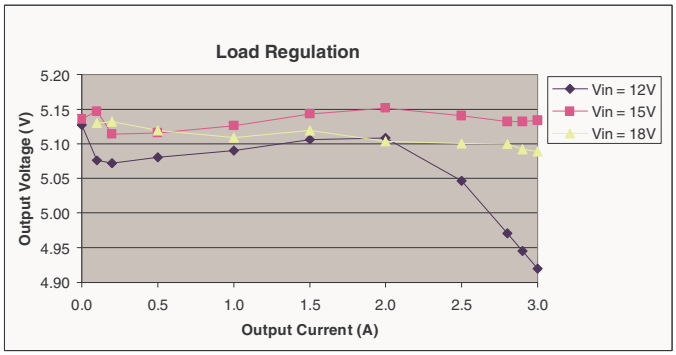


Fig. 5. Plot of experimentally measured DC output voltage v_{o} versus output load current at input voltages of $v_{\mathrm{i}} = 12$ V, 15 V, and 18 V.

A hardware prototype is developed for a 15 W (5 V, 3 A) SC converter with specification given in Table IV. The parameters of the SM controller are $K = 0.2$, $\eta = 11.76$, and $\gamma = 2.52 + \frac{20991}{s}$. Note that the pole term in the γ serves to reduce the steady-state error of the converter. The detailed description can be found in [9]. Fig. 5 shows the measured DC output voltage against the different operating load currents at input voltage conditions of 12 V (minimum), 15 V (nominal), and 18 V (maximum). The result shows good load regulation properties for this range of operating condition with the largest v_{o} deviation occurring at $v_{\mathrm{i}} = 12$ V being 0.20 V (i.e., around 4 % of v_{od}). The measurement also shows good line regulation with the largest v_{o} deviation occurring at $r_{\mathrm{L}} = 1.67\ \Omega$ being 0.21 V (i.e., around 4.2 % of v_{od}).

B. Dynamic Performance

The dynamical property of the proposed controller in handling large-signal load disturbances under wide input voltage condition is compared to that of a conventional PWM voltage mode controller. Figs. 6(a)–6(c) show the experimental output voltage ripple waveforms of the PWM voltage mode controlled SC converter operating at a load resistance that alternates between $r_{\mathrm{L}} = 1.67\ \Omega$ and $r_{\mathrm{L}} = 16.67\ \Omega$ for various input voltages. The controller has been optimally tuned for the condition shown in Fig. 6(b) with a settling time of around 1 ms. It can be observed that with this controller, the worst-case operating condition occurs at $v_{\mathrm{i}} = 12$ V with a settling time of around 5.0 ms (see Fig. 6(a)). Figs. 6(d)–6(f) show the output voltage ripple waveforms of the proposed SM controlled SC converter captured at similar operation conditions. It can be seen that at input voltage $v_{\mathrm{i}} = 15$V and 18 V, the transient settling time of this converter is similar (around 1 ms) to that of the converter with the conventional PWM voltage controller (see Figs. 6(b), 6(c), 6(e), and 6(f)). However, at $v_{\mathrm{i}} = 12$ V, which represents the worst-case operating condition of this converter, the maximum settling time is 3.5 ms. The time taken is 30 % shorter than that with the conventional PWM voltage controller which took around 5 ms. Thus, the advantage of the proposed SM controller in giving fast dynamical responses over a wide range of operating conditions is demonstrated.

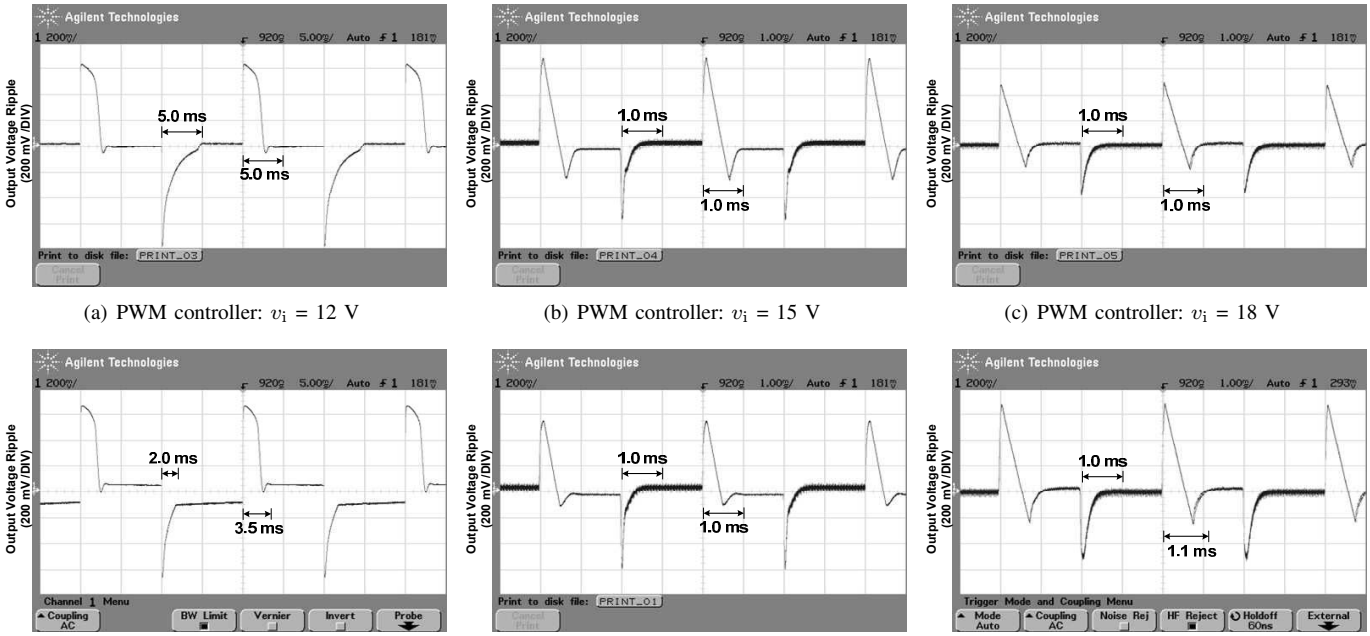
V. Conclusion

A constant-frequency sliding mode controller which gives good control performances over a wide range of operating conditions is proposed for the switching capacitor converters. The various issues concerning the mathematical development and implementation of the controller are discussed in the paper. The experimental results verified that when the switching capacitor converter is operated over a wide range of input voltage, the proposed controller gives a faster dynamical response as compared to the conventional PWM voltage mode controller. This would mean that using the proposed controller, the operating range of the switched-capacitor converters can be enlarged, and could lead to wider application possibilities. Nevertheless, the tradeoff of using this controller over the conventional controller is the requirement for an additional current sensor and inheriting a more complex circuit architecture.

Acknowledgment

The authors would like to thank Mr. S. Y. Lam for developing the prototype and conducting the experiment.

Description	Parameter	Nominal Value
Input voltage	v_{i}	12 V $\leq v_{\mathrm{i(nominal)}} = 15\ V \leq$ 18 V. V
Charging operation switches	S_1, S_3	IRF9530 p-type MOSFET, 300 mΩ
Discharging operation switches	S_2, S_4	IRF540 n-type MOSFET, 85 mΩ
Storage Capacitors	C_1, C_2, C_3, C_4	47 μF, 20 mΩ
Output Capacitors	C_{o}	100 μF, 35 mΩ
Switching frequency	f_{S}	92.25 kHz
Charging operation resistance	$R_{\mathrm{in}} = r_{S1} + r_{C1} + r_{C2}$	340 mΩ
Discharging operation resistance	$R_C = 2r_{S2} + r_{C1}$	190 mΩ
Load resistance	r_{L}	$r_{\mathrm{L(min)}} = 1.67\ \Omega$, $r_{\mathrm{L(max)}} = 16.67\ \Omega$
Desired output voltage	V_{od}	5 V



(a) PWM controller: v_{i} = 12 V (b) PWM controller: v_{i} = 15 V (c) PWM controller: v_{i} = 18 V

(d) SM controller: v_{i} = 12 V (e) SM controller: v_{i} = 15 V (f) SM controller: v_{i} = 18 V

Fig. 6. Experimental waveforms of the output voltage ripple $\widetilde{v_{\mathrm{o}}}$ of the SC converter with the conventional PWM voltage controller (a, b, c) and with the proposed SM controller (d, e, f), operating at input voltages of 12 V (minimum), 15 V (nominal), and 18 V (maximum) and alternating between load resistances 1.67 Ω (minimum) and 16.67 Ω (maximum).

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