Theoretical Study of Switching Power Converters with Power Factor Correction and Output Regulation

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***Abstract*—This paper discusses a systematic method for deriving basic converter configurations that achieve power factor correction (PFC) and voltage regulation. The discussion begins with a general three-port representation of power supplies that provide PFC and voltage regulation. Based on this representation and a power flow consideration, a systematic procedure is derived to generate all possible minimal configurations. It is found that two basic converters are, in general, required for implementing any of the possible configurations. Among these configurations only a few have been known previously and been used in practice. The various possible configurations are compared in terms of their theoretical efficiency and control requirements of the basic constituent converters.**

***Index Terms*—Circuit synthesis, control, dc/dc converters, power factor correction, switching regulators.**

I. Introduction

HIGH-POWER factor and low input-current harmonics are becoming mandatory design criteria for switching power supplies, in addition to a tight output voltage regulation. Recently, there have been numerous attempts in combining a so-called power-factor-correction (PFC) switching stage with a conventional dc/dc converter to form a high-power-factor voltage regulator which converts power from the ac mains to a resistive load [1]–[10]. The PFC stage is typically a switching converter operating in discontinuous conduction mode (DCM) or in continuous conduction mode (CCM) under a special current-mode control scheme. Of much research interest is, moreover, the amalgamation of two stages to form the required PFC voltage regulator. In much of the literature such an amalgamation is referred to as single-stage design, despite the fact that two switching stages are invariably contained in the combined system [3]–[6].

The basic requirement of the aforementioned combined system, to which we simply refer as the PFC regulator, is the presence of an energy storage element which buffers the difference between the instantaneous input power and the output power. For the case of the unity power factor and perfect regulation, the power difference p_c that has to be buffered is given by

$$p_c(t) = \hat{e}\hat{i}_{\rm in}\sin^2 2\pi f_m t - P_o \tag{1}$$

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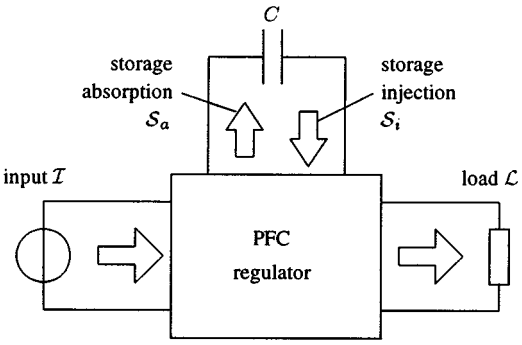

Fig. 1. Three-port model of a PFC switching regulator.

where $\hat{e}$ is the peak input voltage, $\hat{i}_{\rm in}$ is the peak input current, f_m is the mains frequency, and P_o is the output power [11]. It is worth noting that such continuous power buffering occurs at twice the mains frequency, which is usually a few orders of magnitude below the switching frequency of the individual converter stages. Thus, in analyzing a PFC regulator, care must be taken in differentiating between the low-frequency (around the mains frequency) and high-frequency (around the switching frequency) power flows which take place, respectively, between and within the power stages.

We consider the general configuration of a voltage regulator with PFC capability as a three-port network terminating in an input voltage, a low-frequency storage element, and an output load, as shown in Fig. 1. Within the three-port, high-frequency power flows occur as usual for switching converters. In this paper, however, we will focus on the low-frequency power flows into and out of the three-port network and attempt to derive a general procedure for synthesizing minimal practical PFC voltage regulator circuits based on the use of only two basic converters. The possible circuit configurations will then be compared in terms of their efficiency and control requirements. A particularly illuminating result of this study is that efficient PFC regulators can be constructed by selecting appropriate configurations that minimize redundant processing of power by the two constituent converters, as will be demonstrated in the sequel. Furthermore, the study of the control problem provides formal criteria in selecting control parameters and operating modes and clarifies some previous misconceptions in the design of single-stage PFC regulators.

II. Three-Port Model of Switching Regulators with PFC

Most practical power supplies convert an input voltage to an output voltage. The storage needed for PFC is conveniently

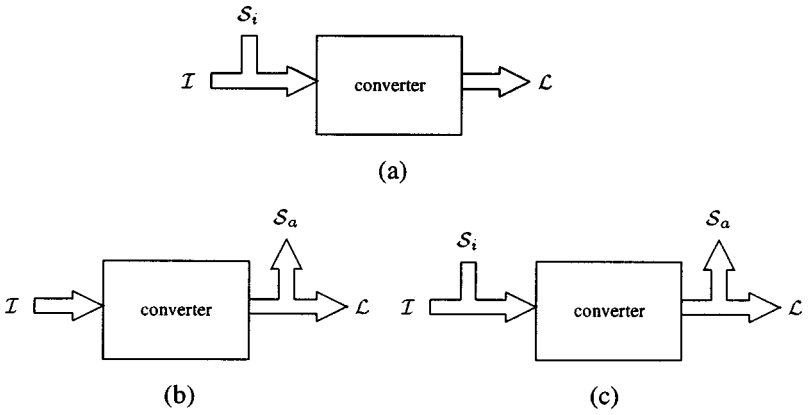

Fig. 2. Three possible types of multiple connection to a converter. (a) Converter's input connected to two ports. (b)Converter's output connected to two ports. (c) Converter's input and output each connected to two ports.

capacitive although, in theory, inductive storage can also be employed under certain conditions [12]. Thus, we may consider a PFC regulator as a three-port network which comprises a number of simple voltage-terminated converters, i.e., the simple buck, boost, and buck-boost converters, which connect the input voltage, output load, and capacitive storage.

A. Minimum Number of Converters Needed

Suppose the input and the load allow energy to be transferred in only one direction, while the storage element allows a bidirectional energy flow, as indicated by the arrows in Fig. 1. In this representation, power goes into the three-port network via the input port and the storage port and power goes out via the load port and the storage port. Effectively, we may treat the storage port as being composed of a power injection and a power absorption port.

As a prelude to the subsequent analysis, we first address the complexity of the circuit construction that is required of a PFC regulator. Specifically, we wish to find the minimum number of simple converters that are needed to ensure the right amount of power buffered in the storage at any time.

Theorem 1: Assume that a simple converter has one input port and one output port. The minimum number of simple converters needed to construct a PFC regulator is equal to two.

Proof: Observe that we need to control only two of the three ports of the PFC regulator since the remaining port will automatically be controlled as a result of power conservation. Since each constituent converter is single-input-single-output, it is not possible for a converter to have full separate control of two or more power input (or output) ports of the PFC regulator simultaneously. Furthermore, if two or more converters are used and each port is connected to at least one converter, then at least two of the ports will be fully controlled, $q.e.d.$

B. Conceptual Connections of Converters

For ease of reference we use $\mathcal{I}, \mathcal{L}, \mathcal{S}_a$, and $\mathcal{S}_i$ to denote, respectively, the power flow at the input port, load port, storage absorption, and storage injection ports, as shown in Fig. 1.

Suppose each constituent converter has one power input port and one power output port. Two basic rules govern the connection.

1) In order for the PFC regulator to perform the necessary power buffering function, there must exist power conversion from $\mathcal{I}$ to $\mathcal{S}_a$ and from $\mathcal{S}_i$ to $\mathcal{L}$.
2) In order to ensure the minimal number of power flow paths (so as to avoid redundant power processing), no converter should convert power from a port back to itself, i.e., input-to-input, storage-to-storage, and load-to-load conversions should be avoided.

Before we attempt to derive the possible connections, we observe that a converter can possibly connect its input or output to more than one power ports of the PFC regulator. Fig. 2 shows the three possibilities, regardless of the aforementioned connection rules. In general, we let n be the number of converters having any of these connections. We now sketch all possible connections of converters in a PFC regulator as follows.

Case 1: $n = 0$. Suppose we first connect $\mathcal{I}$ (or $\mathcal{S}_i$) to a converter's input port and $\mathcal{S}_a$ (or $\mathcal{L}$) to its output port. Then, we connect another converter to the remaining ports of the PFC regulator. We may denote the possible connections as follows:

$$\text{Case 1a:} \quad \begin{cases} \mathcal{I} \mapsto \mathcal{S}_a \\ \mathcal{S}_i \mapsto \mathcal{L} \end{cases} \tag{2}$$

$$\text{Case 1b:} \quad \begin{cases} \mathcal{I} \mapsto \mathcal{L} \\ \mathcal{S}_i \mapsto \mathcal{S}_a \end{cases} \quad \text{(rejected)} \tag{3}$$

where $\mapsto$ denotes power conversion through a converter or precisely a mapping from a power flow to another power flow. Clearly, case 1b should be rejected as it violates the aforementioned connection rules.

Case 2: $n = 1$. With no loss of generality we assume that when a power port is connected to two converters simultaneously, power is split in a ratio of k to $(1-k)$, where $0 < k < 1$. It is readily shown that the following connections satisfy the basic connection rules

$$\text{Case 2a:} \quad \begin{cases} k\mathcal{I} + \mathcal{S}_i \mapsto \mathcal{L} \\ (1-k)\mathcal{I} \mapsto \mathcal{S}_a \end{cases} \tag{4}$$

$$\text{Case 2b:} \quad \begin{cases} \mathcal{I} \mapsto \mathcal{S}_a + k\mathcal{L} \\ \mathcal{S}_i \mapsto (1-k)\mathcal{L} \end{cases} \tag{5}$$

where $+$ denotes algebraic addition. Other connections have been omitted since, like Case 1b, they violate the connection rules. (Readers can verify this easily.)

Case 3: $n = 2$. We assume that input power is split in a ratio of k to $(1-k)$ when it is injected into two converters simultaneously and that the output power is combined at a ratio of k' to $(1-k')$ from the outputs of two converters, where $0 < k < 1$ and $0 < k' < 1$. The only connection that does not violate the connection rules is

$$\text{Case 3:} \quad \begin{cases} k\mathcal{I} \mapsto \mathcal{S}_a + k'\mathcal{L} \\ (1-k)\mathcal{I} + \mathcal{S}_i \mapsto (1-k')\mathcal{L} \end{cases}. \tag{6}$$

Thus, we may conclude that any PFC regulator as represented by the three-port network of Fig. 1 can be constructed by a minimum of two simple converters and that four possible types of connections are available, as illustrated above by Cases 1a, 2a, 2b and 3. In Section III, we will discuss a systematic procedure for deriving all possible minimal circuit configurations that fulfill the dual requirement of PFC and voltage regulation.

C. Low-Frequency Versus High-Frequency Power Flows

As was mentioned previously, it is important to differentiate between low-frequency power flow and high-frequency power flow. Within a converter, power flow occurs at the switching frequency which is typically several orders of magnitude above the mains frequency. This high-frequency (switching frequency) power flow is controlled, usually through the duty cycle or frequency modulation, to result in a certain overall low-frequency power flow function that is required by the design specification. Thus, the power flows into and out of the three-port model are all low-frequency. A simple formulation of the power flow through a converter is as follows. First, we assume that any converter can be controlled through variation of one or more parameters (typically duty cycle and switching frequency) and that such control affects the low-frequency behavior of the converter. For the sake of theoretical consideration, we let $\xi(t)$ and $\psi(t)$ be the control parameters of a switching converter. Suppose the low-frequency power flow P through a given converter for given input and output conditions is

$$P|_{v_i(t),v_o(t)} = F(\xi(t), \psi(t)) \tag{7}$$

which is dictated by the circuit topology. Also, suppose that the required low-frequency power flow function is $f(t)$. For example, for a PFC converter, $f(t)$ takes the form of

$$f(t) = 2P_o \sin^2 2\pi f_m t \tag{8}$$

and for a voltage regulator, it is given by

$$f(t) = P_o \tag{9}$$

where P_o is the output power level. The usual control problem is to find $\xi(t)$ and $\psi(t)$ such that the power flow through the converter fulfills the requirement, i.e.,

$$F(\xi(t), \psi(t)) = f(t). \tag{10}$$

It should be stressed that since PFC is a low-frequency requirement, $F(\cdot)$ is a low-frequency function in the steady state when it is controlled to satisfy the PFC requirement. We will use this theoretical formulation in Section VI to consider the formal control requirement of a PFC voltage regulator.

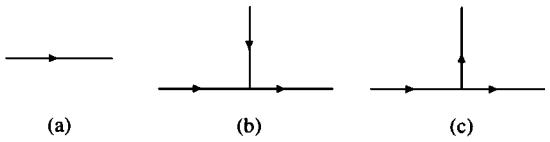

Fig. 3. Power flow subgraphs. (a) Type I. (b) Type II. (c) Type III.

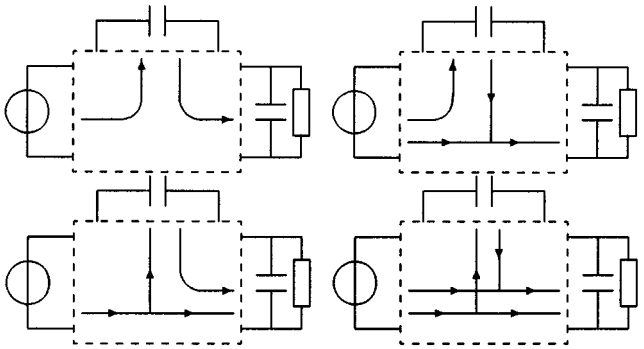

Fig. 4. Power flow graphs for PFC regulators. (a) Type I-I. (b) Type I-II. (c) Type I-III. (d) Type II-III.

III. Configurations of PFC Regulators Based on Power Flow Graphs

Since the primary objective of a PFC regulator is to transfer power from the input port to the load port with low-frequency buffering in the storage element, we begin with the basic process of power flow between the three ports of a PFC regulator.

A. Power Flow Sub-Graphs

We introduce, for ease of presentation, power flow graphs for describing the way in which power is transferred among the three ports. The branches in a power flow graph denote the paths through which power is being transferred and the arrows on the branches indicate the direction of power flow. One or more branches form a power flow subgraph or, simply, a subgraph. For a three-port network, it is clear that only three types of subgraphs can be used to connect the ports.

Type I: Power is transferred from one port to another port [Fig. 3(a)].

Type II: Power is transferred from two ports to one port [Fig. 3(b)].

Type III: Power is transferred from one port to two ports [Fig. 3(c)].

Remarks: The power flow subgraph is introduced here as an alternative and convenient tool for classifying the possible types of power flow scenarios. In fact, as we will see, the above Types I, II, and III subgraphs are closely related to the connection cases studied previously in Section II-B.

B. Power Flow Graphs

Now we can construct the complete power flow graph for a PFC regulator using the three types of subgraphs of Fig. 3. Clearly, there are only four possible constructions, each comprising two subgraphs. For ease of reference, we denote the complete power flow graph by Type I-I if it involves two Type I subgraphs. For a power flow graph that involves one Type I subgraph and one Type II subgraph, we refer to it as Type I-II.

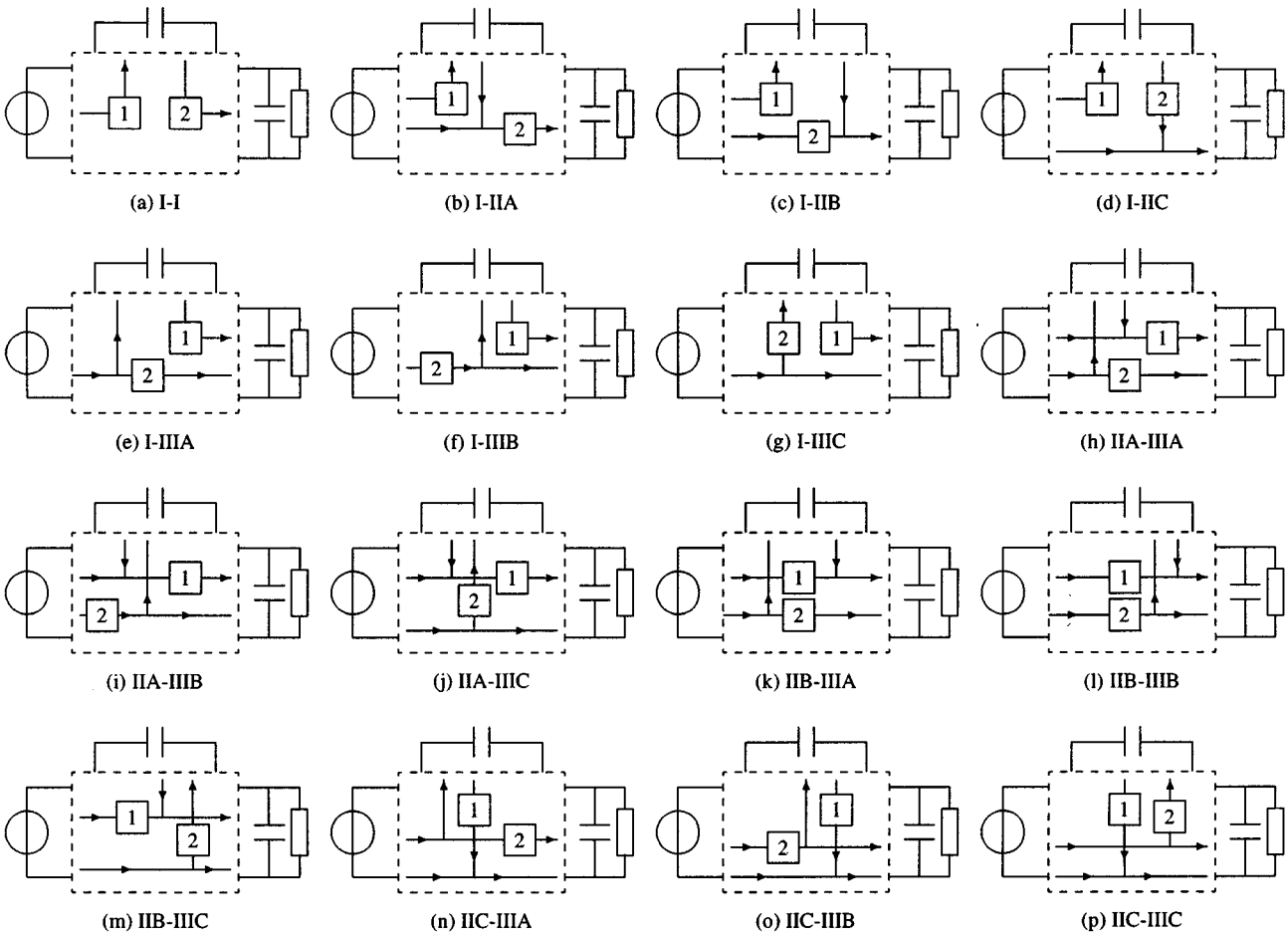

Fig. 5. Configurations of PFC regulators in terms of power flow. Solid square boxes denote simple converters.

Likewise, we also have Type I-III and Type II-III power flow graphs, as shown in Fig. 4.

Now, a moment's reflection will convince us that these power flow graphs effectively represent the connection Cases 1a, 2a, 2b and 3 of Section II-B. The use of power flow graphs provides a more systematic solution to the classification problem.

C. Minimal Configurations of PFC Regulators

Finally, since the minimal configuration requires two simple converters, we complete the derivation by putting two converters in the appropriate paths of the power flow graph. In particular, we consider putting one converter to each subgraph in order to take full control of power flow to and/or from each port. Also, for each Type II and Type III subgraph, we have three possible ways of placing a converter. Hence, 16 configurations of PFC regulators are possible. For simplicity, we denote them as Configuration I-I, Configuration I-IIA, Configuration I-IIB, Configuration I-IIC, Configuration I-IIIA, Configuration I-IIIB, Configuration I-IIIC, etc., as shown in Fig. 5.

In the next section we will illustrate how these minimal configurations can be transformed into practical circuits by placing a simple switching converter in each converter block and appropriately connecting the input and output of the constituent converters to the input, storage, and load ports of the PFC regulator.

TABLE I
PREVIOUSLY REPORTED PFC REGULATOR CIRCUITS

PFC regulator circuit	Configuration
Ćuk, SSIPP [3], BIBRED [1]	I-I
Zeta	I-IIA
Chow-Tse-Lee [13]	I-IIA
SEPIC, BIFRED [1]	I-IIIB
PPFC [2]	I-IIIB
García *et al.* [7]	I-IIIB

IV. Examples of Derivation of Practical PFC Regulator Circuits

Based on the aforementioned configurations, we can construct actual circuits using two simple converters. For the cascade configuration, i.e., Configuration I-I, many topologies have been proposed previously [1]–[3]. The well-known BIFRED circuit is an example of Configuration I-IIIB. In García *et al.*[7], a practical circuit was proposed again for Configuration I-IIIB, but with two duty-cycle control for achieving PFC and output regulation. In Jiang *et al.* [2], yet another circuit of Configuration I-IIIB was proposed. The other configurations are rarely reported. Table I lists some previously reported circuits and their respective configurations.

In the following we will exemplify the creation of some rarely known circuit topologies for PFC voltage regulators based on

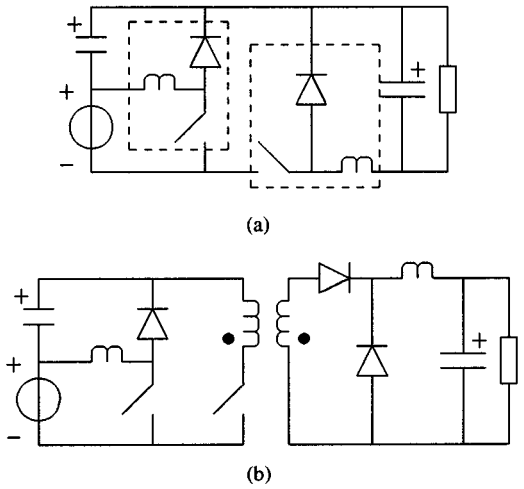

Fig. 6. A practical circuit for (a) I-IIA by direct substitution. (b) I-IIA isolated version. Core reset arrangement omitted for brevity.

some of the configurations given in Fig. 5. Our general procedure consists of selecting the types of basic converters for Converter 1 and Converter 2, and connecting them in accordance with the required power flow configuration.

Example 1: Realization of Configuration I-IIA: To illustrate the synthesis of practical circuits, we consider Configuration I-IIA. Suppose we choose a buck-boost converter and a buck converter as the constituent converters. Placing the two converters appropriately in Fig. 5(b), we obtain the circuit shown in Fig. 6(a). A transformer isolated version is shown in Fig. 6(b). This circuit has been tested experimentally [13].

Example 2: Realization of Configuration I-IIB: Consider Configuration I-IIB. Suppose we choose a buck-boost converter and a buck converter as the constituent converters. Similarly to Example 1, we obtain a new PFC regulator, as shown in Fig. 7(a), a transformer isolated version of which is shown in Fig. 7(b).

Example 3: Realization of Configuration I-IIIA: Consider Configuration I-IIB. Suppose we choose a buck converter and a buck-boost converter as the constituent converters. Similarly to Examples 1 and 2, we obtain a new PFC regulator, as shown in Fig. 8(a). A transformer isolated version is shown in Fig. 8(b).

Example 4: Realization of Configuration I-IIIB: Consider Configuration I-IIIB. Suppose we choose two buck-boost converters as the constituent converters. As in the previous examples, we obtain a PFC regulator, as shown in Fig. 9(a), a transformer isolated version of which is shown in Fig. 9(b).

Example 5: Realization of Configuration IIA-IIIA: Suppose we choose two buck-boost converters as the constituent converters for Configuration IIA-IIIA. As in the previous examples, we obtain a PFC regulator, as shown in Fig. 10. Note that one buck-boost converter takes energy from the sum of the input voltage and storage capacitor voltage and the other buck-boost converter takes energy from the difference of the input voltage and storage capacitor voltage. Each converter is under the control of one pair of switches, and the two pairs of switches need to operate under two sets of nonoverlapping duty-cycle signals. Effectively the storage capacitor is time multiplexed to give and take energy alternately.

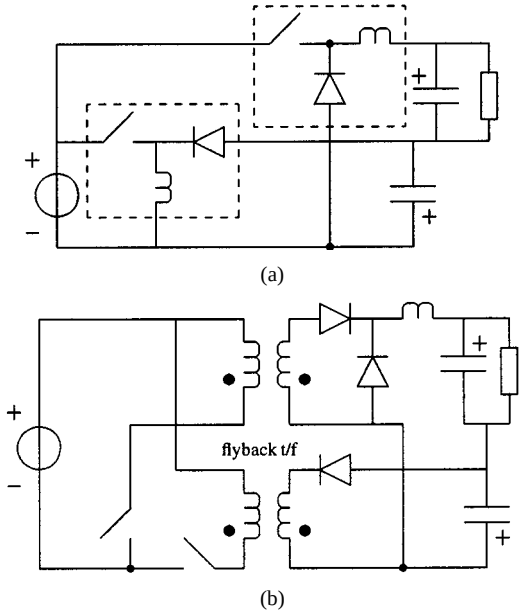

Fig. 7. A practical circuit for Configuration I-IIB. (a) Direct substitution. (b) Isolated version. Core reset of the upper transformer omitted for brevity.

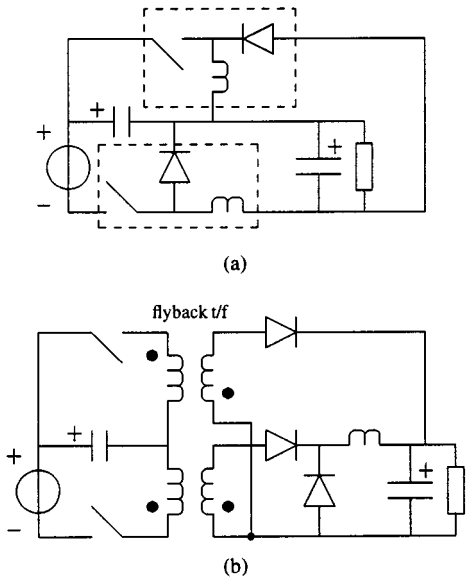

Fig. 8. A practical circuit for (a) I-IIIA by direct substitution. (b) I-IIIA isolated version.

Example 6: Realization of Configuration IIA-IIIB: As a last example, consider Configuration IIA-IIIB, with two buck-boost converters serving as the constituent converters. As shown in Fig. 11, we obtain yet another PFC regulator.

V. Comparison of Efficiency

Intuitively, the cascade configuration, i.e., Configuration I-I, has a poor efficiency since the input power is processed by the two converters serially before reaching the load. If η_1 and η_2 are the efficiencies of the two converters, the overall efficiency of Configuration I-I is given by

$$\eta_{\text{I-I}} = \eta_1 \eta_2. \tag{11}$$

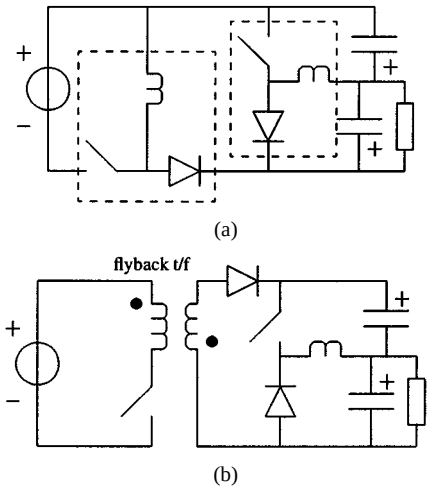

Fig. 9. A practical circuit for Configuration I-IIIB. (a) Direct substitution. (b) Isolated version (independently reported by García *et al.* [7]).

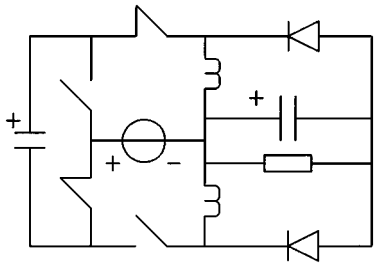

Fig. 10. A practical circuit for Configuration IIA-IIIA.

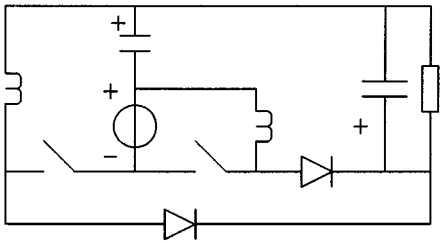

Fig. 11. A practical circuit for Configuration IIA-IIIB.

For Configuration I-IIA, the efficiency is expected to be higher than $\eta_1\eta_2$ since part of the input power goes through only one converter stage. Suppose the input power is split in a ratio of k to $1-k$ into Converters 1 and 2, as shown in Fig. 5(b). The efficiency in this case is

$$\begin{aligned}\eta_{\text{I-IIA}} &= k\eta_1\eta_2 + (1-k)\eta_2 \\ &= \eta_1\eta_2 + (1-k)\eta_2(1-\eta_1) \\ &> \eta_1\eta_2, \qquad \text{for all } 0<k<1. \end{aligned} \tag{12}$$

For Configuration I-IIB, we assume that the input power is split, in a ratio of k to $1-k$, into Converters 1 and 2, as shown in Fig. 5(c). The efficiency is given by

$$\begin{aligned}\eta_{\text{I-IIB}} &= k\eta_1 + (1-k)\eta_2 \\ &> \min\{\eta_1,\eta_2\}, \qquad \text{for all } 0<k<1 \\ &> \eta_1\eta_2. \end{aligned} \tag{13}$$

For Configuration I-IIC we assume that the input power is split in a ratio of k to $1-k$ into Converter 1 and the load, as shown in Fig. 5(d). The efficiency is given by

$$\begin{aligned}\eta_{\text{I-IIC}} &= k\eta_1\eta_2 + (1-k) \\ &= \eta_1\eta_2 + (1-k)(1-\eta_1\eta_2) \\ &> \eta_1\eta_2, \qquad \text{for all } 0<k<1. \end{aligned} \tag{14}$$

For Configuration IIA-IIIB, we assume that a fraction of $1-k$ of the input power is fed to Converter 2. The rest of the input power combines with the power released from the storage to supply Converter 1, as shown in Fig. 5(i). The output of Converter 2 is split in a ratio of m to $1-m$ into the load and the storage. Hence, we can write the efficiency as

$$\begin{aligned}&\eta_{\text{IIA-IIIB}} \\ &= (1-k)m\eta_2 + [(1-k)(1-m)\eta_2 + k]\eta_1 \\ &= \eta_1\eta_2\left[1 + \frac{(1-k)m}{\eta_1} + \frac{k}{\eta_2} - (m+k) + km\right] \\ &= \eta_1\eta_2\left[1 + m(1-k)\left(\frac{1}{\eta_1}-1\right) + k\left(\frac{1}{\eta_2}-1\right)\right] \\ &> \eta_1\eta_2, \qquad \text{for all } 0<k<1 \quad \text{and} \quad 0<m<1. \end{aligned} \tag{15}$$

Likewise, the efficiencies of the other configurations can be found, as tabulated in Table II. It is readily shown that Configurations I-IIA through IIC-IIIC all have a higher efficiency than Configuration I-I. In other words, the lower bound of the efficiency of a PFC regulator η is theoretically equal to $\eta_{\text{I-I}}$, i.e.,

$$\eta \le \eta_1\eta_2. \tag{16}$$

It should be noted that the above conclusion remains theoretical and the efficiency of real converters can be affected by a number of such other factors as transformer design, use of soft switching, choice of components, etc. Nonetheless, the above theoretical efficiency calculation does highlight a possible way to the design of inherently efficient PFC regulators, which is to minimize redundant power processing of the two constituent converters.

Remarks: The choice of m and k is affected by the efficiency as well as control requirements. In practice, efficiency and control specification represent conflicting requirements. For instance, if k is set at the extreme value of one for a I-IIB configuration, the efficiency is high, but no power factor correction can be achieved. Also, m and k are related to the voltage ratios of the constituent converters. Thus, depending upon the particular converter topologies used, there are limits to which m and k can be assigned to satisfy the specified control requirements (i.e., power factor and regulation). Selecting m and k is an important practical problem that deserves further investigation.

VI. Comparison of Control Requirements

The basic requirement of the control of a PFC regulator is to regulate the power flow among the input, load, and storage ports. In order to take full control of the amount of power being injected to and released from the storage, that being injected to the load, and that being taken from the input, the two constituent

TABLE II
THEORETICAL EFFICIENCIES (WHERE $0 < k < 1$ AND $0 < m < 1$). EXPRESSIONS ARRANGED FOR EASY COMPARISON WITH $\eta_1\eta_2$

Config.	Efficiency	
I-I	$\eta_1\eta_2$	
I-IIA	$\eta_1\eta_2 + (1-k)\eta_2(1-\eta_1)$	where $(1-k)\eta_2(1-\eta_1) > 0$
I-IIB	$k\eta_1 + (1-k)\eta_2$	where $k\eta_1 + (1-k)\eta_2 > \min\{\eta_1, \eta_2\} > \eta_1\eta_2$
I-IIC	$\eta_1\eta_2 + (1-k)(1-\eta_1\eta_2)$	where $(1-k)(1-\eta_1\eta_2) > 0$
I-IIIA	$k\eta_1 + (1-k)\eta_2$	same as I-IIB
I-IIIB	$\eta_1\eta_2 + (1-k)\eta_2(1-\eta_1)$	same as I-IIA
I-IIIC	$\eta_1\eta_2 + (1-k)(1-\eta_1\eta_2)$	same as I-IIC
IIA-IIIA	$k\eta_1 + (1-k)\eta_2$	same as I-IIB
IIA-IIIB	$\eta_1\eta_2 + m(1-k)\eta_2(1-\eta_1) + k\eta_1(1-\eta_2)$	where $m(1-k)\eta_2(1-\eta_1) + k\eta_1(1-\eta_2) > 0$
IIA-IIIC	$\eta_1\eta_2 + m(1-k)(1-\eta_1\eta_2) + k\eta_1(1-\eta_2)$	where $m(1-k)(1-\eta_1\eta_2) + k\eta_1(1-\eta_2) > 0$
IIB-IIIA	$\eta_1\eta_2 + \eta_1\eta_2\left[\frac{km}{\eta_1}\left(\frac{1}{\eta_2}-1\right) + \left(\frac{(1-k)\eta_1+k\eta_2}{\eta_1\eta_2}-1\right)\right]$	where $(1-k)\eta_1 + k\eta_2 > \eta_1\eta_2$ (see I-IIB)
IIB-IIIB	$k\eta_1 + (1-k)\eta_2$	same as I-IIB
IIB-IIIC	$\eta_1\eta_2 + \eta_1\eta_2\left[\frac{km}{\eta_1}\left(\frac{1}{\eta_2}-1\right) + \left(\frac{(1-k)\eta_1+k\eta_2}{\eta_1\eta_2}-1\right)\right]$	where $(1-k)\eta_1 + k\eta_2 > \eta_1\eta_2$ (see I-IIB)
IIC-IIIA	$\eta_1\eta_2 + \eta_1\eta_2\left[\frac{(1-k)\eta' + k\eta_1\eta_2}{(\eta_1\eta_2)\eta'} - 1\right]$	where $\eta' = \frac{\eta_1\eta_2}{(1-m)\eta_1 + m\eta_2}$ and $(1-k)\eta' + k\eta_1\eta_2 > \eta_1\eta_2\eta'$
IIC-IIIB	$\eta_1\eta_2 + \eta_1\eta_2\left[k + \left(\frac{(1-k)\eta_2 + k\eta''}{\eta_2\eta''} - 1\right)\right]$	where $\eta'' = \eta_1\eta_2$ and $(1-k)\eta_2 + k\eta'' > \eta_2\eta''$
IIC-IIIC	$\eta_1\eta_2 + (1-km)(1-\eta_1\eta_2)$	where $(1-km)(1-\eta_1\eta_2) > 0$

converters should be controlled separately. The following theorem is instrumental.

Theorem 2: For any PFC regulator consisting of two simple converters, it is not possible to achieve unity power factor and output regulation simultaneously under the control of only one control parameter.

Proof: We will prove this theorem by contradiction. First we assume that unity power factor (p.f.) and output regulation are achieved with only one control parameter $\xi(t)$ controlling both converters. It is worth recalling that we are considering only low-frequency power flows. Suppose the power processed by Converter 1 and Converter 2 are $F_1(\xi(t))$ and $F_2(\xi(t))$, respectively. Thus, we hope to find $\xi(t)$ such that the PFC and output regulation are satisfied simultaneously. We will exemplify the proof with Configuration I-I. Assuming that the converters are lossless, the PFC requirement dictates that for all t

$$\begin{aligned} & F_1(\xi(t)) = 2P_o \sin^2 2\pi f_m t \\ \Rightarrow \quad & \xi(t) = F_1^{-1}(2P_o \sin^2 2\pi f_m t) \end{aligned} \tag{17}$$

where P_o is the output power. However, output regulation requires that for all t

$$\begin{aligned} & F_2(\xi(t)) = P_o \\ \Rightarrow \quad & \xi(t) = F_2^{-1}(P_o) \end{aligned} \tag{18}$$

which contradicts (17). Likewise, for all other configurations, we will arrive at an obvious contradiction if we begin with the assumption of using only one parameter for control. Thus, in general we are not able to maintain PFC and output regulation using only one control parameter, $q.e.d.$

It should be apparent that if two separate control parameters are allowed, then the control problem can be solved. (A straightforward proof can be constructed based on Theorem 2's proof.) Two forms of the solution can be logically deduced.

1) The power flow functions F_1 and F_2 are controlled separately by $\xi_1(t)$ and $\xi_2(t)$, where $\xi_1(t) \neq \xi_2(t)$.
2) One of the power flow functions is controlled by two control parameters $\xi(t)$ and $\psi(t)$, while the other one is controlled by either $\xi(t)$ or $\psi(t)$.

As we will see later, the above first solution covers the conventional design of cascading a PFC preregulator and a dc/dc converter, which are under separate control. The second solution, moreover, covers the single-stage design utilizing both duty cycle modulation and frequency modulation for achieving almost perfect PFC and fast regulation [9].

Remarks: In formulating practical solutions, the choice of the types of converters is crucial since the power flow functions F_1 and F_2 depend on circuit topologies. In the following discussion we assume that the converters have been properly chosen to ensure satisfaction of the required power flow functions.

VII. APPLICATION TO THE CONTROL OF PRACTICAL CONVERTERS

We may now take a further step in applying the above result to real converters. The usual parameters available for control are the duty cycle d and the switching frequency f_s. For converters operating in discontinuous mode, both d and f_s are available control parameters. However, for converters operating in continuous mode, only d is available since such converters are highly immune to variation of the switching frequency. For brevity, we write the power flow function for a continuous-mode (CM) converter as $F_{\rm CM}(d(t))$ and that of a discontinuous-mode (DM) converter as $F_{\rm DM}(d(t), f_s(t))$, respectively.

A. Choice of Control Parameters

As studied in Section VI, we generally need two separate control loops for controlling two parameters. Moreover, operating modes of the converters will affect the complexity of the control problem. It is not difficult to see the following results which are straightforward extensions of the above discussion.

Operating Regime 1: When both converters are in CM operation, the use of two separate duty cycle signals for the two converters is mandatory. The power flow functions are

$$P_1 = F_{\mathrm{CM}_1}(d_1(t)) \tag{19}$$
$$P_2 = F_{\mathrm{CM}_2}(d_2(t)) \tag{20}$$

where P_1 and P_2 denote the power flows through the two converters, $F_{\mathrm{CM}_1}(\cdot)$ and $F_{\mathrm{CM}_2}(\cdot)$ are the respective power flow functions and $d_1(t)$ and $d_2(t)$ are the duty cycle signals controlling separately the two converters.

Operating Regime 2: When one converter is in CM operation and the other in DM operation, we may employ any combination of two control parameters chosen from two available duty cycles and a switching frequency, i.e.,

$$P_1 = F_{\mathrm{CM}_1}(d_1(t)) \tag{21}$$
$$P_2 = F_{\mathrm{DM}_2}(d_2(t), f_{s_2}(t)). \tag{22}$$

Operating Regime 3: When both converters are in DM operation, we may employ any combination of two control parameters chosen from two available duty cycles and two available switching frequencies, i.e.,

$$P_1 = F_{\mathrm{DM}_1}(d_1(t), f_{s_1}(t)) \tag{23}$$
$$P_2 = F_{\mathrm{DM}_2}(d_2(t), f_{s_2}(t)). \tag{24}$$

It is worth noting that the above control cases are applicable to all 16 configurations. In particular, they cover all conventional two-stage designs in which a PFC preregulator and a dc/dc converter are cascaded together under the control of two separate loops.

B. Application to Single-Stage Design

Due to its popularity, the single-stage PFC regulator may deserve further discussion [3]–[6]. Specifically, since only one (set of) active switch(es) exists, it is not possible to use two duty cycle signals as the control parameters. Thus, we must base our design on the combined use of duty cycle and frequency control. This also necessitates the operation of at least one of the converters in DM. Two possibilities exist, corresponding to Operating Regimes 2 and 3. Since only one duty cycle and one switching frequency are available, they become the inevitable choice of control parameters. Specifically, for Operating Regime 2, we have

$$P_1 = F_{\mathrm{CM}_1}(d(t)) \tag{25}$$
$$P_2 = F_{\mathrm{DM}_2}(d(t), f_s(t)) \tag{26}$$

and for Operating Regime 3, we have

$$P_1 = F_{\mathrm{DM}_1}(d(t), f_s(t)) \tag{27}$$
$$P_2 = F_{\mathrm{DM}_2}(d(t), f_s(t)). \tag{28}$$

Obviously, in practice, Operating Regime 2 has the advantage over Operating Regime 3 because if one converter is not affected by frequency variation, then frequency modulation can be used solely for controlling the other converter [9]. In short, we may state the results of our analysis of the control requirement of single-stage PFC regulators as follows.

1) Perfect PFC and output regulation are not simultaneously achieveable if both constituent converters are operating in continuous mode.
2) Perfect PFC and output regulation are simultaneously achieveable only if at least one of the constituent converters is operating in discontinuous mode. (We use only if here because we still require the converter topologies be properly chosen.)
3) Combined use of duty cycle and switching frequency control is inevitable in achieving perfect PFC and output regulation.

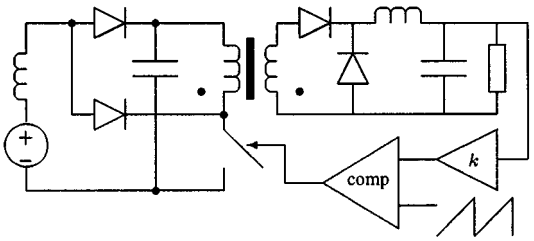

Fig. 12. Single-stage single-switch PFC regulator based on Configuration I-I (Redl *et al.* [3]).

Notwithstanding the above, control can be simplified in some configurations if performance can be compromised. In fact, imperfect PFC can still be acceptable from a practical point of view since most regulatory standards, e.g., IEC-1000, do not demand a perfect unity power factor. For example, Configuration I-I (cascaded converters) can allow the use of one duty cycle signal for achieving reasonably high power factor and fast output transient, thus making the design very easy [3]. Such control simplicity represents an attraction of Configuration I-I, as will be illustrated in the following example.

C. Illustrative Example: Single-Stage Single-Switch PFC Regulator

A single-stage PFC regulator employing one switch and comprising a cascade connection of a boost converter and a forward converter has been proposed for some time by Redl *et al.* [3]. This converter, as shown in Fig. 12, belongs to Configuration I-I. The original design employs Operating Regime 3 (i.e., with both the boost and the forward stages operating in discontinuous mode), but uses only duty cycle control for output regulation. It has been shown experimentally [3] that a reasonable power factor and fast output response can in fact be obtained without the use of two separate controls. Clearly, from the foregoing discussion, we can improve the performance of this PFC regulator if we have an extra control parameter.

Specifically, to achieve perfect PFC and output regulation, we need two control parameters. Owing to the single-switch design, the combined use of duty cycle and switching frequency control is inevitable, as discussed previously. In Chow *et al.* [9], the same converter is redesigned to employ Operating Regime 2 so as to immunize one converter against frequency variation. Hence, control can be easily achieved with one loop regulating the output via duty cycle modulation and another loop shaping the input current via frequency modulation. Specifically, the

boost converter is made to operate in DM, whereas the forward converter is in CM. The control equation for the DM boost converter, as derived in Chow *et al.* [9] is

$$f_s = \frac{f_o}{1 - \frac{v_i(t)}{V_c}} \tag{29}$$

where $v_i(t)$ is the input voltage, V_c is the voltage across the storage capacitor, and f_o is the minimum switching frequency. The forward converter is simply controlled by a conventional PWM scheme. Details of practical implementation and experimental results can be found in [9].

Remarks: It should be noted that the choice between Operating Regimes 2 and 3 is also affected by the problem of variable voltage stress. The foregoing discussion only focuses on the control issue. Readers may refer to Redl and Balogh [4] and Tse [11] for an analysis of the voltage stress problem associated with the two operating regimes.

VIII. Conclusion

Although a number of PFC regulator topologies have been reported recently, they represent isolated cases of innovative circuit design and very little formal work has been performed on the basic procedure for deriving the required circuit configurations that can shed light on the creation of new circuit topologies for such applications. This paper derives the basic configurations of converters for achieving PFC and voltage regulation. The starting point of our investigation is the fundamental requirement of the presence of a low-frequency storage which leads to a simple three-port model of the PFC regulator. The main result of this investigation is the derivation of sixteen minimal circuit configurations, based on which PFC regulators can be constructed systematically. In practice, each configuration can be implemented using two basic converter stages. The study provides insight into the systematic synthesis of converter circuits that can provide high power factor and output voltage regulation. Furthermore, the control aspect of the PFC regulator is studied in some depth, providing a theoretical basis for further investigation of control methods relevant to this specific type of applications. The results reported in this paper also clear up some previous misconceptions which accounted for the failure in attempting to use, for example, a BIFRED circuit or a Ćuk converter operating in continuous mode as a PFC regulator, despite the use of any sophisticated duty cycle and/or frequency control.

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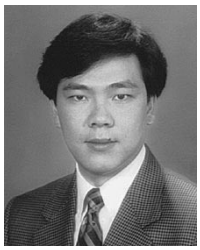

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