Circuit Theoretic Classification of Parallel Connected DC–DC Converters

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Abstract—This paper describes a classification of paralleling schemes for dc–dc converters from a circuit theoretic viewpoint. The purpose is to provide a systematic classification of the types of parallel converters that can clearly identify all possible structures and control configurations, allowing simple and direct comparison of the characteristics and limitations of different paralleling schemes. In the proposed classification, converters are modeled as current sources or voltage sources, and their connection possibilities, as constrained by Kirchhoff’s laws, are categorized systematically into three basic types. Moreover, control arrangements are classified according to the presence of current sharing and voltage-regulation loops. Computer simulations are presented to illustrate the characteristics of the various paralleling schemes.

Index Terms—Control methods, current-sharing schemes, dc–dc converters, parallel connected converters, topology.

I. INTRODUCTION

POWER supplies based on paralleling a number of switching converters offer several advantages over a single high-power centralized power supply, such as low component stresses, increased reliability, ease of maintenance and repair, improved thermal management, etc. [1]–[4]. Paralleling of standardized converters will continue to be a popular approach adopted in distributed power systems for both front-end and load converters.

One basic objective of parallel connected converters is to share the load current among the constituent converters. To do this, some form of control has to be used to equalize the currents in the individual converters. A variety of approaches, with varying complexity and current-sharing performance, have been proposed in the past two decades [5]–[9]. In general, methods for paralleling dc–dc converters are described in terms of connection styles, control configurations and feedback functions. Although some forms of classifications and comparisons have been given for paralleling schemes [10]–[12], most fall short of a systematic identification of all possible structures and control configurations. For instance, in Luo et al. [10], a classification has been given based on the existing paralleling methods. Basically, Luo et al. categorized the methods into two categories according to the type of current-sharing method, namely, passive droop methods and active current-sharing methods. They reported five specific schemes that exploit the droop characteristics of the converters, and two specific schemes that use active-current sharing methods, i.e., the master–slave scheme and the average scheme. In addition, three control structures, namely, inner loop regulation, outer loop regulation and external control, were identified. Their classification is thus basically a systematic collection of existing schemes. Other classification works, such as Liu et al. [11] and Choi [12], focus on the control loop configurations of selected active current-sharing paralleling schemes.

In order to facilitate design and choice of appropriate paralleling configurations, a systematic classification of the paralleling schemes that permits a clear exposure of the structures, behaviors and limitations of all possible schemes, is needed. In this paper, we investigate the classification problem and utilize basic circuit theory to identify the basic structures and control methods of paralleled dc–dc converters. Our objective is to provide a simple classification that eliminates redundancy, includes all possible basic structures, permits comparative analysis of different structures, and hence allows systematic derivation of paralleling schemes.

Our starting point will be the two Kirchhoff’s laws that dictate the possible connection styles. Considering converters as either voltage sources or current sources, we define three basic structures for paralleling converters. As we will see, these structures actually form the basis of all practical paralleling schemes. We will develop equivalent models which can be used in analysis. Furthermore, control methods will be systematically introduced to complete the output regulation and current-sharing functions. Finally, computer simulations will be presented to provide a full comparison of the various configurations.

II. BASIC CIRCUIT THEORY OF PARALLELING CONNECTIONS

A. Basic Constraints in Paralleling Independent Sources

The output of any converter is normally expected to provide regulated voltage or current. Thus, an appropriate model for a converter (seen at output terminals) is either a voltage source or a current source. Two basic laws must be obeyed when connecting sources together. First, Kirchhoff’s voltage law (KVL) dictates that the sum of voltages of all branches (in the same sense) forming a loop must equal zero. This means that no two independent voltage sources are permitted to be connected in parallel. Theoretically, even if the voltage sources are of the same magnitude, paralleling them is still not permitted as it makes the current values undefined [13]. Likewise, Kirchhoff’s current law (KCL) dictates that the sum of currents of all branches in a cutset (emerging from the same sub-graph) must equal zero. This clearly eliminates the possibility of connecting two independent current sources in series. In this paper, as our focus is paralleling sources, we do not consider the case of connecting sources in series.
and the branch. For a current source branch, we have

\[ Z = \begin{cases} \frac{Z_o}{1 + T}, & \text{for Thévenin form} \\ Z_o(1 + T), & \text{for Norton form} \end{cases} \]  

(1)

where \( Z_o \) is the open-loop output impedance. If the loop gain \( T \) is high enough, \( Z \) becomes negligibly small for the voltage source representation or very large for current source representation. The output characteristic of the converter resembles that of a nearly independent source.

III. GENERAL CLASSIFICATION OF PARALLEL CONNECTED DC–DC CONVERTERS

From the foregoing discussion, it is clear that any paralleling scheme involving voltage and current sources must comply with the two basic structures described earlier. Moreover, if the voltage sources are imperfect (i.e., with a nonzero output impedance), they can still be connected in parallel. Thus, we have three basic configurations for paralleling imperfect sources.

When dc–dc converters are treated as imperfect voltage or current sources, three basic configurations for paralleling practical dc–dc converters can be developed, as summarized in Fig. 3. For brevity, we refer to these configurations as Types I, II, and III connections. For a voltage source branch, we have

\[ V_o = V_i - I_{o,i}Z_i \quad \text{or} \quad I_{o,i} = \frac{V_i - V_o}{Z_i} \]  

(2)

where subscript \( i \) (1 to \( n_t \)) indicates the branch number, and \( I_{o,i} \) is the output current of the \( i \)th branch, i.e., the part of load current shared by the \( i \)th branch. For a current source branch, we have

\[ V_o = (I_i - I_{o,i})Z_i \quad \text{or} \quad I_{o,i} = I_i - \frac{V_o}{Z_i} \]  

(3)

where \( I_i \) is the equivalent current source of the \( i \)th branch.

In practice, we need to apply appropriate control to dc–dc converters in order to “cast” them as voltage or current sources. For instance, a voltage feedback loop is obviously needed for controlling a dc–dc converter so that it behaves as a voltage source. Thus, the paralleling configurations are closely related to the control method which effectively determines whether a dc–dc converter would behave as a voltage or current source.

In addition to the defining control of current and voltage sources, a current sharing control can be used to ensure even sharing of the load current among the converters. In a parallel converter system, each constituent converter is a power supply. To avoid confusion, we will use the term current-sharing loop in a specific context. If a current-sharing reference is derived from the output currents of one/all constituent converters, the control scheme is said to contain a current-sharing loop.

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1By “small” impedance and “large” impedance, we actually refer to the modulus of the impedance.

2By imperfect sources, we mean those voltage sources having nonzero output impedance and those current sources having finite output impedance.
Fig. 3. Three configurations for paralleling converters. (a) Type I. (b) Type II, with practical form on the right. (c) Type III, with practical form on the right.

Fig. 4. Systematic classification of parallel connected converters.

Otherwise, the control scheme does not have a current-sharing loop.

We may therefore further classify parallel converter systems according to the presence of a current-sharing loop, resulting in a simple, systematic classification, as shown in Fig. 4. Two layers are included in the classification. In the first layer, we get three configurations, Types I, II, and III, based on the circuit theoretic connection styles. In the second layer, the presence of a current-sharing loop is the classifying criterion.

IV. THREE TYPES OF CONNECTION STYLES AND ASSOCIATED CONTROL METHODS

In this section, in light of the classification framework mentioned in the foregoing, the various types of parallel connected dc–dc converters are described in detail. Our emphases here are the generic circuit theoretic structures and the necessary control methods. As a prerequisite, we note that converters aiming to imitate voltage sources should have tight voltage feedback loops for voltage regulation purposes, whereas converters imitating current sources would necessitate some form of current-mode control in order to set the current magnitudes. The presence of a current-sharing loop is an additional feature, contributing to the current sharing of the constituent converters.

A. Type I

The Type-I connection is shown in Fig. 3(a). Each branch represents a converter, which is basically a Thévenin source, i.e., a dependent voltage source behind an output impedance. For the control without current-sharing loop, the branches are simply connected in parallel. However, the absence of a current-sharing loop imposes some specific requirements on the individual branches in order to provide natural current sharing [15], [16]. This has been commonly known as the droop method [7], [17]. Specifically, each converter (branch), in the absence of a current-sharing loop, should have a finite output resistance at steady state.

As an example, Fig. 5 shows the output characteristics of two converters connected in parallel, without employing a current-sharing loop. Suppose the output current, equivalent Thévenin voltage and output resistance of converter \(i\) (branch \(i\)) is \(I_i, V_i, R_i\).
For the Type-I connection shown in Fig. 3(b), one converter behaves as a good current source. Current-programming methods, such as master–slave current-sharing method [19]–[21], where the voltage source is the master and the current sources are the slaves whose currents are programmed to follow the master’s.

C. Type III

In the Type-III configuration shown in Fig. 3(c), all converters are current (Norton) sources. In the absence of a current-sharing loop, all converters have to follow a common current control signal $i_{\text{con}}$ which is derived from the output voltage feedback loop, as shown in Fig. 8(a). The voltage feedback loop aims to achieve voltage regulation as well as current sharing. In the ideal case, the load current is distributed equally, i.e., $I_1 = I_2 = \cdots = I_n$. A simple implementation can be found in Lu et al. [22].

Finally, for the Type-III configuration with current-sharing loop, all converters are under current-mode control so that they behave as good current sources. Current-programming methods, such as master–slave method or average method, can be used to generate the common current-sharing control signal [23], [24]. The amplified errors between the current-sharing control signal and the feedback currents $v_{\text{con}1}, v_{\text{con}2}, \ldots, v_{\text{con}n}$, are injected to the feedback loop, adjusting the current control signals $i_{\text{con}1}, i_{\text{con}2}, \ldots, i_{\text{con}n}$. The basic structure is shown in Fig. 8(b).
V. COMPARISON OF PARALLeLING SCHEMES

In the foregoing section, we have discussed the structures and the associated control methods for paralleling dc–dc converters. In this section, we compare the different structures and control methods in terms of current-sharing accuracy, voltage regulation, dynamical performance, etc. Intuitively, we can make the following general observations:

1) Type-I schemes are simple but suffer fundamentally from paralleling voltage sources. The adjustment range for current sharing is small since each constituent converter is designed primarily to regulate its local output voltage, and the currents in the converters can only be adjusted by controlling the voltages which are not allowed to vary too much.

2) Type-II schemes are theoretically more viable as there is only one voltage source, paralleling with current sources. The dynamics of the voltage regulation thus depends on the control method being employed by the voltage regulating loop. The other current source converters control their currents directly to achieve the desired current sharing. Thus, the current-sharing performance is generally much better compared to Type-I schemes.

3) Type-III schemes are more complicated in terms of implementation due to substantial current programming requirements. However, Type-III schemes are generally best in terms of current sharing as all converters are fundamentally current controlled. The voltage regulation can also enjoy fast response due to the direct load voltage control.

For a detailed comparison, we consider a system of three buck converters connected in parallel, as shown in Fig. 9(a).

Fig. 9. Paralleled converters and the compensator networks. (a) Three parallel-connected buck converters. (b) Two-zero two-pole compensator. (c) Proportional-integral compensator. (d) Single-pole compensator.

Fig. 9(b)–(d) shows the controllers used in the simulations for voltage regulation and current sharing. In our simulations, models are constructed using MATLAB/SIMULINK.

As it is important to ensure generality of any conclusion made in our study, we have consistently used the same type of compensation networks and equivalent values of control parameters in order to ensure that fair comparison can be made and generally valid conclusions are drawn. Here, we have chosen the most typical compensation networks for the different control situations. Specifically, for voltage-mode buck converters, we employ a typical two-zero two-pole compensator, as shown in Fig. 9(b). Denoting the Laplace transforms of the control signal and converter output signal as $V_{\text{con}}(s)$ and $V_o(s)$, respectively, the transfer function is

$$\frac{V_{\text{con}}(s)}{V_o(s)} = \frac{\omega_1(1+s/\omega_2)}{s(1+s/\omega_3)(1+s/\omega_2)}$$

where $\omega_1 = 1/(R_1(C_1 + C_2))$, $\omega_2 = 1/(R_2C_1)$, $\omega_3 = 1/(R_3 + R_4)$, $\omega_4 = 1/(R_0C_2)$, $\omega_5 = (C_1 + C_3)/(R_0C_2C_3)$. For the current-mode control, moreover, the outer voltage feedback loop employs a PI controller, as shown in Fig. 9(c). The transfer function is

$$\frac{V_{\text{con}}(s)}{V_o(s)} = -\frac{K(1+s/\omega_2)}{s}$$
Finally, for current-sharing loops, we employ a simple single-pole compensator, as shown in Fig. 9(d). Denoting the Laplace transforms of the control voltage and the inductor current as $V_{cs}(s)$ and $I_L(s)$, the transfer function is given by

$$V_{cs}(s) = \frac{K}{1 + s/\omega_{pcs}} \tag{7}$$

where $K = 1/(R_1 C_1)$, $\omega_{cs} = 1/(R_2 C_1)$. Finally, for current-sharing loops, we employ a simple single-pole compensator, as shown in Fig. 9(d). Denoting the Laplace transforms of the control voltage and the inductor current as $V_{cs}(s)$ and $I_L(s)$, the transfer function is given by

$$V_{cs}(s) = \frac{K_{cs}}{1 + s/\omega_{pcs}} \tag{7}$$

where $K_{cs} = R_1 R_2 / R_1$, $\omega_{pcs} = 1/(R_2 C_1)$. The current sharing control signal, $i_{con}$, is the average value of all inductance currents, i.e., $i_{con} = (1/3) \sum_{n=1}^{3} i_L$.

The component values used in the simulations are listed in Table I. For different types of paralleling schemes, appropriate controllers, as shown in Fig. 9(b)-(d), are selected and designed to ensure that the same voltage loop bandwidth is achieved, i.e., about 10 kHz. The parameters used in the controllers are shown in Table II.

For the Type-I configuration, each converter is under voltage-mode control. For the paralleling scheme without current-sharing loop (droop scheme), extra current feedback is used to produce a droop in the output voltage, where the equivalent droop resistance is proportional to the current feedback gain [10]. Figs. 10 and 11 show the output voltage and current waveforms under a stepped load condition. In Fig. 10, we also illustrate the effect of the output resistance, which is crucial to this kind of droop scheme. The output resistance used for simulations of Fig. 10(a) and (b) is ten times larger than that used for the simulations of Fig. 10(c) and (d). From the simulation results, we clearly see that the Type-I scheme without current-sharing loop does not perform very satisfactorily. Normally, with large output resistance, we may achieve good current sharing but poor output regulation. However, the current sharing becomes worse and output regulation becomes better with smaller output resistance. This remains the fundamental limitation of such droop schemes, as multiple nonidentical voltage sources are paralleled and there is only a very narrow adjustment range for controlling the currents via the voltage drops in the output resistances.

Another dynamical test is the plug-in transient. Initially, two converters share the load. Then, a third converter plugs in and shares the load with the other two operating converters. The results are shown in Fig. 11 for the Type-I paralleling scheme without current-sharing loop. The currents in the two operating converters drop to zero during the plug-in transient. Such blackout is undesirable as it imposes high current stress on the third converter during the transient.

<table>
<thead>
<tr>
<th>TABLE I</th>
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<tr>
<td><strong>POWER STAGE COMPONENT VALUES USED IN SIMULATIONS</strong></td>
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<tr>
<td><strong>Circuit Components</strong></td>
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<tr>
<td>Switching Period $T_s$</td>
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<tr>
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<tr>
<td>Output Voltage $V_o$</td>
</tr>
<tr>
<td>Inductance $L_1$, ESR $r_{L1}$</td>
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<tr>
<td>Inductance $L_2$, ESR $r_{L2}$</td>
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<td>Inductance $L_3$, ESR $r_{L3}$</td>
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<tr>
<td>Capacitance $C$, ESR $r_c$</td>
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<td>Load Resistance $R_L$</td>
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<th>TABLE II</th>
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<tr>
<td><strong>CONTROLLER PARAMETERS USED IN SIMULATIONS (UNIT FOR ALL $\omega$’S: RADS$^{-1}$, UNIT FOR $K$: RADS$^{-1}$, UNIT FOR $K_{con}$: $\Omega$)</strong></td>
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<table>
<thead>
<tr>
<th>Type I</th>
<th>Type II</th>
<th>Type III</th>
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<tr>
<td>without current-sharing loop</td>
<td>with current-sharing loop</td>
<td>without current-sharing loop</td>
</tr>
<tr>
<td>$\omega_1$</td>
<td>4.5 $\times$ 10$^2$</td>
<td>4.5 $\times$ 10$^2$</td>
</tr>
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<td>$\omega_{L1}$</td>
<td>2 $\times$ 10$^3$</td>
<td>2 $\times$ 10$^3$</td>
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<tr>
<td>$\omega_{L2}$</td>
<td>6 $\times$ 10$^3$</td>
<td>6 $\times$ 10$^3$</td>
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<tr>
<td>$\omega_{L3}$</td>
<td>2 $\times$ 10$^3$</td>
<td>2 $\times$ 10$^3$</td>
</tr>
<tr>
<td>$\omega_{L4}$</td>
<td>3 $\times$ 10$^3$</td>
<td>3 $\times$ 10$^3$</td>
</tr>
<tr>
<td>$K$</td>
<td>—</td>
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<tr>
<td>$\omega_{K1}$</td>
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<tr>
<td>$\omega_{K2}$</td>
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<tr>
<td>$K_{con}$</td>
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<td>0.7</td>
</tr>
<tr>
<td>$\omega_{pcs}$</td>
<td>—</td>
<td>1 $\times$ 10$^5$</td>
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Fig. 10. Simulation results for stepped load for Type-I scheme without current-sharing loop. (a) Output voltage with large output resistance. (b) Converter output current with large output resistance. (c) Output voltage with small output resistance. (d) Converter output current with small output resistance.

Fig. 11. Simulation results for plug-in transient for Type-I scheme without current-sharing loop. (a) Output voltage. (b) Converter output currents.
With current-sharing loop, the Type-I scheme performs better, as demonstrated in Fig. 12(a) and (b) and Fig. 13. Moreover, as would be expected, increasing the current-sharing gain and/or the voltage feedback gain would affect the stability of the system. As shown in Fig. 12(c) and (d), the system becomes unstable when the current-sharing gain increases. Likewise, the system becomes unstable when the voltage feedback gain is large, as shown in Fig. 12(e) and (f). This is because the current-sharing error signal outside of the voltage loop is amplified and fed back to the voltage loop causing possible unstable behavior if the current-sharing gain or the voltage feedback gain is too large. To get stable operation, we have to limit these gains, which also limit the dynamic response. The plug-in transient is shown in Fig. 13. The system rebalances itself without drastic blackout of individual converter currents. This is an improvement over the Type-I scheme without current-sharing loop.

Shown in Figs. 14 and 15 are simulation results for the Type-II scheme without current-sharing loop. As shown in Fig. 14, satisfactory dynamic response under stepped load change is demonstrated. However, the current-sharing accuracy relies on the precision of the current divider. Small variation of the current divider can give large current-sharing errors between the voltage converter and current converters. In this case, we observe current-sharing errors from 6.25% to 13.25% ($i_{L1} = 3.47 \text{ A}$, $i_{L2} = 4.28 \text{ A}$, $i_{L3} = 4.25 \text{ A}$). Also, the plug-in transient is shown in Fig. 15. The system is able to rebalance itself without causing current blackout, though fairly slowly with settling time of around 2 ms in this case.

In Figs. 16 and 17, we show the simulation results for the Type-II scheme with current-sharing loop. As seen from Fig. 16, satisfactory dynamic response under stepped load change is demonstrated. Also, the current-sharing accuracy is improved compared to the Type-II scheme without current-sharing loop, with current-sharing errors from 1.25% to 5% ($i_{L1} = 4.05 \text{ A}$, $i_{L2} = 4.15 \text{ A}$, $i_{L3} = 3.8 \text{ A}$) in this case. This is because the slaves set their currents to equal that of the master via...
comparison their currents with the master’s. Here, we clearly confirm our earlier theoretical analysis that only one voltage loop is enough to regulate the output voltage. However, the master should be as fast as possible to provide stable reference for the slaves. Moreover, Fig. 17 shows satisfactory re-balancing after a plug-in transient, with a settling time of around 1.2 ms.

Results for the Type-III scheme without current-sharing loop are shown in Figs. 18 and 19. Here, we observe satisfactory dynamic response for large load change. However, the current-sharing errors are quite large (1.25% to 8.75% in this case, \(i_{L1} = 4.3\, \text{A}, i_{L2} = 4.05\, \text{A}, i_{L3} = 3.65\, \text{A}\)) because it is sensitive to the current comparator due to the absence of current sharing comparison. Moreover, as shown in the plug-in transient of Fig. 19, the re-balancing can be achieved very quickly with a settling time of less than 1 ms.

Finally, for the Type-III scheme with current-sharing loop, the simulation results are shown in Figs. 20 and 21. In this case we observe very fast dynamic response, and very precise current sharing, with current-sharing errors from 0% to 3.75% in this case (\(i_{L1} = 4.15\, \text{A}, i_{L2} = 4\, \text{A}, i_{L3} = 3.85\, \text{A}\)). Further improvement of current sharing can be obtained by adjusting the current-sharing compensator. Also, very fast re-balancing after a plug-in transient can be observed, as shown in Fig. 21.

From the foregoing simulation results, we may summarize the general features of the three configurations and their control methods. In short, Type-I schemes, though simple, suffer from some fundamental limitations as voltage sources are being paralleled. Type-II schemes have one voltage source paralleling a number of current sources. The voltage regulation performance thus depends on the feedback arrangement of the voltage source. Current sharing is much easier to obtain than that of Type-I schemes. Type-III schemes are basically parallel current sources. They achieve very fast response and generally good current sharing as voltage regulation is based on the load.
voltage feedback and current sharing is done via direct current control. Table III compares their relative pros and cons in terms of ease of expansion, dynamic performance, current-sharing accuracy and regulation capability.

VI. CONCLUSION

In this paper, a systematic classification of parallel connected switching power converters is given. Our starting point is circuit theory of connecting voltage and current sources as converters can be regarded as voltage or current sources. Three basic types of paralleling schemes can be identified, corresponding to: i) connecting Thévenin sources in parallel; ii) connecting one Thévenin source with many Norton sources in parallel and iii) connecting Norton sources in parallel. The presence of current-sharing loop has been considered as an optional feature, though its use has been clearly proven to be important for achieving good performance in current balancing. The classification presented in this paper allows the structures and control requirements of paralleling schemes to be systematically analyzed.

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Dr. Tse was awarded the L.R. East Prize by the Institution of Engineers, Australia, in 1987. He won the IEEE TRANSACTIONS ON POWER ELECTRONICS Prize Paper Award for 2001 and the International Journal of Circuit Theory and Applications Best Paper Award for 2003. In 2005, he was named an IEEE Distinguished Lecturer. While with Hong Kong Polytechnic University, he received twice the President’s Award for Achievement in Research, the Faculty’s Best Researcher Award, the Research Grant Achievement Award and a few other teaching awards. From 1999 to 2001, he served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: FUNDAMENTAL THEORY AND APPLICATIONS, and since 1999 he has been an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS. He currently also serves as an Associate Editor of the International Journal of Systems Science, a Guest Associate Editor of the IEICE Transactions on Fundamentals of Electronics, Communications and Computers, and a Guest Editor of Circuits, Systems and Signal Processing.