Circuit Theoretic Classification of Parallel Connected DC–DC Converters

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***Abstract*—This paper describes a classification of paralleling schemes for dc–dc converters from a circuit theoretic viewpoint. The purpose is to provide a systematic classification of the types of parallel converters that can clearly identify all possible structures and control configurations, allowing simple and direct comparison of the characteristics and limitations of different paralleling schemes. In the proposed classification, converters are modeled as current sources or voltage sources, and their connection possibilities, as constrained by Kirchhoff's laws, are categorized systematically into three basic types. Moreover, control arrangements are classified according to the presence of current sharing and voltage-regulation loops. Computer simulations are presented to illustrate the characteristics of the various paralleling schemes.**

***Index Terms*—Control methods, current-sharing schemes, dc–dc converters, parallel connected converters, topology.**

I. Introduction

POWER supplies based on paralleling a number of switching converters offer several advantages over a single high-power centralized power supply, such as low component stresses, increased reliability, ease of maintenance and repair, improved thermal management, etc. [1]–[4]. Paralleling of standardized converters will continue to be a popular approach adopted in distributed power systems for both front-end and load converters.

One basic objective of parallel connected converters is to share the load current among the constituent converters. To do this, some form of control has to be used to equalize the currents in the individual converters. A variety of approaches, with varying complexity and current-sharing performance, have been proposed in the past two decades [5]–[9]. In general, methods for paralleling dc–dc converters are described in terms of connection styles, control configurations and feedback functions. Although some forms of classifications and comparisons have been given for paralleling schemes [10]–[12], most fall short of a systematic identification of all possible structures and control configurations. For instance, in Luo *et al.* [10], a classification has been given based on the existing paralleling methods. Basically, Luo *et al.* categorized the methods into two categories according to the type of current-sharing method, namely, passive droop methods and active current-sharing methods. They reported five specific schemes that exploit the droop characteristics of the converters, and two specific schemes that use active-current sharing methods, i.e., the master–slave scheme and the average scheme. In addition, three control structures, namely, inner loop regulation, outer loop regulation and external control, were identified. Their classification is thus basically a systematic collection of existing schemes. Other classification works, such as Liu *et al.* [11] and Choi [12], focus on the control loop configurations of selected active current-sharing paralleling schemes.

In order to facilitate design and choice of appropriate paralleling configurations, a systematic classification of the paralleling schemes that permits a clear exposure of the structures, behaviors and limitations of all possible schemes, is needed. In this paper, we investigate the classification problem and utilize basic circuit theory to identify the basic structures and control methods of paralleled dc–dc converters. Our objective is to provide a simple classification that eliminates redundancy, includes all possible basic structures, permits comparative analysis of different structures, and hence allows systematic derivation of paralleling schemes.

Our starting point will be the two Kirchhoff's laws that dictate the possible connection styles. Considering converters as either voltage sources or current sources, we define three basic structures for paralleling converters. As we will see, these structures actually form the basis of all practical paralleling schemes. We will develop equivalent models which can be used in analysis. Furthermore, control methods will be systematically introduced to complete the output regulation and current-sharing functions. Finally, computer simulations will be presented to provide a full comparison of the various configurations.

II. Basic Circuit Theory of Parallel Connections

A. Basic Constraints in Paralleling Independent Sources

The output of any converter is normally expected to provide regulated voltage or current. Thus, an appropriate model for a converter (seen at output terminals) is either a voltage source or a current source. Two basic laws must be obeyed when connecting sources together. First, Kirchhoff's voltage law (KVL) dictates that the sum of voltages of all branches (in the same sense) forming a loop must equal zero. This means that no two independent voltage sources are permitted to be connected in parallel. Theoretically, even if the voltage sources are of the same magnitude, paralleling them is still not permitted as it makes the current values undefined [13]. Likewise, Kirchhoff's current law (KCL) dictates that the sum of currents of all branches in a cutset (emerging from the same sub-graph) must equal zero. This clearly eliminates the possibility of connecting two independent current sources in series. In this paper, as our focus is paralleling sources, we do not consider the case of connecting sources in series.

Manuscript received July 10, 2006. This work was supported by the Hong Kong Research Grants Council under CERG Project PolyU 5237/04E. This paper was recommended by Associate Editor S. Banerjee.

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Digital Object Identifier 10.1109/TCSI.2007.890631

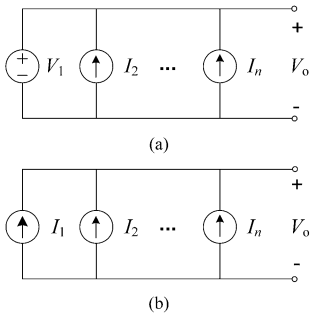

Fig. 1. Structures for paralleling ideal independent sources.

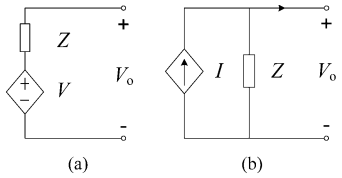

Fig. 2. Equivalent circuits for power converters. (a) Thévenin form. (b) Norton form.

From the above discussion, it is clear that independent sources can be connected in parallel under only two possible circumstances, as shown in Fig. 1. First, only one of them can be an independent voltage source, and the rest must be current sources, as shown in Fig. 1(a). The output voltage is decided by the voltage source branch, and the current in the voltage source is determined by the load. Second, all parallel branches are current sources, as shown in Fig. 1(b). The output voltage is decided by the load.

It should be clear that in practice, the voltage and current sources are not independent but are controlled sources in order to allow regulated output voltage and specific sharing of current to be maintained. Nonetheless, the aforementioned two basic configurations will form the basis of parallel connection styles. The applications of these connection styles and the associated control problem will be the main subjects of discussion of this paper.

B. Equivalent Circuits for DC–DC Power Converters

DC–DC converters are devices for processing power. For most practical purposes, a regulated output voltage or current is required of a converter, mandating the use of some feedback control to keep the converter unaffected by load and input disturbances. As a result, a dc–dc converter can be viewed as an imperfect voltage or current source with appropriate control of its magnitude in response to output and/or input variations [14]. In general, we may simply and generically represent a dc–dc converter in Thévenin form or Norton form, i.e., a dependent voltage behind a small impedance (at low frequency) or a dependent current source in parallel with a large impedance (at low frequency), as shown in Fig. 2.[1] Theoretically, the two representations are arbitrary. However, it should be clear that the Thévenin form is more suited for converters whose purpose is to achieve a regulated output voltage, whereas the Norton form is suited for converters whose purpose is to achieve a regulated output current. Obviously, voltage feedback is needed for the former case, and current feedback for the latter.

We should reiterate that the two equivalent representations are interchangeable except for the case where the equivalent output impedance is zero. Denoting the output impedance by Z and the loop gain by T, we may write

$$Z = \begin{cases} \frac{Z_o}{1+T}, & \text{for Thévenin form} \\ Z_o(1+T), & \text{for Norton form} \end{cases} \tag{1}$$

where Z_o is the open-loop output impedance. If the loop gain T is high enough, Z becomes negligibly small for the voltage source representation or very large for current source representation. The output characteristic of the converter resembles that of a nearly independent source.

III. General Classification of Parallel Connected DC–DC Converters

From the foregoing discussion, it is clear that any paralleling scheme involving voltage and current sources must comply with the two basic structures described earlier. Moreover, if the voltage sources are imperfect (i.e., with a nonzero output impedance), they can still be connected in parallel. Thus, we have three basic configurations for paralleling imperfect sources.[2]

When dc–dc converters are treated as imperfect voltage or current sources, three basic configurations for paralleling practical dc–dc converters can be developed, as summarized in Fig. 3. For brevity, we refer to these configurations as Types I, II, and III connections. For a voltage source branch, we have

$$V_o = V_i - I_{o,i}Z_i \quad \text{or} \quad I_{o,i} = \frac{V_i - V_o}{Z_i} \tag{2}$$

where subscript i (1 to n) indicates the branch number, and $I_{o,i}$ is the output current of the ith branch, i.e., the part of load current shared by the ith branch. For a current source branch, we have

$$V_o = (I_i - I_{o,i})Z_i \quad \text{or} \quad I_{o,i} = I_i - \frac{V_o}{Z_i} \tag{3}$$

where I_i is the equivalent current source of the ith branch.

In practice, we need to apply appropriate control to dc–dc converters in order to "cast" them as voltage or current sources. For instance, a voltage feedback loop is obviously needed for controlling a dc–dc converter so that it behaves as a voltage source. Thus, the paralleling configurations are closely related to the control method which effectively determines whether a dc–dc converter would behave as a voltage or current source.

In addition to the defining control of current and voltage sources, a current sharing control can be used to ensure even sharing of the load current among the converters. In a parallel converter system, each constituent converter is a power supply. To avoid confusion, we will use the term *current-sharing loop* in a specific context. If a current-sharing reference is derived from the output currents of one/all constituent converters, the control scheme is said to contain a *current-sharing loop.*

[1]By "small" impedance and "large" impedance, we actually refer to the modulus of the impedance.

[2]By imperfect sources, we mean those voltage sources having nonzero output impedance and those current sources having finite output impedance.

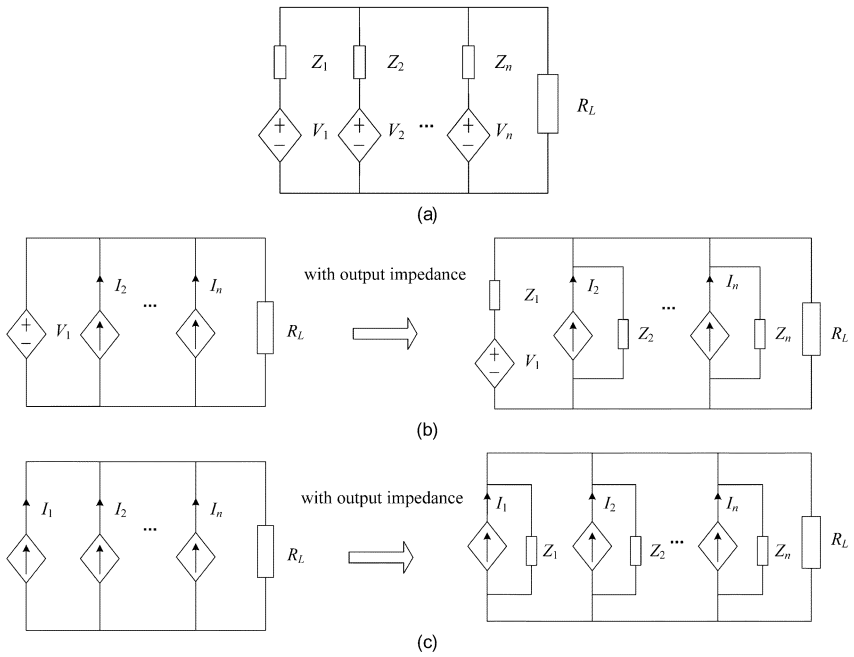

Fig. 3. Three configurations for paralleling converters. (a) Type I. (b) Type II, with practical form on the right. (c) Type III, with practical form on the right.

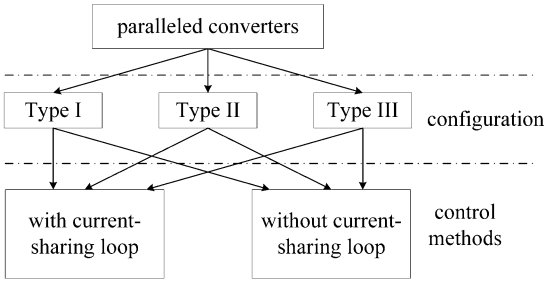

Fig. 4. Systematic classification of parallel connected converters.

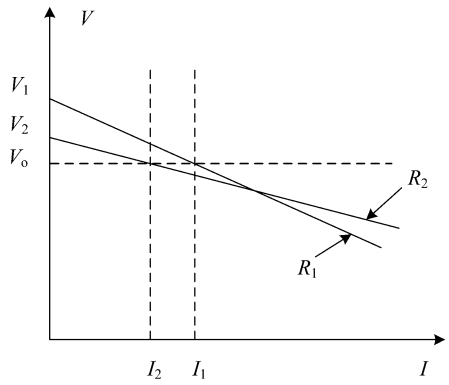

Fig. 5. Output characteristics of two parallel connected converters.

Otherwise, the control scheme does not have a current-sharing loop.

We may therefore further classify parallel converter systems according to the presence of a current-sharing loop, resulting in a simple, systematic classification, as shown in Fig. 4. Two layers are included in the classification. In the first layer, we get three configurations, Types I, II, and III, based on the circuit theoretic connection styles. In the second layer, the presence of a *current-sharing loop* is the classifying criterion.

IV. Three Types of Connection Styles and Associated Control Methods

In this section, in light of the classification framework mentioned in the foregoing, the various types of parallel connected dc–dc converters are described in detail. Our emphases here are the generic circuit theoretic structures and the necessary control methods. As a prerequisite, we note that converters aiming to imitate voltage sources should have tight voltage feedback loops for voltage regulation purposes, whereas converters imitating current sources would necessitate some form of current-mode control in order to set the current magnitudes. The presence of current-sharing loop is an additional feature, contributing to the current sharing of the constituent converters.

A. Type I

The Type-I connection is shown in Fig. 3(a). Each branch represents a converter, which is basically a Thévevin source, i.e., a dependent voltage source behind an output impedance. For the control without current-sharing loop, the branches are simply connected in parallel. However, the absence of a current-sharing loop imposes some specific requirements on the individual branches in order to provide natural current sharing [15], [16]. This has been commonly known as the *droop method* [7], [17]. Specifically, each converter (branch), in the absence of a current-sharing loop, should have a finite output resistance at steady state.

As an example, Fig. 5 shows the output characteristics of two converters connected in parallel, without employing a current-sharing loop. Suppose the output current, equivalent Thévenin voltage and output resistance of converter i (branch i) is I_i, V_i

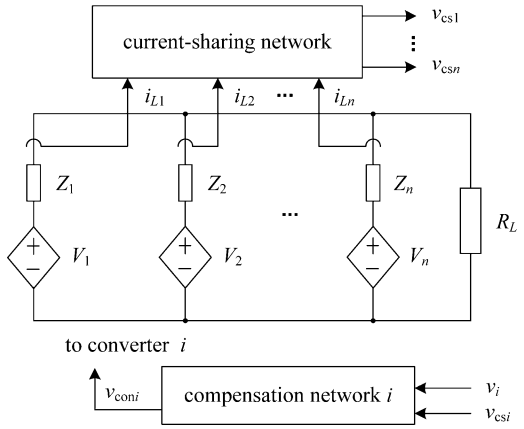

Fig. 6. Control structure for Type-I configuration with current-sharing loop.

and R_i, respectively, and the common output voltage is V_o. The current sharing error is expressed as

$$\Delta I = I_1 - I_2 = \frac{R_2V_1 - R_1V_2 + 2(V_1 - V_2)R_L}{R_x} \quad (4)$$

where R_L is the load resistance and $R_x = R_1R_2 + R_1R_L + R_2R_L$. The current error ΔI will be zero only if $V_1 = V_2$ and $R_1 = R_2$. Thus, in practice, current sharing can be achieved by adjusting V_1, V_2, R_1 and R_2.

For Type-I connection with current-sharing loop, since all converters are Thévenin sources, output regulation and current sharing are achieved by controlling $V_1, V_2, \ldots, V_n$ and/or the output impedance $Z_1, Z_2, \ldots, Z_n$. The control structure is shown in Fig. 6, where the equivalent voltage sources are controlled to obtain current sharing. In this configuration, each converter is an dependant voltage source under voltage feedback control. In Fig. 6, v_{csi} represents the control information provided by current sharing, v_i and v_{coni} are the feedback voltage and switch control signal of converter i, respectively. In the current-sharing network, the currents sensed from different converters are first programmed to obtain a common current control signal, which will be compared with the individual currents to generate v_{csi}. Then, v_{csi} is used to regulate individual equivalent voltages $V_1, V_2, \ldots, V_n$. The control objective is to ensure that all converters share the load equally.

B. Type II

For the Type-II connection shown in Fig. 3(b), one converter serves as the voltage (Thévenin) source and others are current (Norton) sources. The control structure without current-sharing loop is shown in Fig. 7(a). There is a main voltage feedback loop, which acts on the voltage (Thévenin) source to regulate the output voltage. Other branches are under current-mode control, whose objective is to make all individual output currents share the same portion of the load current [18]. The current in the voltage source branch is thus controlled indirectly (automatically) in the equilibrium state, i.e., $I_1 = V_o/R_L - I_2 - \cdots - I_n$. Thus, the current for each converter is equal to I_o/n, where $I_o = V_o/R_L$.

For the Type-II configuration with current-sharing loop, a variety of control methods can be used to fabricate the voltage source and current sources. The control structure is shown in Fig. 7(b). Again, there is a main voltage feedback loop to control the voltage source branch. The current control signal i_{con} for the current source branches will be derived from the voltage source branch. This control signal is then compared with the individual current of the $n-1$ converters to achieve current sharing. This control method is commonly known as *master–slave current-sharing method* [19]–[21], where the voltage source is the master and the current sources are the slaves whose currents are programmed to follow the master's.

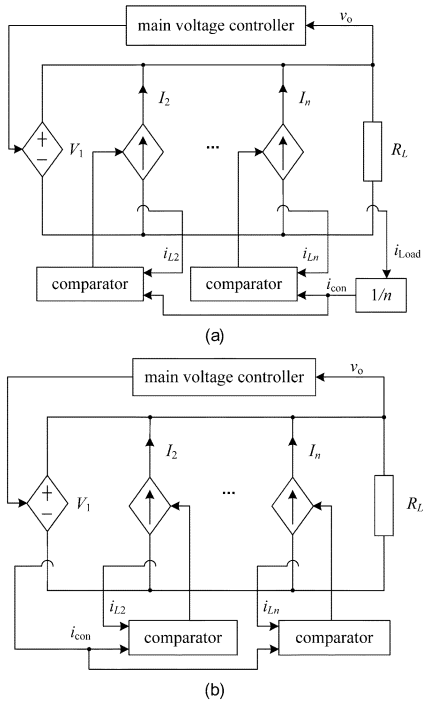

Fig. 7. Control structures for Type-II configuration (a) without current-sharing loop, and (b) with current-sharing loop (also known as master–slave current sharing).

C. Type III

In the Type-III configuration shown in Fig. 3(c), all converters are current (Norton) sources. In the absence of a current-sharing loop, all converters have to follow a current control signal i_{con} which is derived from the output voltage feedback loop, as shown in Fig. 8(a). The voltage feedback loop aims to achieve voltage regulation as well as current sharing. In the ideal case, the load current is distributed equally, i.e., $I_1 = I_2 = \cdots = I_n$. A simple implementation can be found in Iu *et al.* [22].

Finally, for the Type-III configuration with current-sharing loop, all converters are under current-mode control so that they behave as good current sources. Current-programming methods, such as master–slave method or average method, can be used to generate the common current-sharing control signal [23], [24]. The amplified errors between the current-sharing control signal and the feedback currents $v_{cs1}, v_{cs2}, \ldots, v_{csn}$, are injected to the feedback loop, adjusting the current control signals $i_{con1}, i_{con2}, \ldots, i_{connn}$. The basic structure is shown in Fig. 8(b).

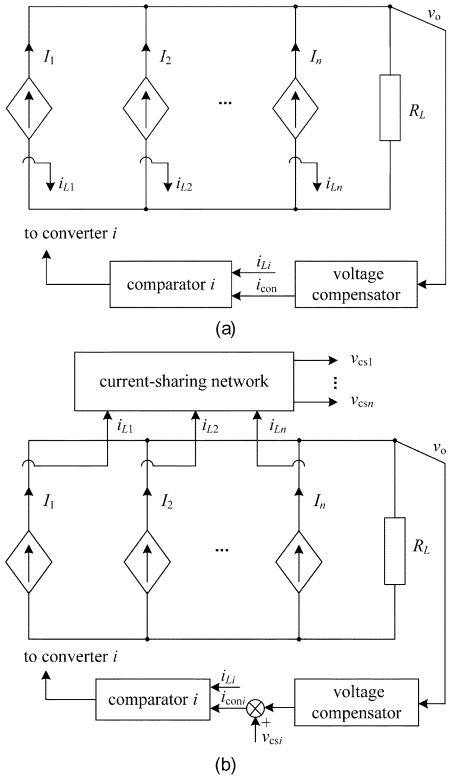

Fig. 8. Control structures for Type-III configuration (a) without current-sharing loop and (b) with current-sharing loop (also known as democratic current sharing).

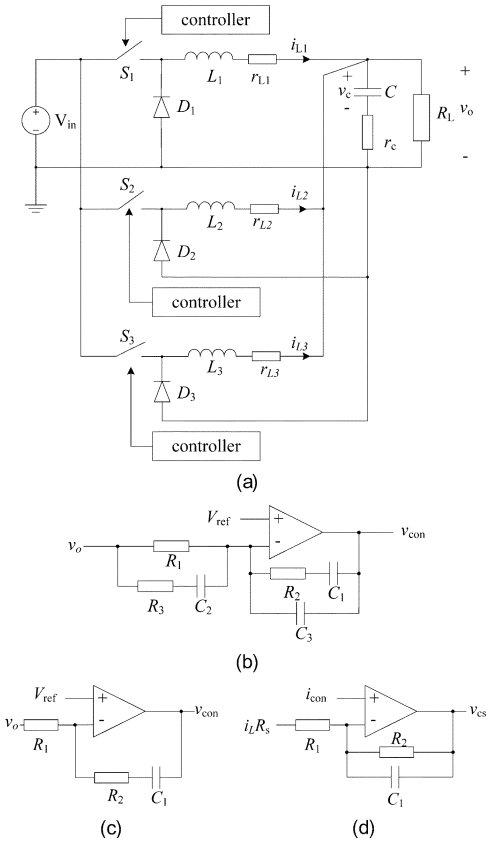

Fig. 9. Paralleled converters and the compensator networks. (a) Three parallel-connected buck converters. (b) Two-zero two-pole compensator. (c) Proportional-integral compensator. (d) Single-pole compensator.

V. Comparison of Paralleling Schemes

In the foregoing section, we have discussed the structures and the associated control methods for paralleling dc–dc converters. In this section, we compare the different structures and control methods in terms of current-sharing accuracy, voltage regulation, dynamical performance, etc. Intuitively, we can make the following general observations:

1) Type-I schemes are simple but suffer fundamentally from paralleling voltage sources. The adjustment range for current sharing is small since each constituent converter is designed primarily to regulate its local output voltage, and the currents in the converters can only be adjusted by controlling the voltages which are not allowed to vary too much.
2) Type-II schemes are theoretically more viable as there is only one voltage source, paralleling with current sources. The dynamics of the voltage regulation thus depends on the control method being employed by the voltage regulating loop. The other current source converters control their currents directly to achieve the desired current sharing. Thus, the current-sharing performance is generally much better compared to Type-I schemes.
3) Type-III schemes are more complicated in terms of implementation due to substantial current programming requirements. However, Type-III schemes are generally best in terms of current sharing as all converters are fundamentally current controlled. The voltage regulation can also enjoy fast response due to the direct load voltage control.

For a detailed comparison, we consider a system of three buck converters connected in parallel, as shown in Fig. 9(a). Fig. 9(b)–(d) shows the controllers used in the simulations for voltage regulation and current sharing. In our simulations, models are constructed using MATLAB/SIMULINK.

As it is important to ensure generality of any conclusion made in our study, we have consistently used the same type of compensation networks and equivalent values of control parameters in order to ensure that fair comparison can be made and generally valid conclusions are drawn. Here, we have chosen the most typical compensation networks for the different control situations. Specifically, for voltage-mode buck converters, we employ a typical two-zero two-pole compensator, as shown in Fig. 9(b). Denoting the Laplace transforms of the control signal and converter output signal as $V_{\rm con}(s)$ and $V_o(s)$, respectively, the transfer function is

$$\frac{V_{\rm con}(s)}{V_o(s)} = -\frac{\omega_i(1+s/\omega_{z1})(1+s/\omega_{z2})}{s(1+s/\omega_{p1})(1+s/\omega_{p2})} \tag{5}$$

where $\omega_i = 1/(R_1(C_1+C_3))$, $\omega_{z1} = 1/(R_2C_1)$, $\omega_{z2} = 1/(C_2(R_1+R_3))$, $\omega_{p1} = 1/(R_3C_2)$, $\omega_{p2} = (C_1+C_3)/(R_2C_1C_3)$. For the current-mode control, moreover, the outer voltage feedback loop employs a PI controller, as shown in Fig. 9(c). The transfer function is

$$\frac{V_{\rm con}(s)}{V_o(s)} = -\frac{K(1+s/\omega_{zv})}{s} \tag{6}$$

TABLE I
POWER STAGE COMPONENT VALUES USED IN SIMULATIONS

Circuit Components	Values
Switching Period T_s	10 μs
Input Voltage V_{in}	24 V
Output Voltage V_o	12 V
Inductance L_1, ESR r_{L1}	300 μH, 0.01 Ω
Inductance L_2, ESR r_{L2}	200 μH, 0.1 Ω
Inductance L_3, ESR r_{L3}	100 μH, 0.05 Ω
Capacitance C, ESR r_c	126 μF, 0.01 Ω
Load Resistance R_L	1 Ω

TABLE II
CONTROLLER PARAMETERS USED IN SIMULATIONS (UNIT FOR ALL ω'S: RAD/S, UNIT FOR K: RAD/S, UNIT FOR K_{cs}: Ω)

	Type I		Type II		Type III	
	without current-sharing loop	with current-sharing loop	without current-sharing loop	with current-sharing loop	without current-sharing loop	with current-sharing loop
ω_i	4.5×10^2	4.5×10^2	2.6×10^3	2.6×10^3	–	–
ω_{z1}	2×10^3	2×10^3	2×10^3	2×10^3	–	–
ω_{z2}	6×10^3	6×10^3	6×10^3	6×10^3	–	–
ω_{p1}	2×10^5	2×10^5	2×10^5	2×10^5	–	–
ω_{p2}	3×10^5	3×10^5	3×10^5	3×10^5	–	–
K	–	–	–	–	4.8×10^4	4.8×10^4
ω_{zv}	–	–	–	–	6×10^3	6×10^3
K_{cs}	–	0.7	–	–	–	0.7
ω_{pcs}	–	1×10^5	–	–	–	1×10^5

where $K = 1/(R_1C_1)$, $\omega_{zv} = 1/(R_2C_1)$. Finally, for current-sharing loops, we employ a simple single-pole compensator, as shown in Fig. 9(d). Denoting the Laplace transforms of the control voltage and the inductor current as $V_{cs}(s)$ and $I_L(s)$, the transfer function is given by

$$\frac{V_{cs}(s)}{I_L(s)} = -\frac{K_{cs}}{1+s/\omega_{pcs}} \tag{7}$$

where $K_{cs} = R_sR_2/R_1$, $\omega_{pcs} = 1/(R_2C_1)$. The current sharing control signal, i_{con}, is the average value of all inductance currents, i.e., $i_{con} = (1/n)\sum_{i=1}^{n} i_{Li}$.

The component values used in the simulations are listed in Table I. For different types of paralleling schemes, appropriate controllers, as shown in Fig. 9(b)–(d), are selected and designed to ensure that the same voltage loop bandwidth is achieved, i.e., about 10 kHz. The parameters used in the controllers are shown in Table II.

For the Type-I configuration, each converter is under voltage-mode control. For the paralleling scheme without current-sharing loop (droop scheme), extra current feedback is used to produce a droop in the output voltage, where the equivalent droop resistance is proportional to the current feedback gain [10]. Figs. 10 and 11 show the output voltage and current waveforms under a stepped load condition. In Fig. 10, we also illustrate the effect of the output resistance, which is crucial to this kind of droop scheme. The output resistance used for simulations of Fig. 10(a) and (b) is ten times larger than that used for the simulations of Fig. 10(c) and (d). From the simulation results, we clearly see that the Type-I scheme without current-sharing loop does not perform very satisfactorily. Normally, with large output resistance, we may achieve good current sharing but poor output regulation. However, the current sharing becomes worse and output regulation becomes better with smaller output resistance. This remains the fundamental limitation of such droop schemes, as multiple nonidentical voltage sources are paralleled and there is only a very narrow adjustment range for controlling the currents via the voltage drops in the output resistances.

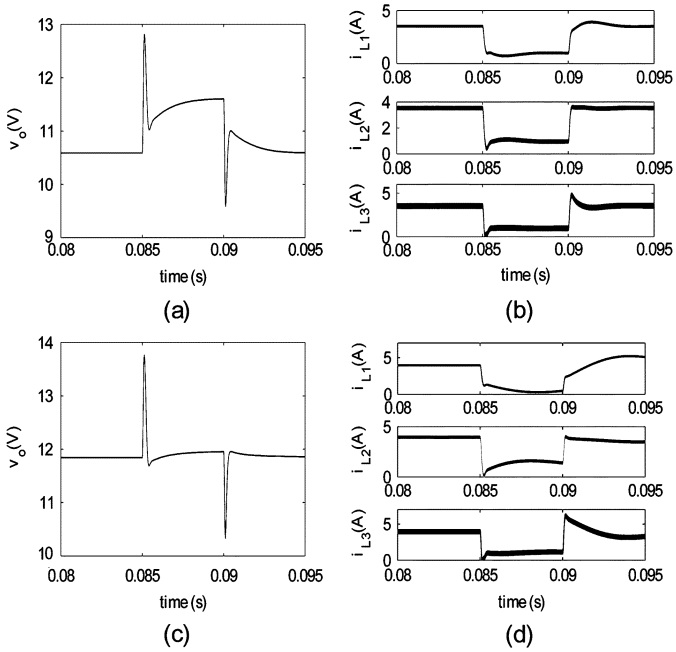

Fig. 10. Simulation results for stepped load for Type-I scheme without current-sharing loop. (a) Output voltage with large output resistance. (b) Converter output currents with large output resistance. (c) Output voltage with small output resistance. (d) Converter output currents with small output resistance.

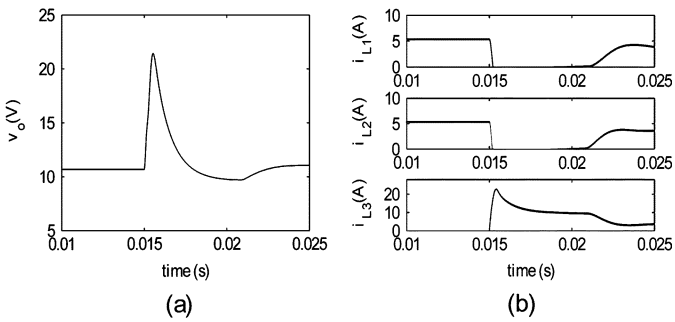

Fig. 11. Simulation results for plug-in transient for Type-I scheme without current-sharing loop. (a) Output voltage. (b) Converter output currents.

Another dynamical test is the plug-in transient. Initially, two converters share the load. Then, a third converter plugs in and shares the load with the other two operating converters. The results are shown in Fig. 11 for the Type-I paralleling scheme without current-sharing loop. The currents in the two operating converters drop to zero during the plug-in transient. Such blackout is undesirable as it imposes high current stress on the third converter during the transient.

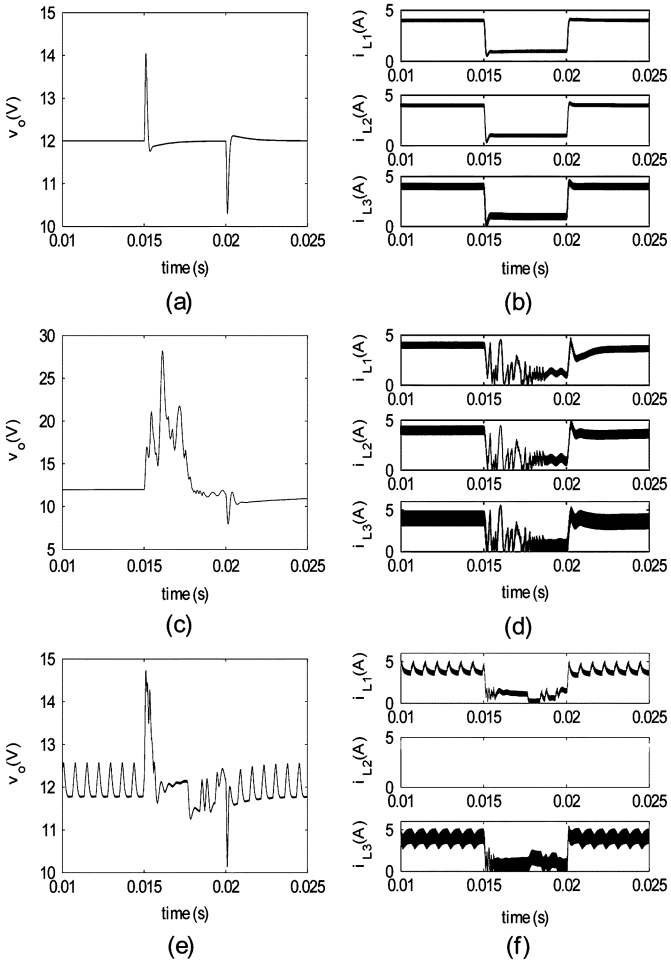

Fig. 12. Simulation results for stepped load for Type-I scheme with current-sharing loop. (a)–(b) Stable operation with parameter values shown in Table II. (c)–(d) Unstable operation for large current-sharing gain ($K_{\rm cs} = 5\ \Omega$). (e)–(f) Unstable operation for large voltage feedback gain ($\omega_i = 3.1 \times 10^3$ rad/s).

With current-sharing loop, the Type-I scheme performs better, as demonstrated in Fig. 12(a) and (b) and Fig. 13. Moreover, as would be expected, increasing the current-sharing gain and/or the voltage feedback gain would affect the stability of the system. As shown in Fig. 12(c) and (d), the system becomes unstable when the current-sharing gain increases. Likewise, the system becomes unstable when the voltage feedback gain is large, as shown in Fig. 12(e) and (f). This is because the current-sharing error signal outside of the voltage loop is amplified and fed back to the voltage loop causing possible unstable behavior if the current-sharing gain or the voltage feedback gain is too large. To get stable operation, we have to limit these gains, which also limit the dynamic response. The plug-in transient is shown in Fig. 13. The system rebalances itself without drastic blackout of individual converter currents. This is an improvement over the Type-I scheme without current-sharing loop.

Shown in Figs. 14 and 15 are simulation results for the Type-II scheme without current-sharing loop. As shown in Fig. 14, satisfactory dynamic response under stepped load change is demonstrated. However, the current-sharing accuracy relies on the precision of the current divider. Small variation

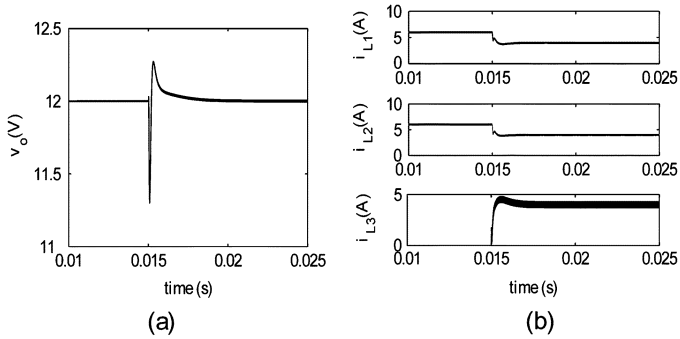

Fig. 13. Simulation results for plug-in transient for Type-I scheme with current-sharing loop. (a) Output voltage. (b) Converter output currents.

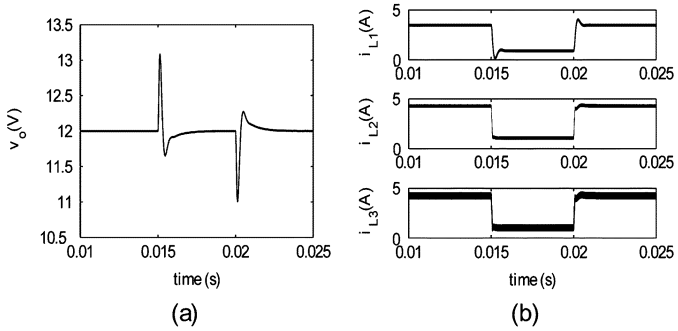

Fig. 14. Simulation results for stepped load for Type-II scheme without current-sharing loop. (a) Output voltage. (b) Converter output currents.

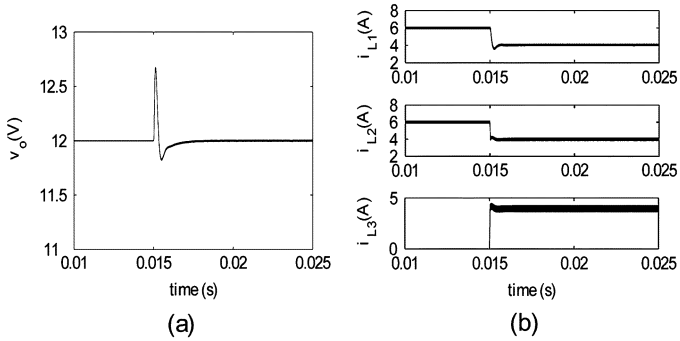

Fig. 15. Simulation results for plug-in transient for Type-II scheme without current-sharing loop. (a) Output voltage. (b) Converter output currents.

of the current divider can give large current-sharing errors between the voltage converter and current converters. In this case, we observe current-sharing errors from 6.25% to 13.25% ($i_{L1} = 3.47$ A, $i_{L2} = 4.28$ A, $i_{L3} = 4.25$ A). Also, the plug-in transient is shown in Fig. 15. The system is able to rebalance itself without causing current blackout, though fairly slowly with settling time of around 2 ms in this case.

In Figs. 16 and 17, we show the simulation results for the Type-II scheme with current-sharing loop. As seen from Fig. 16, satisfactory dynamic response under stepped load change is demonstrated. Also, the current-sharing accuracy is improved compared to the Type-II scheme without current-sharing loop, with current-sharing errors from 1.25% to 5% ($i_{L1} = 4.05$ A, $i_{L2} = 4.15$ A, $i_{L3} = 3.8$ A) in this case. This is because the slaves set their currents to equal that of the master via

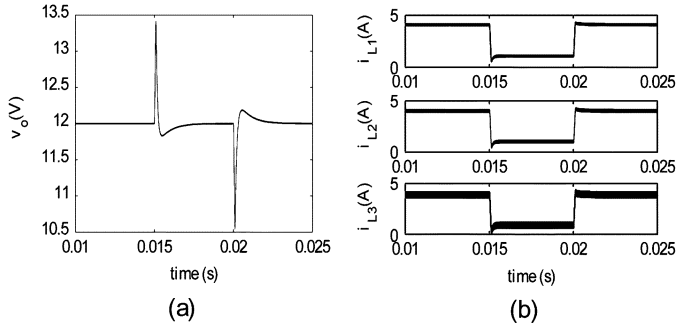

Fig. 16. Simulation results for stepped load for Type-II scheme with current-sharing loop. (a) Output voltage. (b) Converter output currents.

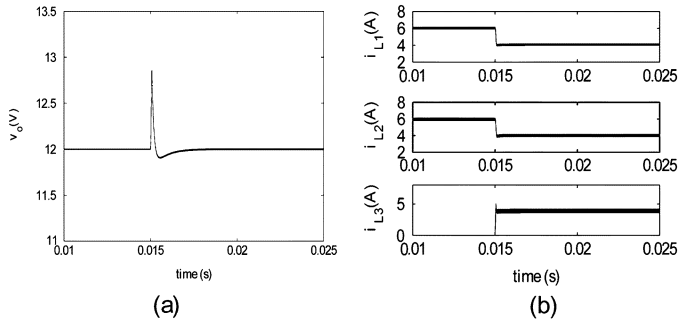

Fig. 17. Simulation results for plug-in transient for Type-II scheme with current-sharing loop. (a) Output voltage. (b) Converter output currents.

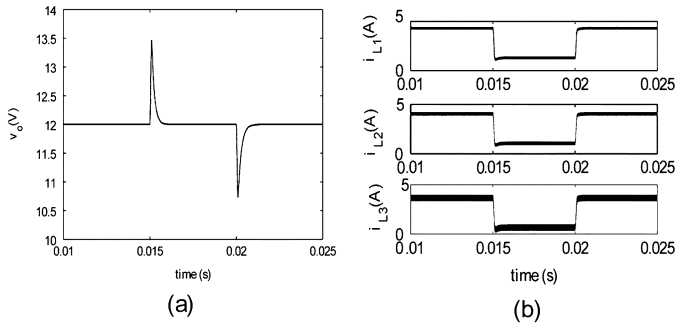

Fig. 18. Simulation results for stepped load for Type-III scheme without current-sharing loop. (a) Output voltage. (b) Converter output currents.

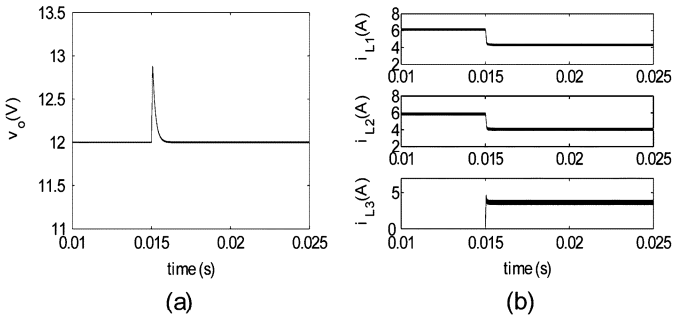

Fig. 19. Simulation results for plug-in transient for Type-III without current-sharing loop. (a) Output voltage. (b) Converter output currents.

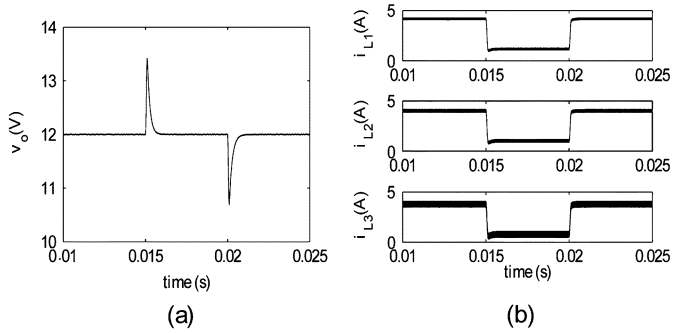

Fig. 20. Simulation results for stepped load for Type-III scheme with current-sharing loop. (a) Output voltage. (b) Converter output currents.

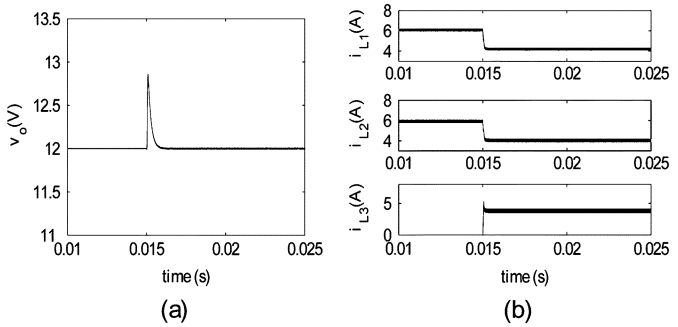

Fig. 21. Simulation results for plug-in transient for Type-III scheme with current-sharing loop. (a) Output voltage. (b) Converter output currents.

comparison their currents with the master's. Here, we clearly confirm our earlier theoretical analysis that only one voltage loop is enough to regulate the output voltage. However, the master should be as fast as possible to provide stable reference for the slaves. Moreover, Fig. 17 shows satisfactory rebalancing after a plug-in transient, with a settling time of around 1.2 ms.

Results for the Type-III scheme without current-sharing loop are shown in Figs. 18 and 19. Here, we observe satisfactory dynamic response for large load change. However, the current-sharing errors are quite large (1.25% to 8.75% in this case, $i_{L1} = 4.3$ A, $i_{L2} = 4.05$ A, $i_{L3} = 3.65$ A) because it is sensitive to the current comparator due to the absence of current sharing comparison. Moreover, as shown in the plug-in transient of Fig. 19, the re-balancing can be achieved very quickly with a settling time of less than 1 ms.

Finally, for the Type-III scheme with current-sharing loop, the simulation results are shown in Figs. 20 and 21. In this case we observe very fast dynamic response, and very precise current sharing, with current-sharing errors from 0% to 3.75% in this case ($i_{L1} = 4.15$ A, $i_{L2} = 4$ A, $i_{L3} = 3.85$ A). Further improvement of current sharing can be obtained by adjusting the current-sharing compensator. Also, very fast re-balancing after a plug-in transient can be observed, as shown in Fig. 21.

From the foregoing simulation results, we may summarize the general features of the three configurations and their control methods. In short, Type-I schemes, though simple, suffer from some fundamental limitations as voltage sources are being paralleled. Type-II schemes have one voltage source paralleling a number of current sources. The voltage regulation performance thus depends of the feedback arrangement of the voltage source. Current sharing is much easy to be obtained than that of Type-I schemes. Type-III schemes are basically parallel current sources. They achieve very fast response and generally good current sharing as voltage regulation is based on the load

TABLE III
COMPARISON OF PARALLELING SCHEMES

		Advantages	Disadvantages
Type I	without current-sharing loop	• Ease of expansion (high modularity) • Simplicity	• Poor dynamic response • Poor voltage regulation due to the exploitation of large output resistance for current sharing • Poor current-sharing accuracy
	with current-sharing loop	• Ease of expansion (high modularity) • Good voltage regulation • Reasonably good current sharing for narrow ranges of parameters	• Dynamic performance generally not optimized for large load range (low gain has to be used for stability in a wide load range) • Relatively slow dynamic response • Not robust to variation of current-sharing gain
Type II	without current-sharing loop	• Good voltage regulation • Reasonably good current sharing due to direct current control • Reasonably good dynamic response	• Accurate current sensor and divider needed at the load side • Low modularity due to the use of current divider
	with current-sharing loop	• Ease of expansion by adding slaves • Good voltage regulation • Good current sharing • Reasonably good dynamic response	• Current-sharing accuracy sensitive to master's current variation (poor noise immunity)
Type III	without current-sharing loop	• Ease of expansion by adding current sources • Reasonably good current sharing • Good dynamic response due to fast current control	• Current-sharing accuracy relies on precise choice of current loop parameters
	with current-sharing loop	• Precise current sharing • Good output regulation • Good dynamic response	• Complex control structure • Low modularity due to the need for interacting current-sharing loops

voltage feedback and current sharing is done via direct current control. Table III compares their relative pros and cons in terms of ease of expansion, dynamic performance, current-sharing accuracy and regulation capability.

VI. CONCLUSION

In this paper, a systematic classification of parallel connected switching power converters is given. Our starting point is circuit theory of connecting voltage and current sources as converters can be regarded as voltage or current sources. Three basic types of paralleling schemes can be identified, corresponding to: i) connecting Thévenin sources in parallel; ii) connecting one Thévenin source with many Norton sources in parallel and iii) connecting Norton sources in parallel. The presence of current-sharing loop has been considered as an optional feature, though its use has been clearly proven to be important for achieving good performance in current balancing. The classification presented in this paper allows the structures and control requirements of paralleling schemes to be systematically analyzed.

ACKNOWLEDGMENT

The authors wish to thank the reviewers for their comments and suggestions that have led to various improvements in the presentation of the paper.

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