

Bifurcation Behavior in Parallel-Connected Buck Converters

H. H. C. Iu and C. K. Tse

Abstract— This paper describes the bifurcation phenomena of a system of parallel-connected dc/dc buck converters. The results provide useful information for the design of stable current sharing in a master–slave configuration. Computer simulations are performed to capture the effects of variation of some chosen parameters on the qualitative behavior of the system. These are summarized in a series of bifurcation diagrams. In particular, it is found that while variation of the voltage feedback gains leads to standard period-doubling bifurcation, variation of the current sharing ratio leads to border collision bifurcation. Analysis is presented to establish the possibility of the bifurcation phenomena and to locate the current sharing ratio at which border collision occurs.

Index Terms— Bifurcation, buck converter, parallel dc–dc converter.

I. INTRODUCTION

Paralleling power converters allows high current to be delivered to loads without the need to employ devices of high power rating. The main design issue in parallel converters is the control of the sharing of current among the constituent converters. If a dc/dc converter is regarded as a voltage regulator that provides very stiff voltage to a load, then it is theoretically impossible to put two such converters in parallel feeding the same load and sharing equal current, unless the two converters are perfectly identical. In practice, mandatory control is needed to ensure proper current sharing, and many effective control schemes have been proposed in the past [1]–[4]. One common approach is to employ an active control scheme to force the current in one converter to follow that of the other. The essence of this control approach is to monitor the difference of the output currents in two constituent converters (i.e., *current error*) and incorporate this information in the main voltage control loop. Specifically, for the case of two converters connected in parallel, one converter simply has a voltage feedback control while the other has an additional inner current loop that provides the current error information which is used in turn to “adjust” the voltage feedback loop to ensure equal sharing of current. Such a scheme is commonly known as the *master–slave* current-sharing scheme [1], [3].

Nonlinear dynamics and bifurcation behavior are important topics of investigation in power electronics [5]–[12]. As parallel converter systems gain popularity in power electronics applications, there is a strong motivation for better understanding of their nonlinear dynamics and bifurcation behavior. In this paper, we attempt to probe into some nonlinear phenomena of a system of parallel-connected buck converters controlled under a master–slave current-sharing scheme.

II. MASTER–SLAVE CONTROLLED PARALLEL-CONNECTED DC/DC CONVERTERS

The system under study consists of two dc/dc converters which are connected in parallel feeding a common load. The current drawn by

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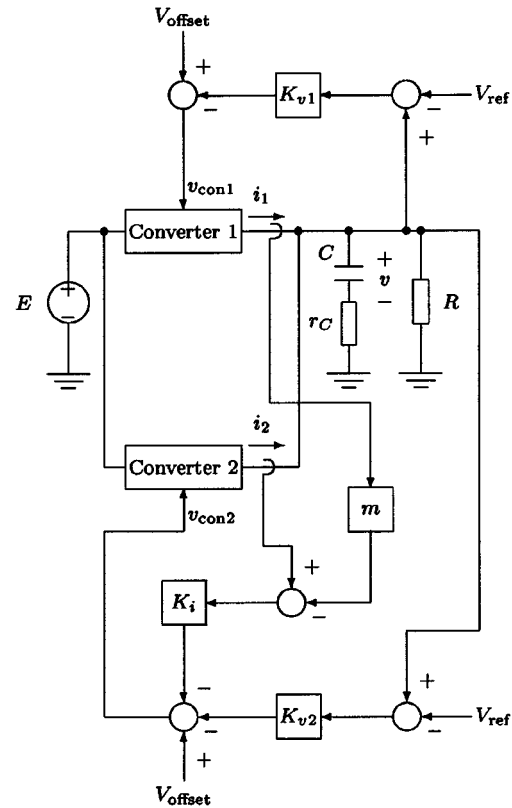


Fig. 1. Block diagram of parallel-connected dc/dc converters under a master–slave control.

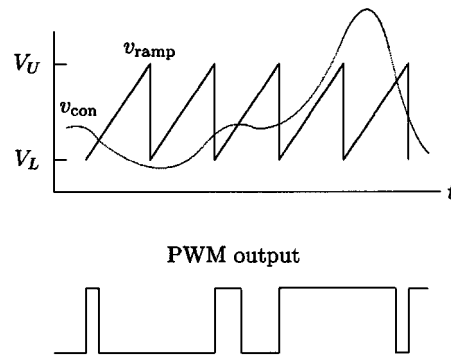


Fig. 2. Pulse-width modulation (PWM) showing relationship between the control voltage and the PWM output.

the load is shared properly between the two buck converters by the action of a master–slave control scheme, as mentioned briefly in the preceding section. Fig. 1 shows the block diagram of this master–slave configuration.

Denoting the two converters as Converter 1 and Converter 2 as shown in Fig. 1, the operation of the system can be described as follows. Both converters are controlled via a simple pulse-width modulation (PWM) scheme, in which a control voltage v_{con} is compared with a sawtooth signal to generate a pulse-width modulated signal that drives the switch, as shown in Fig. 2. The sawtooth signal of the PWM generator is given by

$$v_{ramp} = V_L + (V_U - V_L) \frac{t \bmod T}{T} \quad (1)$$

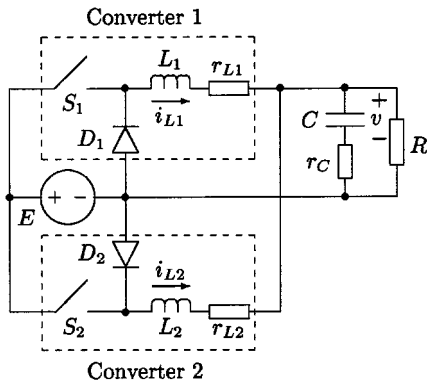


Fig. 3. Two parallel-connected buck converters.

where V_L and V_U are the lower and upper voltage limits of the ramp, and T is the switching period. The PWM output is “high” when the control voltage is greater than V_{ramp} , and is “low” otherwise.

For Converter 1, the control voltage is derived from a voltage feedback loop, i.e.,

$$v_{\text{con1}} = V_{\text{offset}} - K_{v1}(v - V_{\text{ref}}) \quad (2)$$

where

- V_{offset} dc offset voltage that gives the steady-state duty cycle;
- V_{ref} reference voltage;
- K_{v1} voltage feedback gain for Converter 1.

For Converter 2, an additional current error signal, which is proportional to the weighted difference of the output currents of the two converters, determines the control voltage. Specifically we write the control voltage for Converter 2 as

$$v_{\text{con2}} = V_{\text{offset}} - K_{v2}(v - V_{\text{ref}}) - K_i(i_2 - mi_1) \quad (3)$$

where

- K_{v2} voltage feedback gain of Converter 2;
- K_i current feedback gain;
- m current weighting factor.

Under this scheme, the output current of Converter 2 will follow that of Converter 1 at a ratio of m to 1, where $m > 0$. When $m = 1$, we expect equal current sharing. In much of the literature, Converter 1 is referred

to as the “master” which operates independently, and Converter 2 the “slave” which imitates the master’s current value.

III. STATE EQUATIONS FOR TWO PARALLEL BUCK CONVERTERS

The foregoing section defines the essential control scheme that provides current sharing and output voltage regulation. In this section we focus on a specific converter type and derive the state equations that will be needed for subsequent simulation study as well as analysis of the nonlinear phenomena of parallel-connected converters. Specifically, we will focus on the buck converter which is a second-order circuit comprising an inductor, a diode, a switch and a load resistance connected in parallel with a capacitor. Fig. 3 shows two buck converters connected in parallel. The presence of four switches (S_1 , S_2 , D_1 and D_2) allows a total of 16 possible switch states, and in each switch state, the circuit is a linear third-order circuit.

When the converters are operating in continuous conduction mode, diode D_i is always in complementary state to switch S_i , for $i = 1, 2$. That is, when S_i is on, D_i is off, and vice versa. Hence, only four switch states are possible during a switching cycle. These are: 1) S_1 and S_2 are on; 2) S_1 is on and S_2 is off; 3) S_1 is off and S_2 is on; and 4) S_1 and S_2 are off. The state equations corresponding to these switch states are generally given by

$$\begin{aligned} \dot{x} &= A_1 x + B_1 E, & \text{for } S_1 \text{ and } S_2 \text{ on} \\ \dot{x} &= A_2 x + B_2 E, & \text{for } S_1 \text{ on and } S_2 \text{ off} \\ \dot{x} &= A_3 x + B_3 E, & \text{for } S_1 \text{ off and } S_2 \text{ on} \\ \dot{x} &= A_4 x + B_4 E, & \text{for } S_1 \text{ and } S_2 \text{ off} \end{aligned} \quad (4)$$

where E is the input voltage, x is the state vector defined as

$$x = [v \quad i_1 \quad i_2]^T \quad (5)$$

and the A s and B s for the case of two buck converters are given by (6) and (7) as shown at the bottom of the page.

It is worth noting that the sequence of switch states, in general, takes the order as written in (4), i.e., starting with “ S_1 and S_2 on” and ending with “ S_1 and S_2 off” in a switching cycle. However, either “ S_1 on S_2 off” or “ S_1 off S_2 on” (not both) goes in the middle, depending upon the duty cycles of S_1 and S_2 . In the case where S_1 has a larger duty cycle, we should omit the third equation in (4), and likewise for the case where S_2 has a larger duty cycle. This should be taken care of in the simulation and analysis.

$$A_1 = A_2 = A_3 = A_4 = \begin{bmatrix} -\frac{1}{C(R+r_C)} & \frac{R}{C(R+r_C)} & \frac{R}{C(R+r_C)} \\ -\frac{R}{L_1(R+r_C)} & -\frac{1}{L_1} \left(\frac{r_C R}{R+r_C} + r_{L1} \right) & -\frac{1}{L_1} \left(\frac{r_C R}{R+r_C} \right) \\ -\frac{R}{L_2(R+r_C)} & -\frac{1}{L_2} \left(\frac{r_C R}{R+r_C} \right) & -\frac{1}{L_2} \left(\frac{r_C R}{R+r_C} + r_{L2} \right) \end{bmatrix} \quad (6)$$

$$B_1 = \begin{bmatrix} 0 \\ \frac{1}{L_1} \\ \frac{1}{L_2} \end{bmatrix}; \quad B_2 = \begin{bmatrix} 0 \\ \frac{1}{L_1} \\ 0 \end{bmatrix}; \quad B_3 = \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L_2} \end{bmatrix}; \quad B_4 = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \quad (7)$$

TABLE I
COMPONENT VALUES AND STEADY-STATE VOLTAGES USED IN SIMULATION

Circuit Components	Values
Switching Period T	$400\mu\text{s}$
Input Voltage E	48V
Output Voltage v	24V
Offset Voltage V_{offset}	5V
Inductance L_1 , ESR r_{L1}	0.02H, 0.05 Ω
Inductance L_2 , ESR r_{L2}	0.04H, 0.2 Ω
Capacitance C , ESR r_C	47 μF , 0.01 Ω
Load Resistance R	10 Ω

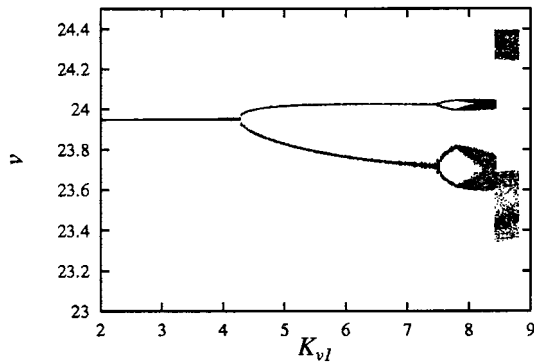


Fig. 4. Bifurcation diagram with K_{v1} as bifurcation parameter ($K_{v2} = 4$, $K_i = 5$ and $m = 1$), first period-doubling occurs when $K_{v1} = 4.47$.

IV. SELECTED BIFURCATION PHENOMENA BY COMPUTER SIMULATIONS

We now begin our investigation with computer simulations. Since we are primarily concerned with system stability in conjunction with the feedback design, we will focus our attention on the effects of varying the various gains on the bifurcation behavior of the system. In particular, the gains K_{v1} , K_{v2} , K_i and m present themselves as design parameters that can be changed at will. We will henceforth focus on variation of these parameters.

Our simulation is based on the exact state equations derived in Section III. Essentially, for each set of parameter values, time-domain cycle-by-cycle waveforms are generated by solving the appropriate linear equation in any sub-interval of time, according to the states of the switches which are determined from values of the control voltages $v_{\text{con}1}$ and $v_{\text{con}2}$. Sampled data are then collected at $t = nT$ in the steady state. With sufficient number of sets of steady-state data, we can construct the bifurcation diagrams as required. Our computer program automatically organizes bifurcation diagrams from time-domain waveforms. The circuit parameters used in our simulations are shown in Table I.

A large number of bifurcation diagrams have been obtained. In the following, only representative bifurcation diagrams are shown, which serve to exemplify the main findings concerning the bifurcation behavior of a system of parallel buck converters under a master-slave sharing scheme.

A. Voltage Feedback Gains as Bifurcation Parameters

We first keep K_{v2} constant and vary K_{v1} . The bifurcation diagram, as shown in Fig. 4, shows repeated period-doublings to chaos. Next, we

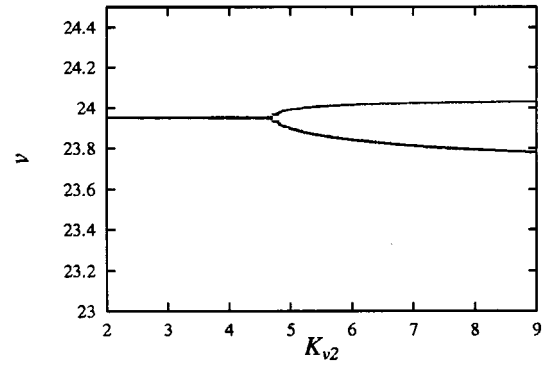


Fig. 5. Bifurcation diagram with K_{v2} as bifurcation parameter ($K_{v1} = 4$, $K_i = 5$ and $m = 1$), first period-doubling occurs when $K_{v2} = 4.85$.

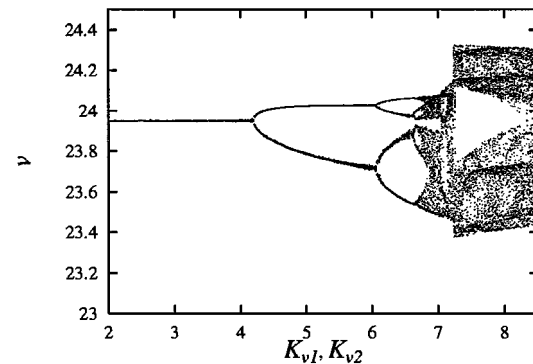


Fig. 6. Bifurcation diagram with K_{v1} and K_{v2} as bifurcation parameters varying simultaneously ($K_i = 5$, $m = 1$).

keep K_{v1} constant and vary K_{v2} . The bifurcation diagram, as shown in Fig. 5, again manifests a period-doubling bifurcation. Finally, we vary K_{v1} and K_{v2} simultaneously, and the corresponding bifurcation diagram is shown in Fig. 6. Again, period-doubling bifurcations are observed.

Remarks: The occurrence of period-doubling bifurcations generally agrees with previous findings for the buck converter. Intuitively speaking, if the two converters were identical, the system would reduce to a buck converter feeding a load. Thus, we may expect period-doubling to occur in the parallel system when the voltage feedback gain is varied, as it would occur likewise in a buck converter [7], [10]. We will present detailed analysis in Section V.

B. Current Gain as Bifurcation Parameter

In studying the bifurcation behavior in respect of current gain variation, we keep m , K_{v1} and K_{v2} constant, and vary K_i . It is found that the system remains in stable period-1 operation irrespective of the choice of K_i . Basically K_i only determines how close the slave follows the master. The larger K_i is, the closer the slave's output current is to the master's.

C. Current-Sharing Ratio as Bifurcation Parameter

Our final computer investigation is performed for variation of the current sharing ratio m . This time, we fix K_{v1} , K_{v2} and K_i at suitable values such that the system is in stable operation. We vary m and collect bifurcation diagrams which look typically like the one shown in Fig. 7.

In this type of bifurcation, the stable operation suddenly gives way to chaos. The origin of such a bifurcation is the nonsmooth operation

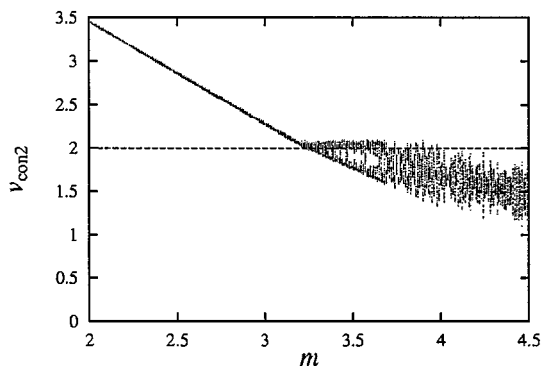


Fig. 7. Bifurcation diagram with current sharing ratio m as bifurcation parameter ($K_{v1} = 3.5$, $K_{v2} = 3.5$, $K_i = 5$).

of the system near the bifurcation point, which has been studied extensively by Nusse, Ott and Yorke [13] who coined such bifurcation as *border collision* bifurcation, and also by Banerjee *et al.* [11], [14]. To probe further into this bifurcation, we examine the time-domain waveforms of the control voltages v_{con1} and v_{con2} and see how they cross the ramp in the process of generating the PWM signals.

In normal operation, v_{con1} and v_{con2} hit the ramp once per switching cycle as shown in Fig. 8(a), and the corresponding inductor waveforms are shown in Fig. 8(b). Now, if we increase m and take a close look at the waveform, we observe the following qualitative change near the point of border collision bifurcation.

- Before border collision—When v_{con2} is slightly larger than V_L , normal operation is maintained, as shown in Fig. 9(a).
- After border collision—When v_{con2} falls below V_L , it fails to hit the ramp. Stable operation is lost and the system bifurcates to chaos. Fig. 9(b) shows the waveform just after the bifurcation.

The above bifurcation, which has not been observed previously for parallel converter systems, indicates that stable operation of such systems require keeping m below a certain value. In Section VI, we will analyze the condition under which this bifurcation occurs.

V. ANALYSIS OF PERIOD-DOUBLING BIFURCATION

From the foregoing simulation study, we have identified period-doubling bifurcation in a system of parallel buck converters when the voltage feedback gains are varied. We have also seen how stability suddenly gives way to chaos when the current sharing ratio is increased. In this and the next sections we analyze these bifurcations in terms of a suitable discrete-time model [12]. We will first derive the model, and examine the Jacobian matrix and the way the system loses stability.

A. Derivation of the Discrete-Time Map

Our purpose in this subsection is to derive a discrete-time map that describes the dynamics of a system of two buck converters connected in parallel, as defined earlier in Section III (see Fig. 3), in the neighborhood of the T -periodic steady state. We let x be the state variables as defined previously, and further let d_1 and d_2 be the duty cycle of Converter 1 (master) and Converter 2 (slave), respectively. The discrete-time map that we aim to find takes the following form:

$$x_{n+1} = f(x_n, d_{1,n}, d_{2,n}) \quad (8)$$

where subscript n denotes the value at the beginning of the n th cycle, i.e., $x_n = x(nT)$. For the closed-loop system, we need also to find the feedback equations that relate $d_{1,n}$ and $d_{2,n}$ to x_n .

The state equations are given in (4) for different switch states. The order in which the system toggles between the switch states depends on d_1 and d_2 . We will study periodic orbits for which $d_{2,n} > d_{1,n}$ for all n as this allows a convenient derivation of the discrete-time model. In particular, the assumption $d_2 > d_1$ is consistent with our simulation study since r_{L1} has a lower value than r_{L2} . Note that such an assumption loses no generality.

Recall that if $d_2 > d_1$, the state “ S_1 on and S_2 off” should be omitted. Hence, we have three switch states. These are as follows.

- 1) For $nT < t \leq nT + d_{1,n}T$, both S_1 and S_2 are turned on.
- 2) For $nT + d_{1,n}T < t \leq nT + d_{2,n}T$, S_1 is turned off and S_2 remains on.
- 3) For $nT + d_{2,n}T < t \leq (n+1)T$, both S_1 and S_2 are off.

In each switch state, the describing state equation is $\dot{x} = A_j x + B_j E$, where $j = 1, 3, 4$. (Note that $j = 2$ does not appear here.) For each state equation, we can derive the solution, and by stacking up the solutions, x_{n+1} can be expressed in terms of x_n , $d_{1,n}$ and $d_{2,n}$, i.e.,

$$\begin{aligned} x_{n+1} = & \Phi_4((1-d_{2,n})T)\Phi_3((d_{2,n}-d_{1,n})T)\Phi_1(d_{1,n}T)x_n \\ & + \Phi_4((1-d_{2,n})T)\Phi_3((d_{2,n}-d_{1,n})T) \\ & \cdot (\Phi_1(d_{1,n}T) - \mathbf{1})A_1^{-1}B_1E + \Phi_4((1-d_{2,n})T) \\ & \cdot (\Phi_3((d_{2,n}-d_{1,n})T) - \mathbf{1})A_3^{-1}B_3E \\ & + (\Phi_4((1-d_{2,n})T) - \mathbf{1})A_4^{-1}B_4E \end{aligned} \quad (9)$$

where $\mathbf{1}$ is the unit matrix, and $\Phi_j(\xi)$ is the transition matrix corresponding to A_j and is given by

$$\Phi_j(\xi) = e^{A_j \xi} = \mathbf{1} + \sum_{k=1}^{\infty} \frac{1}{k!} A_j^k \xi^k, \quad \text{for } j = 1, 2, 3, 4. \quad (10)$$

For parallel-connected buck converters, we let $A = A_1 = A_2 = A_3 = A_4$ and $\Phi(\xi) = \Phi_1(\xi) = \Phi_2(\xi) = \Phi_3(\xi) = \Phi_4(\xi)$. Hence, (9) can be written as

$$\begin{aligned} x_{n+1} = & \Phi(T)x_n + \Phi(T)A^{-1}B_1E + \Phi((1-d_{1,n})T)A^{-1} \\ & \cdot (B_3 - B_1)E + \Phi((1-d_{2,n})T)A^{-1}(B_4 - B_3) \\ & \cdot E - A^{-1}B_4E. \end{aligned} \quad (11)$$

Our next step is to find the feedback relations that connect the duty cycles and the state variables. The control voltages v_{con1} and v_{con2} , as given before by (2) and (3), can be rewritten as

$$v_{con1} = U_1 + \kappa_1^T x \quad (12)$$

$$v_{con2} = U_2 + \kappa_2^T x \quad (13)$$

where U_1 and U_2 are constants, and the gain vectors κ_1 and κ_2 are

$$\kappa_1^T = [-K_{v1} \quad 0 \quad 0] \quad \text{and} \quad \kappa_2^T = [-K_{v2} \quad K_i m \quad -K_i]. \quad (14)$$

The ramp function can also be rewritten simply as

$$v_{ramp} = \alpha + \beta(t \bmod T) \quad (15)$$

where α and β are constants. To find the defining equations for the duty cycles, we first note that the switches are turned off when

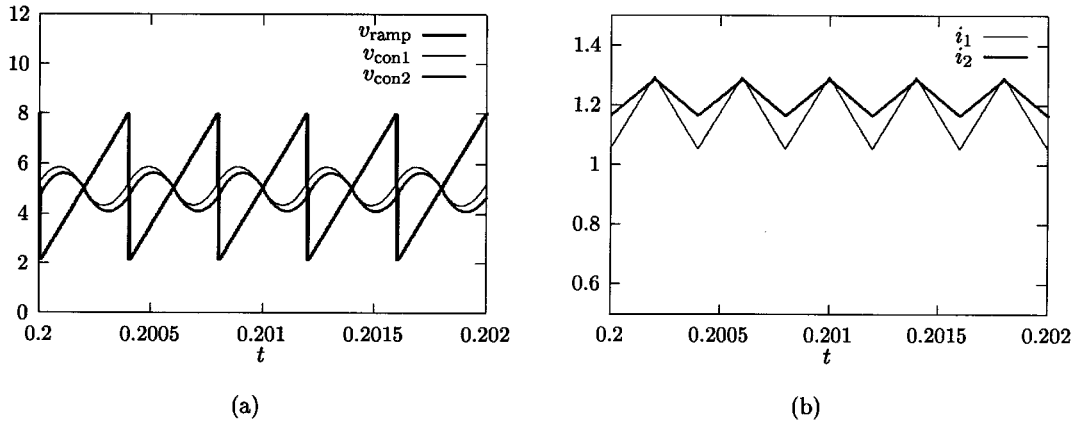
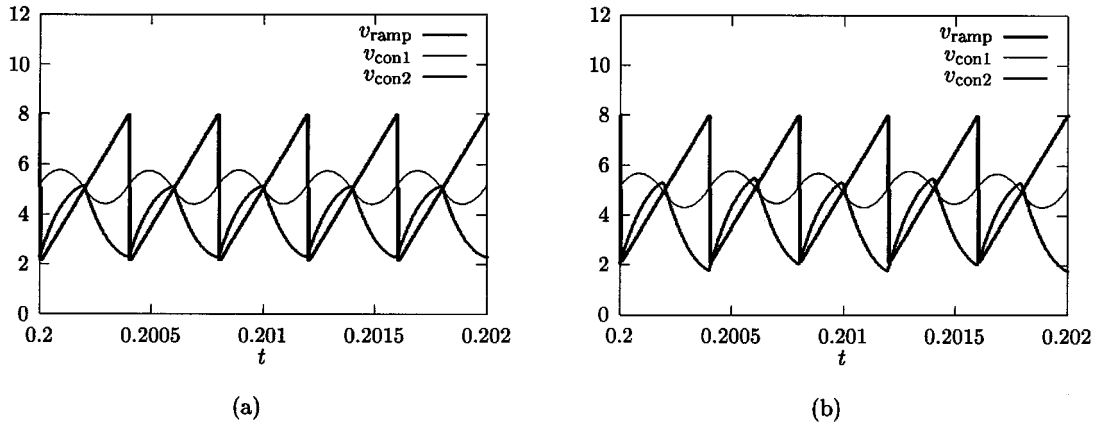


Fig. 8. Stable period-1 operation. (a) Control voltages and ramp; (b) inductor currents.


 Fig. 9. Control voltage waveforms (a) just before border collision bifurcation ($m = 3$); and (b) just after border collision bifurcation ($m = 3.5$).

$v_{con1} = v_{ramp}$ and $v_{con2} = v_{ramp}$. Now, define $s_1(x_n, d_{1,n})$ and $s_2(x_n, d_{1,n}, d_{2,n})$ as

$$\begin{aligned} s_1(x_n, d_{1,n}) & \stackrel{\text{def}}{=} v_{con1} - v_{ramp} \\ & = U_1 + \kappa_1^T x(d_{1,n}T) - (\alpha + \beta d_{1,n}T) \\ & = U_1 + \kappa_1^T [\Phi(d_{1,n}T)x_n + (\Phi(d_{1,n}T) - \mathbf{1})A^{-1}B_1E] \\ & \quad - (\alpha + \beta d_{1,n}T) \end{aligned} \quad (16)$$

$$\begin{aligned} s_2(x_n, d_{1,n}, d_{2,n}) & \stackrel{\text{def}}{=} v_{con2} - v_{ramp} \\ & = U_2 + \kappa_2^T x(d_{2,n}T) - (\alpha + \beta d_{2,n}T) \\ & = U_2 + \kappa_2^T [\Phi(d_{2,n}T)x_n + \Phi(d_{2,n}T)A^{-1}B_1E \\ & \quad + \Phi((d_{2,n} - d_{1,n})T)A^{-1}(B_3 - B_1)E \\ & \quad - A^{-1}B_3E] - (\alpha + \beta d_{2,n}T). \end{aligned} \quad (17)$$

Thus, S_1 and S_2 are turned off, respectively, when

$$s_1(x_n, d_{1,n}) = 0 \quad (18)$$

$$s_2(x_n, d_{1,n}, d_{2,n}) = 0. \quad (19)$$

Solving (18) and (19), $d_{1,n}$ and $d_{2,n}$ can be obtained. Combining with (11), we have the discrete-time iterative map for the closed-loop system.

B. Derivation of the Jacobian Matrix

The Jacobian matrix plays an important role in the study of dynamical systems [15]. The essence of using a Jacobian matrix in the analysis of dynamical systems lies in the capture of the dynamics in the small neighborhood of an equilibrium point or orbit (stable or unstable). We will make use of this conventional method to examine the bifurcation phenomena in Section V-C. But before we move on, we need to find the necessary expressions that enable the Jacobian matrix to be computed.

Suppose the equilibrium point is given by $x(nT) = X_Q$. The Jacobian of the discrete time map evaluated at the equilibrium point can be written as follows:

$$\begin{aligned} J(X_Q) & = \frac{\partial f}{\partial x_n} - \frac{\partial f}{\partial d_{1,n}} \left(\frac{\partial s_1}{\partial d_{1,n}} \right)^{-1} \\ & \quad \cdot \left(\frac{\partial s_1}{\partial x_n} \right) - \frac{\partial f}{\partial d_{2,n}} \left(\frac{\partial s_2}{\partial d_{2,n}} \right)^{-1} \\ & \quad \cdot \left[\left(\frac{\partial s_2}{\partial x_n} \right) + \frac{\partial s_2}{\partial d_{1,n}} \left(\frac{\partial s_1}{\partial d_{1,n}} \right)^{-1} \left(\frac{\partial s_1}{\partial x_n} \right) \right] \Bigg|_{x_n=X_Q} \end{aligned} \quad (20)$$

where

$$\frac{\partial f}{\partial x_n} = \begin{bmatrix} \frac{\partial f_1}{\partial v_n} & \frac{\partial f_1}{\partial i_{1,n}} & \frac{\partial f_1}{\partial i_{2,n}} \\ \frac{\partial f_2}{\partial v_n} & \frac{\partial f_2}{\partial i_{1,n}} & \frac{\partial f_2}{\partial i_{2,n}} \\ \frac{\partial f_3}{\partial v_n} & \frac{\partial f_3}{\partial i_{1,n}} & \frac{\partial f_3}{\partial i_{2,n}} \end{bmatrix} \quad (21)$$

$$\frac{\partial f}{\partial d_{1,n}} = \begin{bmatrix} \frac{\partial f_1}{\partial d_{1,n}} & \frac{\partial f_2}{\partial d_{1,n}} & \frac{\partial f_3}{\partial d_{1,n}} \end{bmatrix}^T \quad (22)$$

$$\frac{\partial s_1}{\partial x_n} = \begin{bmatrix} \frac{\partial s_1}{\partial v_n} & \frac{\partial s_1}{\partial i_{1,n}} & \frac{\partial s_1}{\partial i_{2,n}} \end{bmatrix} \quad (23)$$

$$\frac{\partial f}{\partial d_{2,n}} = \begin{bmatrix} \frac{\partial f_1}{\partial d_{2,n}} & \frac{\partial f_2}{\partial d_{2,n}} & \frac{\partial f_3}{\partial d_{2,n}} \end{bmatrix}^T \quad (24)$$

$$\frac{\partial s_2}{\partial x_n} = \begin{bmatrix} \frac{\partial s_2}{\partial v_n} & \frac{\partial s_2}{\partial i_{1,n}} & \frac{\partial s_2}{\partial i_{2,n}} \end{bmatrix}. \quad (25)$$

Using (16), (17) and (11), we can find all the derivatives in (20). First, $\partial f/\partial x_n$ can be found from (11), i.e.,

$$\frac{\partial f}{\partial x_n} = \Phi(T). \quad (26)$$

Also, direct differentiation gives $\partial f/\partial d_{1,n}$ as

$$\frac{\partial f}{\partial d_{1,n}} = -T\Phi((1-d_{1,n})T)(B_3-B_1)E. \quad (27)$$

Likewise, we get $\partial f/\partial d_{2,n}$ as

$$\frac{\partial f}{\partial d_{2,n}} = -T\Phi((1-d_{2,n})T)(B_4-B_3)E. \quad (28)$$

From (16), we obtain $\partial s_1/\partial x_n$ readily as

$$\frac{\partial s_1}{\partial x_n} = \kappa_1^T \Phi(d_{1,n}T). \quad (29)$$

Again, by direct differentiation, we get

$$\begin{aligned} \frac{\partial s_1}{\partial d_{1,n}} &= \kappa_1^T \frac{\partial \Phi(d_{1,n}T)}{\partial d_{1,n}} x_n \\ &= \kappa_1^T (AT\Phi(d_{1,n}T))x_n + \kappa_1^T (\Phi(d_{1,n}T)B_1T)E - \beta T \\ &= T\kappa_1^T \Phi(d_{1,n}T)(Ax_n + B_1E) - \beta T \end{aligned} \quad (30)$$

and, from (17), we get

$$\frac{\partial s_2}{\partial x_n} = \kappa_2^T \Phi(d_{2,n}T). \quad (31)$$

Finally, we need to get $\partial s_2/\partial d_{2,n}$ and $\partial s_2/\partial d_{1,n}$. From (17) we have

$$\begin{aligned} \frac{\partial s_2}{\partial d_{2,n}} &= \kappa_2^T \frac{\partial \Phi(d_{2,n}T)}{\partial d_{2,n}} x_n + \kappa_2^T \frac{\partial \Phi(d_{2,n}T)A^{-1}B_1}{\partial d_{2,n}} E \\ &\quad + \kappa_2^T \frac{\partial \Phi((d_{2,n}-d_{1,n})T)A^{-1}(B_3-B_1)}{\partial d_{2,n}} E - \beta T \\ &= \kappa_2^T (AT\Phi(d_{2,n}T))x_n + \kappa_2^T (\Phi(d_{2,n}T)B_1T)E \\ &\quad + \kappa_2^T \Phi((d_{2,n}-d_{1,n})T)(B_3-B_1)TE - \beta T \\ &= T\kappa_2^T \Phi(d_{2,n}T)(Ax_n + B_1E) \\ &\quad + T\kappa_2^T \Phi((d_{2,n}-d_{1,n})T)(B_3-B_1)E - \beta T \end{aligned} \quad (32)$$

$$\begin{aligned} \frac{\partial s_2}{\partial d_{1,n}} &= \kappa_2^T \frac{\partial \Phi((d_{2,n}-d_{1,n})T)A^{-1}(B_3-B_1)E}{\partial d_{1,n}} \\ &= -T\kappa_2^T \Phi((d_{2,n}-d_{1,n})T)(B_3-B_1)E. \end{aligned} \quad (33)$$

Now, putting all the derivatives into (20) gives (34) as shown at the bottom of the next page. Numerical algorithms can now be developed for computing $J(X_Q)$ and hence the characteristic multipliers, as will be shown in the next subsection.

C. Characteristic Multipliers and Period-Doubling Bifurcation

The Jacobian derived in the foregoing subsection provides a means to evaluate the dynamics of the system. We will, in particular, study the loci of the characteristic multipliers (also called eigenvalues), the aim being to find out possible bifurcation scenarios as the voltage feedback gains are varied. To find the characteristic multipliers, we solve the following polynomial equation in λ , whose roots actually give the characteristic multipliers

$$\det[\lambda \mathbf{1} - J(X_Q)] = 0 \quad (35)$$

where $J(X_Q)$ is the Jacobian matrix found previously. We will pay attention to the movement of the characteristic multipliers as K_{v1} and K_{v2} are varied. Any crossing from the interior of the unit circle to the exterior indicates a bifurcation. In particular, if a real characteristic multiplier goes through -1 as it moves out of the unit circle, a period-doubling occurs.

Using (34), we can generate loci of characteristic multipliers numerically. Since we are interested here in varying K_{v1} and K_{v2} , we keep $m = 1$, thereby ensuring that the system is remote from any border collision due possibly to large m , as we have seen previously in the simulation. The parameter values of the system are the same in Tables I and II and in Figs. 4 and 5. To maintain conciseness, we exemplify here the typical loci in Tables II and III, which are graphically illustrated in Figs. 10 and 11. Both loci indicate a period-doubling bifurcation as K_{v1} and K_{v2} vary. This agrees with our simulation results in Section IV.

VI. ANALYSIS OF BORDER COLLISION BIFURCATION WITH RESPECT TO VARIATION OF CURRENT-SHARING RATIO

As observed in the simulation, a border collision bifurcation occurs when m increases beyond a certain limit. In this section, we attempt to analyze this border collision and specifically to find the limit of m below which the system maintains stable operation. In the following study, we assume that K_{v1} and K_{v2} are kept within the stable range so that the system is remote from any period-doubling bifurcation due possibly to large K_{v1} and K_{v2} .

TABLE II
 CHARACTERISTIC MULTIPLIERS FOR DIFFERENT VALUES OF K_{v1}

K_{v1}	Char. Mult.	Remarks
3.00	$-0.542 \pm j0.363, 0.998$	Stable 1T
3.50	$-0.608 \pm j0.236, 0.998$	Stable 1T
3.80	$-0.643 \pm j0.106, 0.998$	Stable 1T
3.85	$-0.649, -0.649, 0.998$	Stable 1T
4.00	$-0.801, -0.531, 0.998$	Stable 1T
4.20	$-0.903, -0.471, 0.998$	Stable 1T
4.40	$-0.981, -0.433, 0.998$	Stable 1T
4.47	$-1.000, -0.425, 0.998$	Period-doubling

 TABLE III
 CHARACTERISTIC MULTIPLIERS FOR DIFFERENT VALUES OF K_{v2}

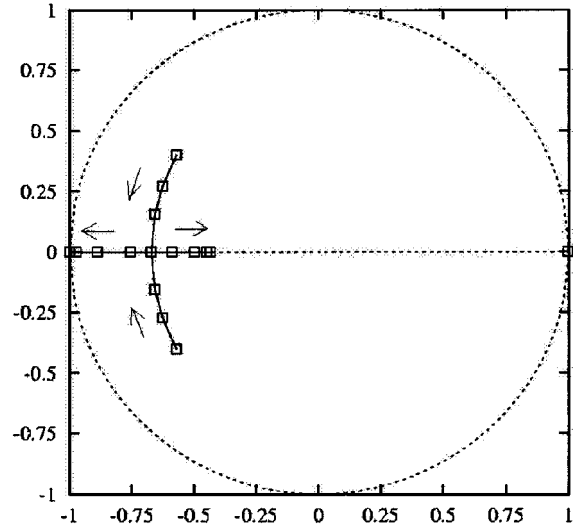
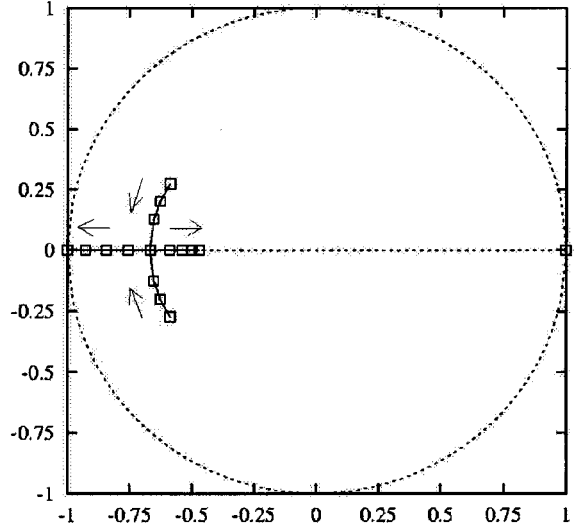
K_{v2}	Char. Mult.	Remarks
3.00	$-0.604 \pm j0.246, 0.998$	Stable 1T
3.40	$-0.631 \pm j0.166, 0.998$	Stable 1T
3.60	$-0.643 \pm j0.109, 0.998$	Stable 1T
3.70	$-0.649, -0.649, 0.998$	Stable 1T
4.00	$-0.801, -0.531, 0.998$	Stable 1T
4.20	$-0.856, -0.497, 0.998$	Stable 1T
4.50	$-0.921, -0.461, 0.998$	Stable 1T
4.85	$-1.000, -0.426, 0.998$	Period-doubling

Inspection of the locus of the characteristic multipliers reveals that a sudden “jump” occurs as m increases, which is typical of border collision bifurcation [11], [13]. Such a bifurcation arises when v_{con1} or v_{con2} begins to pass over or under the ramp without hitting it during the whole switching period. This situation is illustrated in Fig. 12. As m increases, the system traverses from one situation where v_{con1} and v_{con2} both hit the ramp, to another where v_{con1} or v_{con2} misses the ramp. Such a transition is *nonsmooth* at the point where v_{con1} or v_{con2} just misses the ramp, and at this point, border collision bifurcation occurs.

By studying the expressions of v_{con1} , v_{con2} and v_{ramp} , we can estimate the critical value of m , at which border collision takes place. Ignoring the ripple, we have $v \approx V_{ref}$ in the steady state. Thus, (2) and (3) can be approximated by

$$v_{con1}(t) \approx V_{offset} \quad (36)$$

$$v_{con2}(t) \approx V_{offset} - K_i[i_2(t) - mi_1(t)]. \quad (37)$$


 Fig. 10. Locus of characteristic multipliers as K_{v1} varies. Arrows indicate increasing K_{v1} .

 Fig. 11. Locus of characteristic multipliers as K_{v2} varies. Arrows indicate increasing K_{v2} .

Since V_{offset} is always set between V_L and V_U , v_{con1} will always hit the ramp during a switching cycle. We therefore need only to focus on $v_{con2}(nT)$. As mentioned before, we assume that $d_2 > d_1$ in the neighborhood of T periodic state. Also, neglecting the middle period $(d_{2,n} - d_{1,n})T$ in the T periodic state and assuming

$$\begin{aligned}
 J(X_Q) = \Phi(T) - & \frac{-\Phi((1-d_{1,n})T)(B_3-B_1)E\kappa_1^T\Phi(d_{1,n}T)}{\kappa_1^T\Phi(d_{1,n}T)(Ax_n+B_1E)-\beta} \\
 & - \frac{\Phi((1-d_{2,n})T)(B_4-B_3)E \left[\kappa_2^T\Phi(d_{2,n}T) + \frac{-\kappa_2^T\Phi((d_{2,n}-d_{1,n})T)(B_3-B_1)E\kappa_1^T\Phi(d_{1,n}T)}{\kappa_1^T\Phi(d_{1,n}T)(Ax_n+B_1E)-\beta} \right]}{\kappa_2^T\Phi(d_{2,n}T)(Ax_n+B_1E) + \kappa_2^T\Phi((d_{2,n}-d_{1,n})T)(B_3-B_1)E - \beta}
 \end{aligned} \quad (34)$$

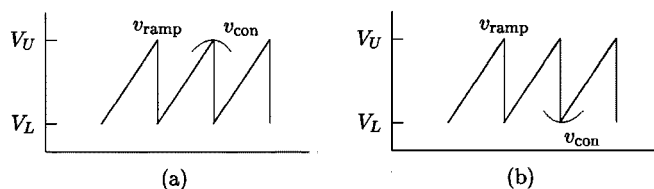


Fig. 12. The two possible border collision scenarios.

$i_2(d_{1,n}T) \approx mi_1(d_{1,n}T)$, and neglecting equivalent-series resistance (ESR) of inductors, we may express $i_1(nT)$ and $i_2(nT)$ as

$$i_1(nT) = i_1(d_{1,n}T) - \frac{v}{L_1}(1 - d_{1,n})T \quad (38)$$

$$i_2(nT) = i_2(d_{1,n}T) - \frac{v}{L_2}(1 - d_{1,n})T. \quad (39)$$

Putting (38) and (39) in (37), we get

$$v_{\text{con}2}(nT) = V_{\text{offset}} - K_i v(1 - d_{1,n})T \left(\frac{m}{L_1} - \frac{1}{L_2} \right). \quad (40)$$

Now, we may substitute either $v_{\text{con}2}(nT) = V_L$ or $v_{\text{con}2}(nT) = V_U$ in (40) to obtain the critical value of m . In particular, putting $v_{\text{con}2}(nT) = V_L$ in (40) gives

$$m_{\text{crit}} = \left(\frac{V_{\text{offset}} - V_L}{K_i v(1 - d_{1,n})T} + \frac{1}{L_2} \right) L_1 \quad (41)$$

where m_{crit} is the critical value of m at which $v_{\text{con}2}$ just hits V_L at $t = nT$. Furthermore, $v_{\text{con}2}(nT) = V_U$ gives a negative value for m , which is not possible, thus ruling out the possibility of a border collision with $v_{\text{con}2}$ hitting V_U .

Using the same set of parameter values and voltages as in Section IV-C, we find that $m_{\text{crit}} = 3.0$ which agrees very well with the bifurcation diagram shown in Fig. 7.

The above result clearly illustrates that the current-sharing ratio m in a master-slave controlled parallel converter system must be kept below a certain value in order to ensure stable operation.

VII. CONCLUSION

Despite the popularity of parallel converter systems in power electronics applications, their bifurcation phenomena are rarely studied. This paper reports some selected bifurcation phenomena in a parallel system of two buck converters which share current under a master-slave control scheme. The study of stability is a complex issue in this type of system [2], [3]. This paper focuses on the effects of variation of some voltage feedback gains and current sharing ratio. It has been found that period-doubling bifurcations are possible when voltage feedback gains are varied, and that a border collision bifurcation is also possible when the current-sharing ratio is varied. These results are useful for practical design of parallel converter systems to ensure stable period-one operation in the expected stable region.

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