Ferroelectric-driven performance enhancement of graphene field-effect transistor based on vertical tunnelling heterostructures

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The shrinking of the geometrical dimensions of current semiconductor devices has required the adoption of new materials and new device geometries.[1-4] Graphene-based field-effect transistor (GFET) has been among the breakthrough results of nanoscale electronic devices in the last decade. The first prototype GFET made by integrating graphene with silicon was reported by Novoselov *et al.*[5]. However, a fundamental problem of GFET is that the device remains conducting even when switched off, ascribed to the absence of an energy gap in graphene. Hence, an obstacle to application for all types of developed planar GFETs is their quite low current on/off ratio.[6,7] Recently, Manchester's group proposed a new conceptual GFET, namely vertical graphene heterostructure FET (VGHFET).[8] The room-temperature I_{on}/I_{off} ratio of the VGHFETs can reach ~50 or close to 10^4 with a tunnel barrier of hBN or MoS_2, respectively. In this architecture, electrons are capable of tunnelling from one layer of graphene to another through the atomically thin barrier layer. Such a groundbreaking work has fueled the research on searching various types of architectures, either vertical structure[9-16] or hybrid planar and vertical structures with Schottky barrier,[17-19] leading to the continuous improvement in GFET performance in the past few years. To date, the highest record of current on/off ratio is about 10^6 in all types of GFET,[9,15] and further improvement of device performance is highly desirable for practical application.

Here we propose a VGHFET using ultrathin ferroelectric film as a tunnel barrier. This work is inspired by another field of ferroelectric tunnel junction (FTJ)[20] and interfacing carbon device materials with ferroelectrics for novel electronic applications.[21-23] It is known that a tunnel junction is basically composed of a nanometer-thick barrier layer sandwiched by two electrodes. Differing from conventional tunnel junctions, the tunnelling barrier height in FTJ can be modulated by spontaneous polarization according to the theoretical predication.[24] Maksymovych *et al*. provided an experimental evidence to present a highly reproducible control of local electron transport through an ultrathin film of ferroelectric oxide, and the

tunnelling current shows amplification upon ferroelectric switching.[25] This mechanism has led to an electrical switching of tunnelling resistance, experimentally further verified by Garcia *et al*. and other groups.[26-30] Unfortunately, there has been no attempt to couple FTJ to GFET and therefore it is unknown to what new functionality can bring to the transistor. In this work, we have developed a novel FET with the complementary heterostructure possessing the features of both FTJ and VGHFET where conventional tunnel barrier of insulator or semiconductor is replaced with ultrathin ferroelectric film. This idea is implemented in the FET based on a multilayer structure composed of Au/BFO/graphene on an oxidized Si wafer in this work. The BFO was selected for the ferroelectric barrier due to its small energy bandgap and good polarization. Most importantly, through ferroelectric switching from the BFO ultrathin film, we firstly realize ultrahigh current on/off ratio of the FET, which is superior to those related devices, including all types of GFETs and FTJs ever reported so far. Such a tunnel device also inherently provides an opportunity to overcome the intrinsic limit of subthreshold swing (SS) for conventional metal-oxide-semiconductor FET (MOSFET). Taking advantage of the significantly enhanced current on/off ratio with small SS, the gate modulation ability of GFETs will become stronger, and the power consumption will become lower.

Figure 1a presents schematic structure of our proposed FET based on vertical graphene-ferroelectric tunnelling heterostructure (VGFTH). For simplicity, we consider the tunnel barrier for electrons and suppose that the initial electronic potential barrier with no bias has rectangular shape. The key operation principle of the VGHFET is related to the changes in the density of states (DoS) and Fermi energy (E_F) level of graphene, as well as effective barrier height of the tunnel barrier adjacent to the bottom graphene layer (Gr_B) when varying gate voltage (V_g) between Si substrate and Gr_B. The use of graphene in the device is essential because this exploits low DoS of graphene, leading to large variation in E_F under a given change in V_g.[8] The sign of the Fermi level shift is determined by the polarity of V_g. For

comparison, the band diagram corresponding to the case of no V_g and drain voltage (V_d) across the barrier of ferroelectric (FE) between Au and Gr_B is shown in Figure 1b. As illustrated schematically in Figure 1c, a negative V_g shifts E_F in Gr_B downwards, resulting in an increase in the barrier height from $<l_0$ to $<l_{1+}$, which represents the OFF state of the FET and then the current in this state is notated as I_{off}. In this scenario, the electronic potential profile of FE mainly depends on the direction of ferroelectric polarization (P). When increasing V_d in excess of the coercive voltage (V_c) of FE, the asymmetry of the electronic potential profile of FE will be reversed upon P reversal,[20] which may cause a shift in the potential barrier height (Figure 1d). However, such a small variation is almost negligible to the overall barrier height as the original barrier height ($<l_{1+}$) is large enough and therefore I_{off} remains little change after P switching. In contrast with the OFF state, a positive V_g shifts E_F upwards, resulting in a reduction in the barrier height from $<l_0$ to $<l_{2+}$, which represents the ON state of the FET and the current in this state is notated as I_{on} (Figure 1e). Importantly, the unique principle of our proposed VGFTH-based FET relies on the tunability of FE in the FTJ side ($Au/FE/Gr_B$)[20] as well apart from the gate control used in conventional VGHFET. When increasing V_d in excess of V_c under forward bias of V_g, P switching will occur (Figure 1f), attributed to the domain behaviour in FE (Figure 1g). In this case, the overall barrier height can be further decreased by extra $L'<l_B$ defined as the difference in the barrier height before and after P switching. Since the original barrier height of $<l_{2+}$ before P switching is quite low in Figure 1e, such an additional reduction of $L'<l_B$ will make an appreciable effect on the overall barrier height, leading to a great enhancement in I_{on}. Consequently, the action of FTJ complementing to conventional VGHFET in the proposed VGFTH-based FET is capable of giving rise to a remarkable I_{on}/I_{off} ratio and significant improvement in GFET performance in principle. Moreover, compared to conventional GFETs, the novel heterostructure device may possess more features from the graphene/FE layered structure.

Figure 2a shows schematic diagrams of our VGFTH-based FET. The detailed fabrication process of the proof-of-concept FET is illustrated in Supplementary Figure S1. Compared to the previously reported VGHFETs with exfoliated flake barriers,[8-10] it should be pointed out that multi-device layout as shown in Figure 2b might be more readily implemented when considering the use of thin-film barrier by physical vapour deposition compatible with state-of-art microfabrication technology. Hence, our work shows the potential of making GFET-based logic circuits on the wafer scale. The Raman characteristics of graphene transferred onto SiO_2/Si substrate before and after growing BFO film are shown in Figure 2c. The intensity is observed to be approximately twice as high for the 2D peak at 2700 cm^{-1} as for the G peak at 1580 cm^{-1}. The full-width half-maximum of 2D peak is less than 30 cm^{-1}. A D defect peak was seen from the graphene after depositing BFO, probably arisen from highly energetic growth process of pulsed laser deposited (PLD). The Raman spectra indicate that the graphene is still monolayer after BFO deposition. In order to ensure that the quality of graphene is maintained after BFO deposition, the mobility of graphene after BFO deposition was measured (Supplementary Figure S2), which was found to be only slightly decreased compared to that of graphene before growing BFO. The results suggest that the graphene after BFO deposition can satisfy the need of further device application in this work. Supplementary Figure S3 also illustrates atomic force microscopy (AFM) image of the polycrystalline BFO film deposited on graphene.

Figure 3a and 3b show the output and transfer characteristics of the fabricated VGFTH-based FET with Au/BFO(10 nm)/monolayer graphene/SiO_2(300 nm)/Si structure, respectively. We found that the direction of the measured current is along with the bias voltage across drain and source. In order to illustrate the positive value of the drain current used for view in the graphs, the drain voltage of V_d is shown here as the same direction of the carrier drift current between source and drain. In Figure 3a, the asymmetric curves of drain current (I_d) as a function of V_d are evident for the V_g ranging from -30 V to 30 V. As expected from the above

operation principle, the variation of I_d is as a result of the changes in tunnel barrier height modulated by V_g (Figure 3b). It is noted that the VGFTH-based FET has an obvious gate modulation under negative V_g, while the FET yields negligible gate modulation under positive V_g. According to the highly asymmetric behaviours, we could conclude that the carrier type of tunnelling is hole. Similar to the first VGHFET, such an observation may be due to the mechanism that the barrier height is lower for holes than for electrons.[8] Another reason responsible for the asymmetry of the charge transport might be associated with p-type graphene. It is common for graphene to show p-type behaviour in an ambient condition due to the presence of water adsorbates.[7] The band diagram of graphene-BFO is presented in Figure 3c, and the detailed description of band alignment can be seen in the Supplementary text after Figure S3. Compared to the reported VGHFET using conventional insulator barrier with large bandgap,[8] the new architecture using the BFO barrier layer with small bandgap of $E_g = 2.2$ eV shows an improved result as shown in Figure 3b. In particular, when V_g was swept between -30 V and 30 V at $V_d = 1$ V, the FET yields a switching ratio of about 10^6 from the transfer characteristic (I_d-V_g) of the device. Notably, such a magnitude of I_{on}/I_{off} has already been comparable to the highest current switching ratio obtained in GFETs.[9,15] The log (I_d) versus V_g plot is presented in the inset of Figure 3b for subsequent comparison. Consequently, the appropriate choice of tunnel barrier is mainly responsible for achieving the high I_{on}/I_{off} here.

As depicted in the proposed device principle (Figure 1), the upper structure of Au/BFO/Gr_B can be considered as a novel type of FTJ. To verify the hypothesis, the characteristic of I_d as a function of V_d was measured when V_g was set to 0 V. As shown in **Figure 4**a, an abrupt current jump is apparent at a positive V_d of about 3.8 V while little change is evident in the side of negative V_d. Piezoresponse force microscopy (PFM) is a tool to demonstrate the existence of a switchable ferroelectric polarization. Figure 4b shows the out-of-plane local hysteretic loops of PFM phase and amplitude recorded from our sample.

Note that the phase difference between the two polarization states is 180° and the minima in the amplitude loop coincides with the switching voltages in the phase signal, implying a ferroelectric nature of the BFO ultrathin barrier used in the device. Figure 4c shows the out-of-plane PFM phase image of BFO. The 180° phase contrast reveals that the polarization is anti-parallel in the two domains, indicating the existence of a switchable polarization in the tunnel barrier. The observed effects are highly reproducibly and stable, ruling out other possible origins involved, such as charging effect. More results for the out-of-plane PFM amplitude and phase images of BFO are shown in Supplementary Figure S4. It is noticeable that the bias voltage at the abrupt current jump as shown in Figure 4a is directly correlated to the coercive voltage (V_c), which is located within the range of ferroelectric polarization switching (Figure 4b). The obtained I_d-V_d profile exhibiting a hysteresis with abrupt switching is similar to the previously observed electron transport through ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$ ultrathin layer.[25] Hence, the large amplification of tunnelling current can be achieved via ferroelectric polarization switching. It is worth mentioning that the transport mechanism responsible for the observed phenomenon distinguishes other kinds of ferroelectric resistance switching, including switching diode typically using thick films.[31] Compared to the use of ultrathin barrier layer, the tunnelling hysteresis characteristic and abrupt current jump of the heterostructure with a thicker BFO (e.g., 30 nm) are not evident, further indicating the tunnelling transport mechanism in our device (Supplementary Figure S5). Very recently, Lu *et al.* reported to employ graphene as electrodes for FTJs composed of graphene/$BaTiO_3$/$(La,Sr)MnO_3$, allowing one to control the interface properties and then enhance the performance of FTJ with on/off ratio of 6000[29]. It is known that FTJ is the type of two-terminal device, while our work is based on three-terminal device combining both GFET and FTJ. When considering the aforementioned operation principle, the complementary heterostructure of our device is capable of offering more freedom to control the transport characteristics of the device, resulting in higher device's performance. As expected, we found

that the performance of the device was greatly enhanced by coupling the ferroelectric switching effect of the novel FTJ to the GFET. As shown in Figure 4d, it is evident that the current on/off ratio of the device increases by nearly two orders of magnitude up to about 7×10^7 compared to the result shown in Figure 3b, when varying bias V_d from 1 V to the voltage $V_d = 4$ V which is beyond V_c. As far as we know, such a remarkable current on/off ratio is the highest found in the literature references for all types of GFETs,[9,15] and also comparable to conventional Si-based FETs.[1] Apart from I_{on}/I_{off} ratio, the subthreshold swing SS = $dV_g/d(\log I_{ds})$ is another key performance parameter significant affecting the leakage power for FETs. From Figure 4d, the calculated SS of the device is estimated by fitting several data points, resulting in the value of 45 mV/decade. Note that the estimated SS value overcomes the intrinsic limit of 60 mV/decade for conventional metal-oxide-semiconductor FET (MOSFET). Such a low SS can be attributed to the tunnelling transport mechanism.[9] Interestingly, the current hysteresis loop of the FET was observed in Figure 4d, which might be originated from the charge trapping on ferroelectric surfaces.[7] It was reported that ferroelectric polarization stability and retention are strongly affected by charged atoms of molecular layer at the graphene/ferroelectric interface,[29] and hysteresis characteristic could be arisen from the screening of the polarization by traps between the graphene/ferroelectric interface. At any rate, the FET device presents two pronounced I_d states with the ratio of more than 20 at $V_g = 0$, showing the promise of non-volatile memory functionality.

As schematically illustrated in Figure 1, the performance enhancement of the device is mainly due to the tunability of barrier height by $\Lambda\chi I_B$ via polarization switching. In order to gain an in-depth understanding of the transport mechanism, we performed theoretical modelling and simulation studies on the novel heterostructure. $\Lambda\chi I_B$ can be expressed by $\Lambda\chi I_B \quad \frac{e_1}{\tau_1} \quad _s$,[25] where $_1$, $_1$ and $_s$ are the width of dielectric gap, dielectric constant and surface charge density, respectively. $\Lambda\chi I_B$ is calculated to be about 0.1 eV, and the reduction

in the barrier height is mainly responsible for the enhanced current on/off ratio. In order to shed light on the mechanism of transport through the barrier sandwiched by the two electrodes, the I_d-V_d curves at gate voltage $V_g = 0$ V was simulated based on Fowler-Nordheim (FN) tunnelling model.[25] Supplementary Figure S6 shows the comparison of experimental and simulation results. It suggests that our measured result can match the FN tunnelling model well, which coincides with the earlier comparison reports.[8,25] Therefore, this finding suggests that the mechanism of FN tunnelling through a triangular potential barrier provides a realistic explanation for understanding the observed carrier transport through BFO between graphene and Au.

In summary, an unexplored type of VGHFET with ultrathin ferroelectric film as a tunnel barrier has been developed. This is fundamentally different from the existing planar graphene-ferroelectric FETs.[7] With the unique ferroelectric switching resulting in large amplification of tunnelling current, we have demonstrated a highest room-temperature current on/off ratio of 7×10^7 ever reported for all types of GFETs. Moreover, the fabricated FETs with the complementary structures possess low SS of 45 mV/decade, wafer-scale barrier, non-volatile memory and tunable transport characteristics. The new family of atomic-scale heterostructures in this study will provide a platform with more degrees of freedom to investigate the underlying mechanisms of tunnelling phenomena. For instance, the heterostructure incorporated with multiferroic BFO in this work may allow the multiferroic control of transport to produce high performance nanoscale memory and spintronic devices with multi-mode and multi-level. Moreover, graphene-based vertical heterostructures exhibit great potential for ultra-broadband and high-speed optoelectronic device[32] and light emitting diodes.[33] Therefore, the studied heterostructure in this work is an appealing atomic-scale assembly which could be interestingly extended from FET electronics to optoelectronics. Consequently, our work opens up the possibility to create various multifunctional nanoscale devices by engineering ferroelectric tunnel layer with two-dimensional layer building blocks.

Experimental Section

The graphene films synthesized on copper foils by chemical vapor deposition (CVD) were transferred onto SiO_2/Si substrates using a standard wet transfer process. The ultrathin BFO films with the thickness of 10 nm were grown on the transferred graphene by PLD. The monolayer graphene transferred on SiO_2/Si substrate was characterized by Raman spectroscopy (Horiba, HR800) using a laser excitation source with the wavelength of 488 nm and the spot size of I μm. AFM (Bruker Multimode 8) was employed to determine the surface topography and the thickness of BFO film. The PFM tests were performed to measure local ferroelecctric hysteresis loops and acquire polarization images using a scanning probe microscope (Asylum Research MFP-3D). The *I-V* curves of the VGHFTH-based FETs were measured by a semiconductor analyzer (Agilent 4156C) at room temperature to characterize the transport characteristics of the FETs.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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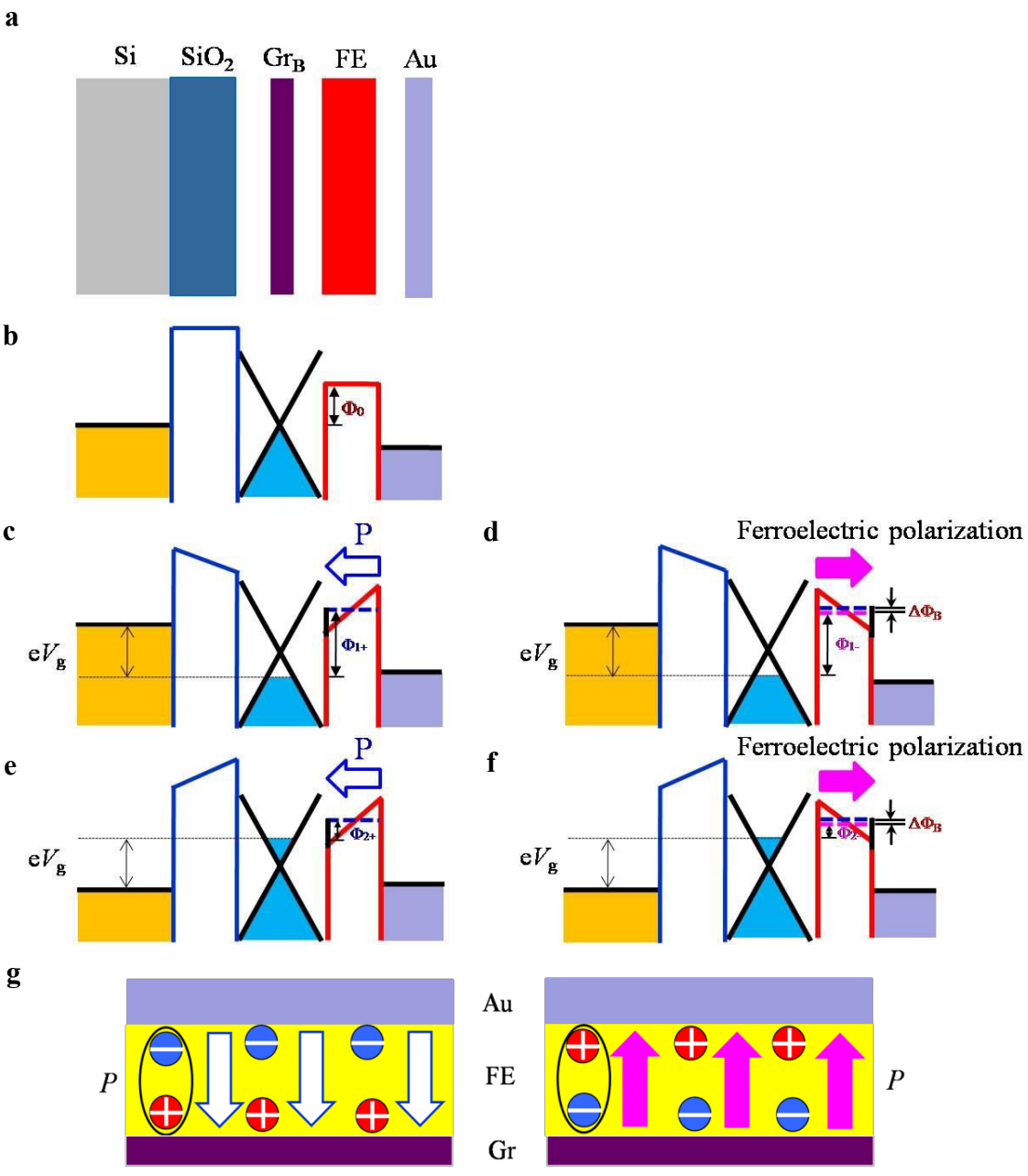

Figure 1. Schematic of energy band and operation principle of VGHFET with the tunnel barrier of ferroelectric (FE) and bottom graphene layer (Gr_B). For simplicity, the tunnel barrier for electrons is considered in the diagrams. (a) Schematic structure of device. (b) Energy band diagram when $V_g = 0$ and $V_d = 0$. (c) When $V_g < 0$ and $V_d < V_c$ (coercive voltage of FE), V_g shifts E_F in Gr_B downwards, resulting in an increase in effective barrier height, which represents the OFF state. (d) When $V_g < 0$ and $V_d > V_c$, the overall potential barrier is slightly shifted (blue line: before P switching; magenta line: after P switching), leading to little change I_{off} because of sufficiently large $<l_{1+}$. (e) When $V_g > 0$ and $V_d < V_c$, V_g shifts E_F upwards, resulting in a decrease in effective barrier height, which represents the ON state. (f) When $V_g > 0$ and $V_d > V_c$, the overall barrier is further decreased by $L' < l_B$ (blue line: before P switching; magenta line: after P switching), leading to a great enhancement in I_{on} because of quite small $<l_{2+}$. (g) Schematic illustration of domain behavior upon P switching.

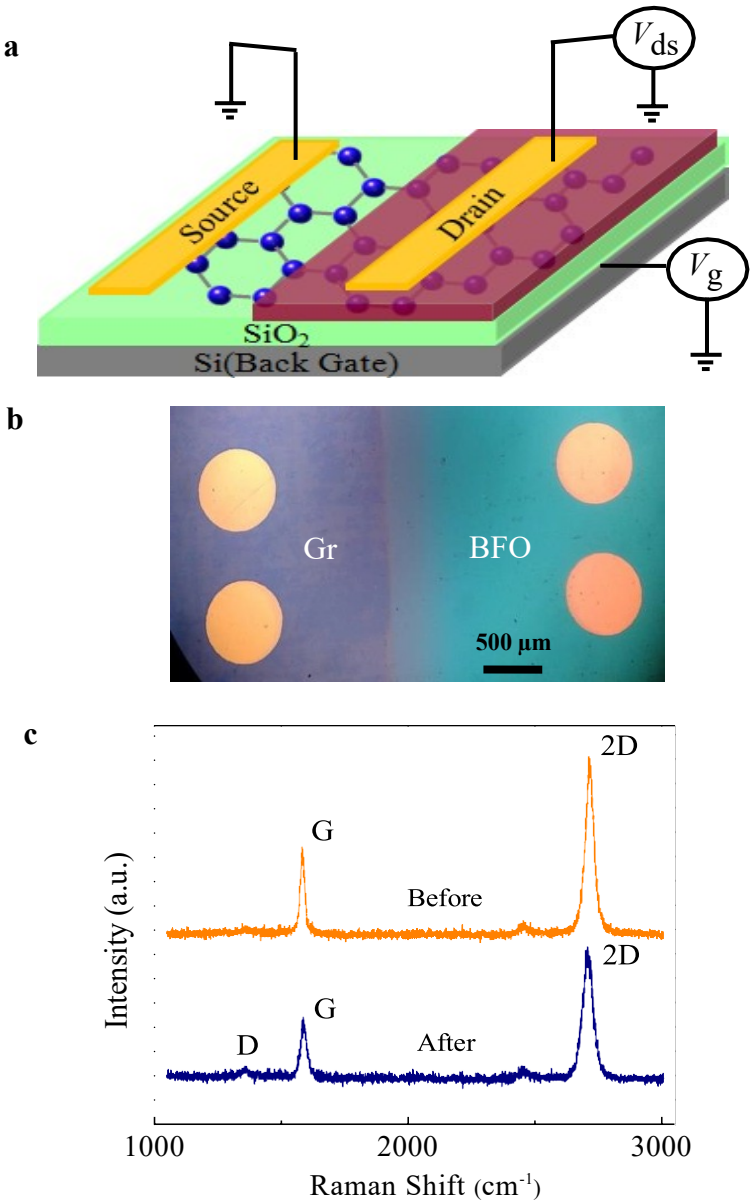

Figure 2. FET based on VGFTH heterostructure. (a) Schematic device structure of the FET based on a multilayer structure composed of Au/BFO/graphene on an oxidized Si wafer. (b) Optical micrograph of the fabricated device showing multi-device layout (top view). (c) Raman spectra of monolayer graphene transferred on SiO_2/Si substrate before (upper) and after (lower) ferroelectric BFO deposition.

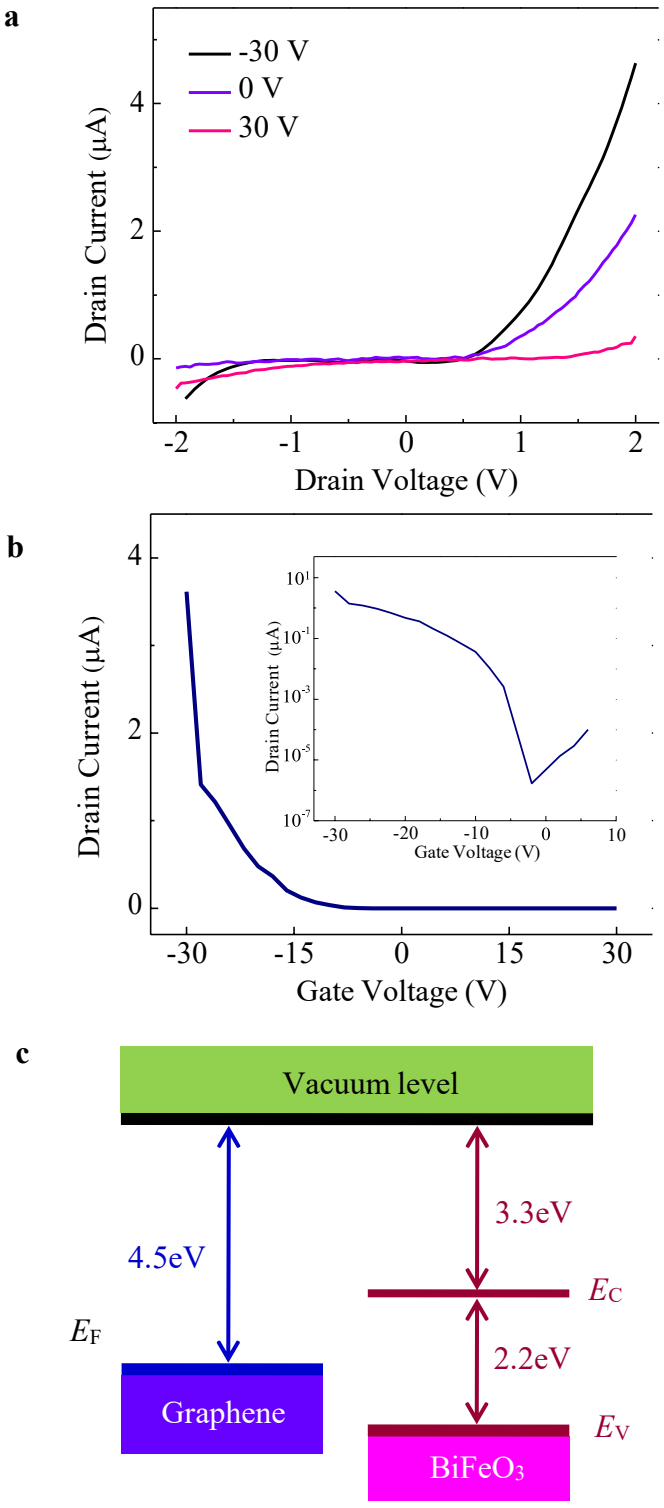

Figure 3. Transport characteristics of VGFTH-based FET. (a) I_d-V_d characteristics of the device for different V_g. (b) I_d-V_g characteristics of the device when the bias voltage across source and drain V_d = 1 V. The inset shows the plot in semi-logarithmic scale. (c) Energy band diagram of graphene-BFO.

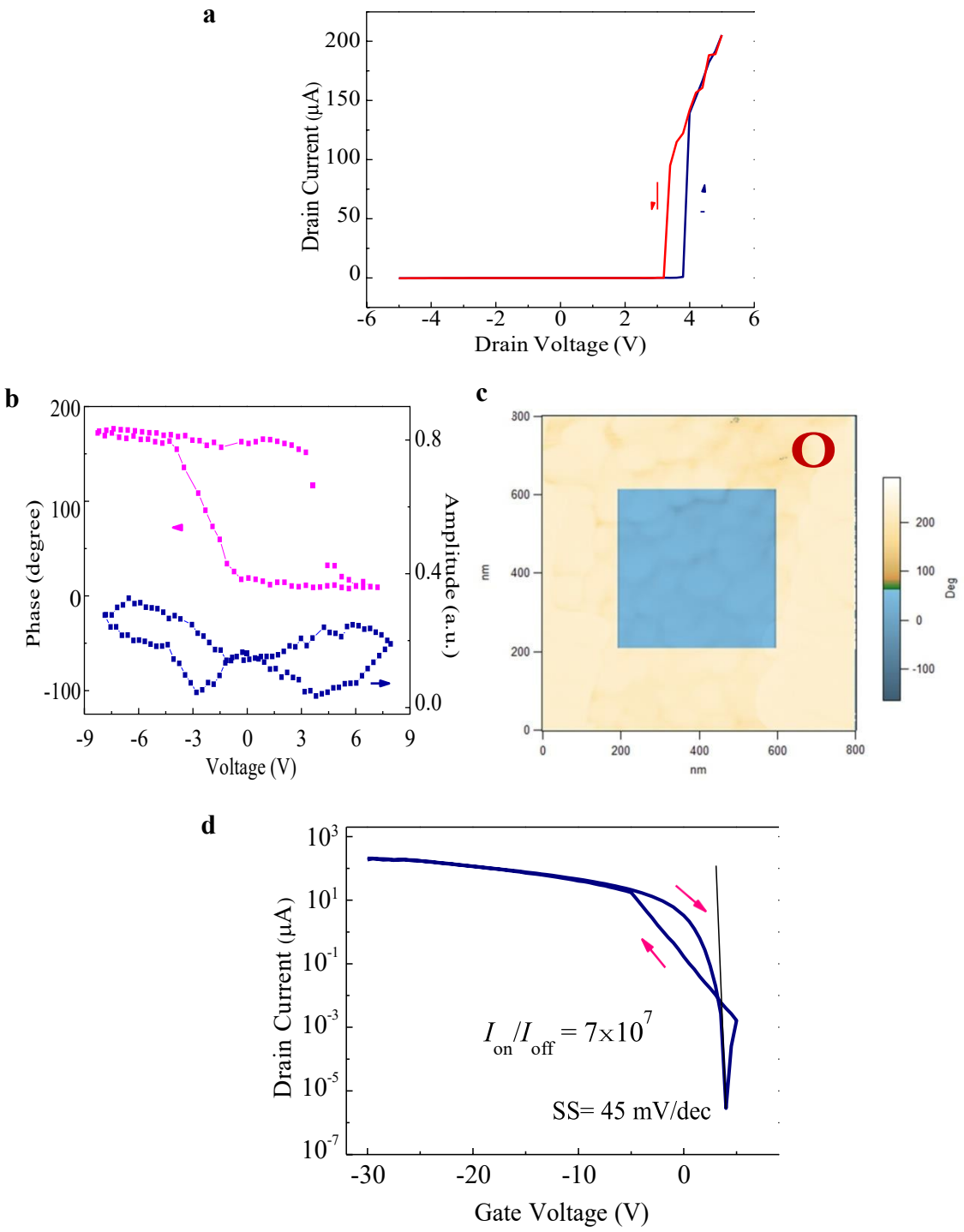

Figure 4. Transport characteristics of the VGFTH-based FET modulated by ferroelectric polarization. (a) I_d-V_d characteristic of the device when V_g = 0 V. (b) Local PFM phase (upper) and amplitude (lower) hysteresis loops of the ultrathin BFO film. (c) PFM out-of-plane phase image of the ultrathin BFO film, where the electrical poling was applied by writing an area with -10 V and then the central square with +10 V. (d) I_d-V_g characteristic of the achieved high performance device when V_d = 4 V.

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We develop vertical graphene heterostructure field-effect transistor (VGHFET) using ultrathin ferroelectric film as a tunnel barrier. The heterostructure is capable of providing new degrees of tunability and functionality via coupling between ferroelectricity and tunnel current of VGHFET, which results in high performance device. The results pave the way for developing novel atomic-scale two-dimensional heterostructures and devices.

Keyword: Graphene; Ferroelectric thin-films; Field-Effect Transistors; Two-dimensional materials; Pulsed laser deposition

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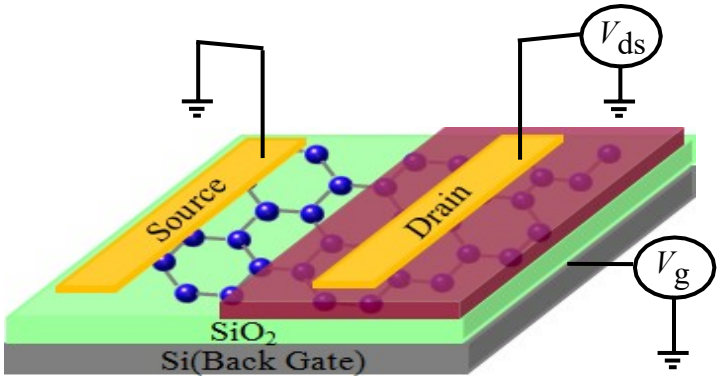
Ferroelectric-driven performance enhancement of graphene field-effect transistor based on vertical tunnelling heterostructures

ToC figure:



Supporting Information should be included here (for submission only; for publication, please provide Supporting Information as a separate PDF file).