Applied Physics Letters

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Cite as: Appl. Phys. Lett. **109**, 193504 (2016); https://doi.org/10.1063/1.4967186
Submitted: 22 May 2016 . Accepted: 13 October 2016 . Published Online: 08 November 2016

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Improved interfacial and electrical properties of HfLaON gate dielectric Ge MOS capacitor by NbON/Si dual passivation layer and fluorine incorporation

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(Received 22 May 2016; accepted 13 October 2016; published online 8 November 2016)

Ge metal-oxide-semiconductor (MOS) capacitor with HfLaON/(NbON/Si) stacked gate dielectric and fluorine-plasma treatment is fabricated, and its interfacial and electrical properties are compared with its counterparts without the Si passivation layer or the fluorine-plasma treatment. The experimental results show that the HfLaON/(NbON/Si) Ge MOS device treated by fluorine plasma exhibits excellent performance: low interface-state density (4.3×10^{11} cm^{-2} eV^{-1}), small flatband voltage (0.22 V), good capacitance-voltage behavior, small frequency dispersion and low gate leakage current (4.18×10^{-5} A/cm^2 at $V_g = V_{fb} + 1$ V). These should be attributed to the suppressed growth of unstable Ge oxides on the Ge surface during gate-dielectric annealing by the NbON/Si dual interlayer and fluorine incorporation, thus reducing the defective states at/near the NbSiON/Ge interface and improving the electrical properties of the device. *Published by AIP Publishing.*
[http://dx.doi.org/10.1063/1.4967186]

Ge-based MOSFET with high-k (dielectric constant) gate dielectric is one of the attractive approaches that has been widely studied due to its higher electron and hole mobilities than its Si counterpart[1,2] and easier integration of Ge on Si than III–V semiconductors on Si. However, the development of Ge MOSFET has been hampered due to the absence of a good thermally-grown oxide on the Ge substrate. In order to overcome the drawback of the unstable and volatile Ge native oxide, a high-quality interface between high-k dielectric and Ge is needed to establish the Ge metal-oxide-semiconductor (MOS) technology.[3] So, different surface passivation layers such as GeO_2,[4–6] GeON,[7] Al_2O_3,[8] AlON,[9] and $Ga_2O_3(Gd_2O_3)$[10] have been investigated, by means of which the interface properties between the high-k dielectric and Ge substrate got improved by different extents. In addition, excellent electrical properties at the insulator/Ge interface could be achieved by thermal oxidation.[11,12] However, the unstable GeO_x at the Ge surface could not be sufficiently suppressed during the high-k deposition. So, it is necessary to employ a new method to suppress the GeO_x. Several monolayers of Si were deposited on a cleaned Ge substrate using remote plasma chemical vapor deposition (RP-CVD),[13,14] resulting in an improved gate-stack quality with an interface-state density (D_{it}) of $\sim 5 \times 10^{11}$ cm^{-2} eV^{-1}. Moreover, an RF-sputtered Si passivating layer has been demonstrated to provide excellent interface quality with GaAs[15,16] because the Si passivation layer could prevent the oxygen in high-k dielectric from diffusing to the GaAs substrate by consuming the oxygen. Based on the same mechanism, it is likely to obtain good high-k/Ge interface quality by depositing an Si passivation layer on the Ge substrate. However, depositing the Si passivation layer on Ge should meet the strict criteria.[17,18] To readily satisfy the requirements, a good way is to deposit another interlayer on the Si passivation layer to consume Si through chemical interaction. NbON can be considered as a good candidate because it is easy to form Nb-Si bonds and simultaneously NbON is an oxidation-resistant material to prevent the oxygen diffusion.[19,20] So, a Ge MOS device with NbON/Si as dual passivation interlayer and HfLaON[21] as high-k gate dielectric is proposed. Besides, fluorine incorporation was reported to be capable of passivating the oxygen vacancies in high-k materials,[22,23] the Ge MOS capacitor is also treated in a fluorine plasma, and its interfacial and electrical characteristics are compared with those of the samples without the Si passivation layer or fluorine-plasma treatment.

The Ge MOS capacitors were fabricated on n-type (100) Ge wafers with a resistivity of 0.02–0.10 Ω cm. The wafers were cleaned using ethanol, acetone and trichloroethylene, followed by dipping in diluted HF (1:50) for 30 s, and then rinsed in deionized water for several times to remove the native oxide. After N_2 drying, the wafers were immediately transferred to the vacuum chamber of a Denton Vacuum Discovery Deposition System. A thin Si film (~1 nm) was deposited by sputtering Si target at room temperature in an Ar ambient, and then a thin NbN film (~2 nm) was deposited by sputtering Nb target at room temperature in an Ar/N_2 = 24/12 ambient, followed by the deposition of HfLaN gate dielectric (~5 nm) by sputtering an HfLa target in Ar/N_2 = 24/12. Next, a sample received a fluorine-plasma treatment in an ambient of CHF_3/O_2 = 10/1 for 5 min. For comparison, a sample with only NbON as interlayer and a control sample without both the Si and NbON interlayers (i.e., HfLaON was directly deposited on Ge) were prepared. So, the samples can be divided into four groups: the sample with NbON/Si dual passivation layer plus fluorine-plasma treatment (denoted as NbSiON + F), the sample with NbON/Si dual passivation layer but no fluorine-plasma treatment

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(denoted as NbSiON), the sample with only NbON interlayer (denoted as NbON) and the control sample without any passivation layer. Subsequently, post-deposition annealing (PDA) was carried out at 500 °C for 300 s in N_2 (500 sccm) + O_2 (50 sccm) to transform NbN/Si to NbSiON as passivation layer and HfLaN to HfLaON as gate dielectric. Finally, Al was thermally evaporated and patterned as gate electrode with an area of 7.85×10^{-5} cm^2, followed by a forming-gas (95% N_2 + 5% H_2) annealing at 300 °C for 20 min.

High-frequency (HF) capacitance-voltage (C-V) and gate leakage current-voltage ($J_g - V_g$) measurements were performed using HP4284A precision LCR meter and HP4156A semiconductor parameter analyzer, respectively. Physical thickness of the gate dielectrics was determined by the spectroscopic ellipsometry.

The TEM images of the NbSiON + F and NbSiON samples are shown in Fig. 1. As can be seen from Fig. 1(a), an NbSiON interlayer (2.1 nm) is formed between the Ge substrate and HfLaON gate dielectric (4.9 nm) with a clear NbSiON/Ge interface and a 7.0-nm total physical thickness for the stacked gate dielectric. However, for the NbSiON sample in Fig. 1(b), a thicker NbSiON interlayer (2.3 nm) is formed, and also the NbSiON/Ge interface is not too sharp. These indicate that the NbSiON + F sample has better interface quality than the NbSiON sample.

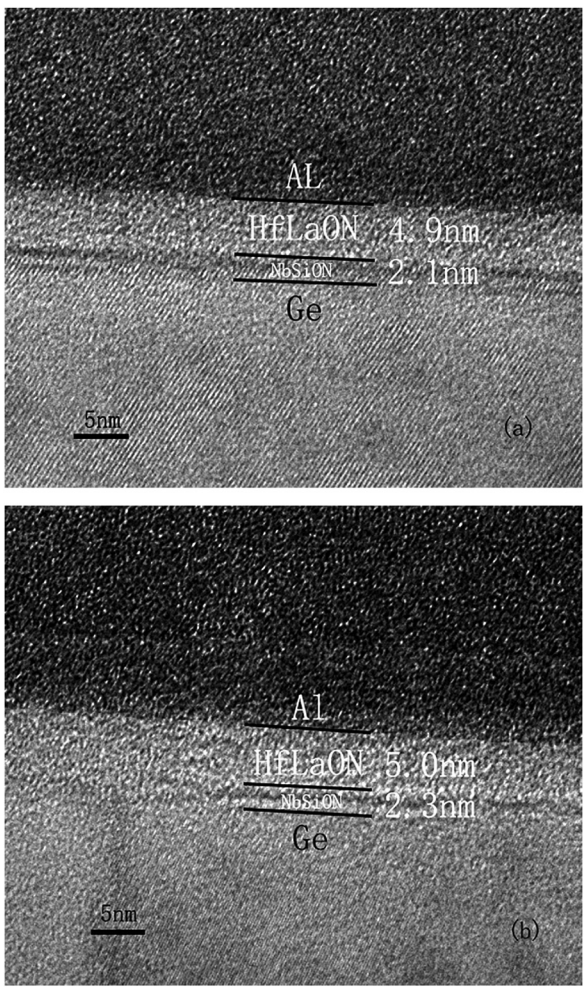

FIG. 1. The cross-sectional TEM images of (a) NbSiON + F sample and (b) NbSiON sample.

Fig. 2(a) shows the typical HF C-V curves of the four samples. Obviously, the control sample has a much smaller accumulation capacitance than the NbSiON + F, NbSiON and NbON samples, implying that a low-k GeO_x interlayer exists in the former but is greatly suppressed in the latter due to the blocking role of the NbSiON or NbON interlayer against the in-diffusion of oxygen and out-diffusion of germanium, as mentioned above. As a result, a stretch out of the C-V curve as well as a small kink in the depletion region is observed for the NbON and control samples in Fig. 2(a), implying a high interface-state density. However, for the NbSiON + F and NbSiON samples, the C-V curve has no distortion occurrence and a large slope from depletion to accumulation, indicating a high-quality NbSiON/Ge interface. Moreover, in Fig. 2(a), a much smaller C-V hysteresis for the NbSiON + F sample (10 mV) and NbSiON sample (32 mV) than the NbON sample (105 mV) and control sample (235 mV) means less slow states or deep-level traps in the former two samples (especially the NbSiON + F sample). The flatband voltage (V_{fb}) of the samples is determined from their flatband capacitance,[24] and equivalent oxide-charge density (Q_{ox}) is calculated as $-C_{ox}(V_{fb} - \varphi_{ms})/q$, with φ_{ms} as the work-function difference between Al and Ge, and C_{ox} as the accumulation capacitance per unit area. The interface-state density near midgap (D_{it}) is estimated from the 1-MHz C-V curve using the Terman's method[25] for the purpose of comparison (Fig. 2(b)). Obviously, the NbSiON + F and NbSiON samples have smaller V_{fb} and D_{it} than the NbON and control samples, with the smallest for the NbSiON + F sample ($V_{fb} = 0.22$ V and $D_{it} = 4.3 \times 10^{11}$ eV^{-1} cm^{-2}). This should be attributed to the fact that the Si interlayer can passivate dangling bonds and absorb the oxygen (forming Si-O bond) diffusing toward the Ge surface, and the F incorporated in the HfLaON/NbSiON stack dielectric by the F plasma treatment can effectively occupy the oxygen vacancies in the NbSiON passivation layer and passivate the traps at/near the interface,[23,26] resulting in a reduction of defect traps in the oxide bulk and at/near the NbSiON/Ge interface. This is further supported by the small frequency dispersion of their C-V curves and small distortion in the depletion region of the 50-kHz C-V curve for the NbSiON + F sample, as shown in Fig. 3. The frequency dispersion in the accumulation region should be attributed to border traps with much larger trapping time constant than the interface traps,[27,28] which leads to a slower electrical response for the former than the latter and thus substantial frequency dispersion of the capacitance in accumulation.[29,30]

The capacitance equivalent thickness (CET) of the gate dielectric is extracted as $CET = k_0 k_{SiO2}/C_{ox}$, where k_0 is the vacuum permittivity, k_{SiO2} is the relative permittivity of SiO_2 and C_{ox} is the measured accumulation capacitance per unit area. Also, the equivalent k value of the gate dielectric is calculated as $k \approx k_{SiO2} T_{ox}/CET$, as also listed in Table I. Obviously, the NbSiON + F sample has the smallest CET (0.98 nm) and largest k value (27.8) due to the fluorine-enhanced suppression of the low-k GeO_x growth, as mentioned above. In addition, the smallest Q_{ox} is obtained for the NbSiON + F sample, followed by the NbSiON sample, indicating the effective blocking capability of both the

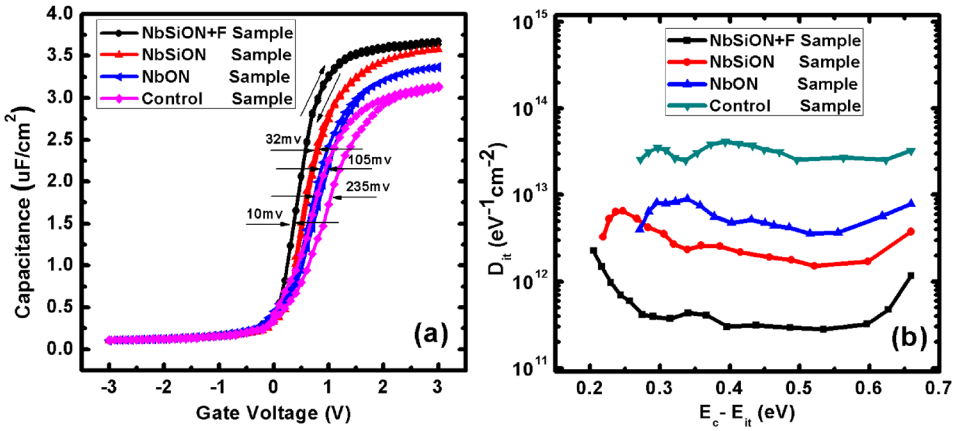

FIG. 2. (a) High-frequency C-V curve and (b) interface-state density (D_{it}) in the bandgap.

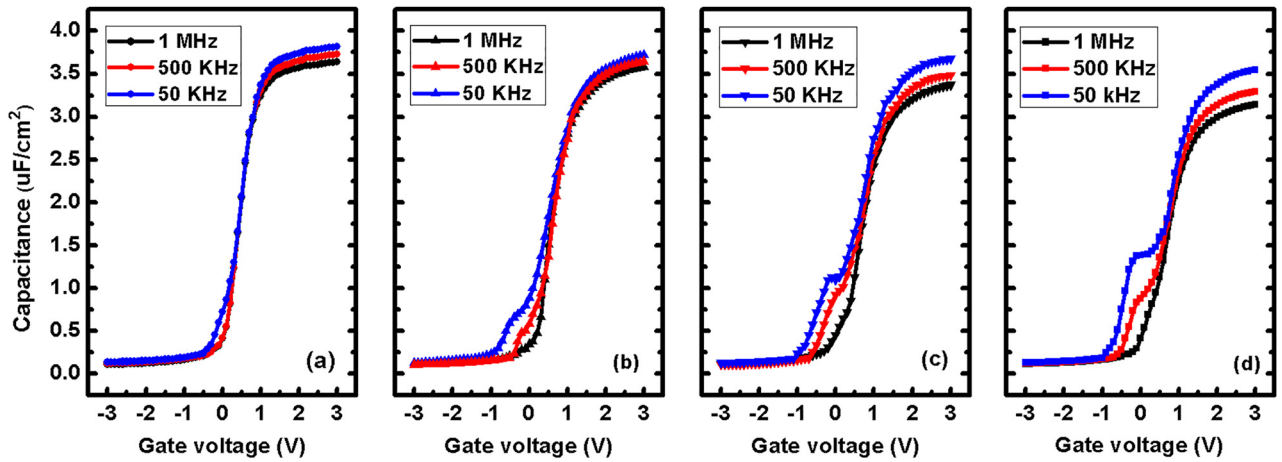

FIG. 3. Frequency dispersion of C-V curves at room temperature: (a) NbSiON + F sample, (b) NbSiON sample, (c) NbON sample, and (d) control sample.

TABLE I. Electrical and physical parameters extracted from HF C-V curves

Sample	NbSiON + F	NbSiON	NbON	Control
C_{ox} (μF/cm^2)	3.53	3.44	3.26	3.13
V_{fb} (V)	0.22	0.35	0.41	0.55
D_{it} (cm^{-2}eV^{-1})	4.3×10^{11}	2.4×10^{12}	8.9×10^{12}	2.53×10^{13}
Q_{ox} (cm^{-2})	-4.45×10^{12}	-7.35×10^{12}	-8.15×10^{12}	-1.02×10^{13}
T_{ox} (nm)	7.0	7.3	7.4	5.9
CET (nm)	0.98	1.01	1.06	1.11
k	27.8	28.1	27.2	20.7

NbSiON interlayer and incorporated fluorine against the inter-diffusion of elements.[31]

In Fig. 4, the NbSiON + F sample has the lowest gate-leakage current among the four samples (e.g., at $V_g = V_{fb} + 1$ V, $J_g = 4.18\times10^{-5}$ A/cm^2, 1.69×10^{-4} A/cm^2, 8.64×10^{-4} A/cm^2, and 4.49×10^{-3} A/cm^2 for the NbSiON + F, NbSiON, NbON, and control samples, respectively), which is closely related to its smallest D_{it} and Q_{ox} due to the absence of the unstable GeO_x interlayer and the suppressed intermixing between the Ge substrate and high-k dielectric,[32,33] greatly weakening the trap-assisted tunneling effect of carriers. Moreover, an effective stress field of 21 MV/cm [$= (V_g - V_{fb})$/CET] is applied for 3600 s to examine the reliability of the devices. Fig. 5 shows the $J_g - V_g$ properties of the devices measured before and after the stressing. The increase in gate leakage current for the four samples after the

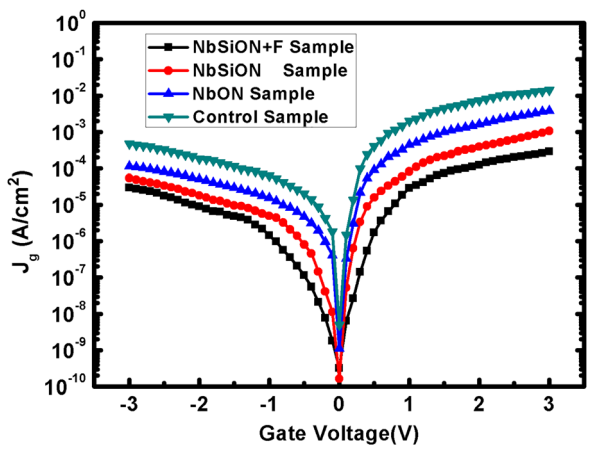

FIG. 4. Gate leakage current density vs. gate voltage (J_g-V_g) characteristics of the four samples.

stressing is due to the trap-assisted tunneling of electrons from the substrate to the gate via newly-generated interface and near-interface traps. Obviously, the NbSiON + F sample has the smallest post-stress leakage current increase, which can be related to the less generation of interface and near-interface traps during the stressing since F tends to segregate to the HfLaON/NbSiON and the NbSiON/Ge interfaces to passivate oxide traps and interface traps by forming stronger Hf-F and F-Si bonds, thus leading to less unstable GeO_x at/near the NbSiON/Ge interface.[34] These stronger bonds can improve the

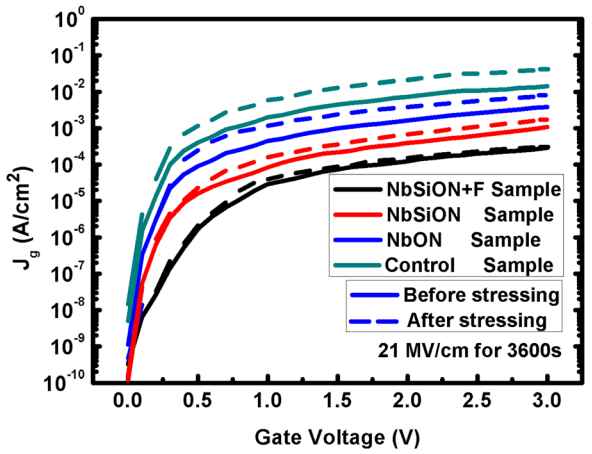

FIG. 5. Gate leakage current density of the samples before and after an effective stress field of 21 MV/cm for 3600 s.

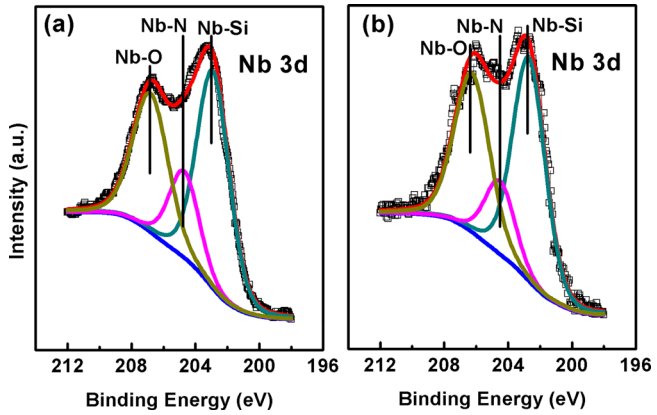

FIG. 7. Nb 3d XPS spectrum in the NbON/Si interlayer. (a) NbSiON + F sample and (b) NbSiON sample.

hot-carrier immunity of the dielectric, resulting in less interface-state generation and positive-charge trapping.[35]

To study the composition and chemical status of the high-k dielectric and passivation interlayer and further analyze the effects of NbSiON on the chemical states of the interface between HfLaON and Ge, the HfLaON film is etched to a distance of ~5 nm above the Ge surface using an in-situ Ar^+ ion beam in the XPS chamber. Fig. 6(a) shows the Si 2p XPS spectrum of the NbSiON + F and NbSiON samples. As compared to the NbSiON sample, the Si 2p peak of the NbSiON + F sample shifts by an energy of 1.45 eV, which should be contributed to the higher electronegativity of F (4.0) than that of O (3.5). Furthermore, Si-O, Si-N and Si-Nb are found at 104.1 eV, 103.1 eV, and 100.7 eV, respectively,[20,36] in Fig. 6(a), indicating that all Si has been consumed and the NbSiON interfacial passivation layer (IPL) has been formed, consistent with the TEM results in Fig. 1. Similarly, the Nb 3d peak of the NbSiON + F sample also shifts to higher energy relative to that of the NbSiON sample, as shown in Fig. 7(a); the Nb-O, Nb-N, and Nb-Si are founded at 206.9 eV, 204.9 eV, and 203.1 eV, respectively,[19,37] from which the content of Nb-O bond for the NbSiON + F and NbSiON samples is calculated to be 41.0% and 48.2%, respectively, based on the Nb-O/Nb3d peak-area ratio. This implies that the fluorine incorporation can block the oxygen diffusion in the dielectric layer towards the substrate surface. Similarly, the content of Nb-Si bond for the NbSiON + F and NbSiON samples is extracted to be 37.2% and 34.5%, respectively, based on the Nb-Si/Nb3d peak-area ratio, implying that the silicon passivation layer is consumed during the subsequent deposition and PDA. Furthermore, the obvious F 1s peak in the F 1s spectrum of the NbSiON + F sample [Fig. 6(c)] indicates that fluorine is indeed incorporated in both the gate dielectric and the passivation layers, resulting in an effective passivation on the dangling bonds and oxide traps at/near the high-k/Ge interface. This is why the NbSiON + F sample has the best interfacial and thus electrical properties, as shown in Table I.

To further analyze the Ge oxides or oxynitride at/near the interface, the XPS spectrum of Ge 3d for the three samples is shown in Fig. 8. As can be seen, the Ge-O, Ge-N, Ge-O_x, Ge $3d_{3/2}$, Ge$3d_{5/2}$, and Ge-Si bonds are found at 32.4 eV, 32.0 eV, 30.6 eV, 29.8 eV, 29.3 eV, and 26.8 eV, respectively,[38–40] demonstrating that there exist GeO_2, GeON, and GeO_x at or near the NbSiON/Ge interface. However, it is worth noting that the content of GeO_x is obviously lower for the NbSiON + F sample (1.4% from the GeO_x/Ge3d peak-area ratio) than the NbSiON sample (4.1%), and similarly, the content of GeO_2 is lower for the NbSiON + F sample (1.1% from the GeO_2/Ge3d peak-area ratio) than the NbSiON sample (3.0%). On the contrary, the content of GeON is higher for the NbSiON + F sample (2.2% from the GeON/Ge3d peak-area ratio) than the NbSiON sample (1.2%). These results indicate that fluorine incorporation can further reduce the oxide traps and block the inter-diffusion of elements near the interface, resulting in the best interface quality and thus electrical properties, as shown for the NbSiON + F sample above.

The effects of NbSiON passivation interlayer and fluorine-plasma treatment on the interfacial and electrical

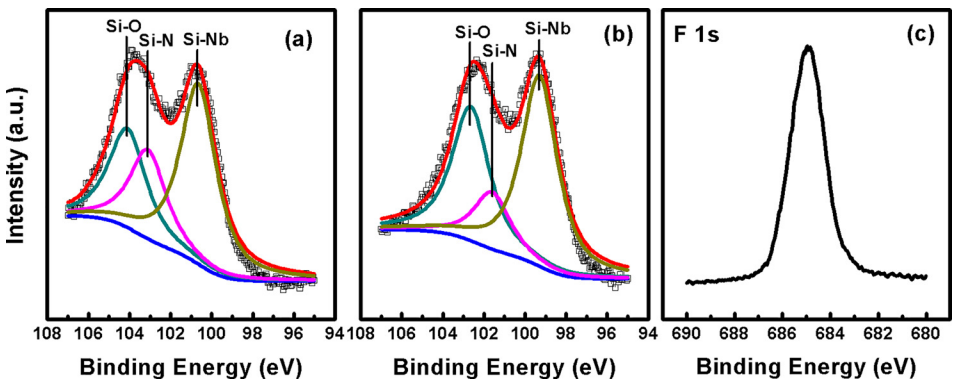

FIG. 6. Si 2p XPS spectrum in the NbON/Si interlayer: (a) NbSiON + F sample, (b) NbSiON sample, and (c) F 1s XPS spectrum of the NbSiON + F sample.

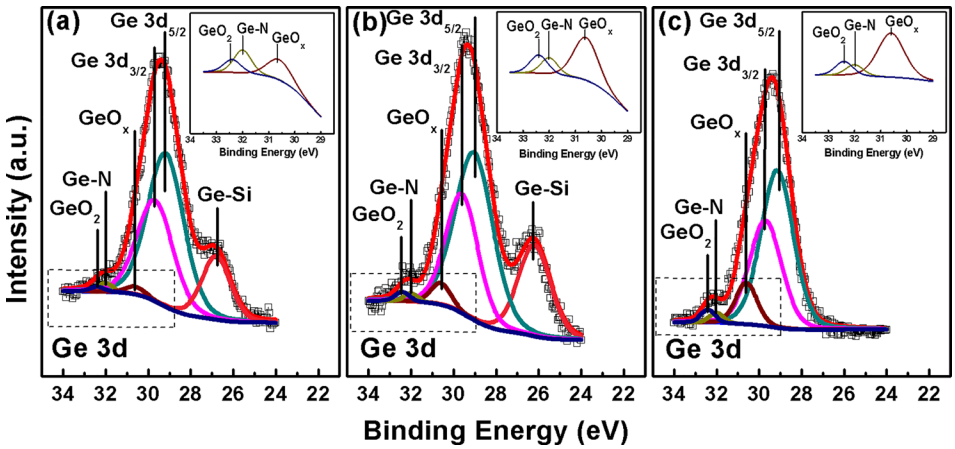

FIG. 8. Ge 3d XPS spectrum at/near the high-k/Ge interface of: (a) NbSiON + F sample, (b) NbSiON sample, and (c) NbON sample. The inset shows the enlarged peaks of Ge oxides.

properties of Ge MOS capacitor with HfLaON gate dielectric are investigated. Measured results show that the Ge MOS devices with NbSiON interlayer have less interface state and oxide charges, which can be further reduced by fluorine incorporation. The XPS analysis indicates that the NbSiON passivation layer can effectively suppress the growth of unstable native oxides at the Ge surface, and also fluorine incorporation can suppress the inter-diffusion of elements and reduce the oxide traps at/near the high-k/Ge interface, thus giving good electrical properties to the Ge MOS device. Therefore, the NbSiON interlayer combined with the fluorine-plasma treatment is a promising way for improving the interface quality and thus obtaining high-performance Ge MOS devices.

This work is financially supported by the National Natural Science Foundation of China (Grant Nos. 61274112, 61176100, and 61404055), the University Development Fund (Nanotechnology Research Institute, 00600009) of the University of Hong Kong and the Hong Kong Polytechnic University (Project No. 1-ZVB1).

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