All-optical add-drop node for optical packet-switched networks

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We have demonstrated all-optical packet add-drop for all-optical packet-switched networks. Intelligent alloptical add-drop of packets is performed, based on all-optical processing of packet headers. The header and payload rates are 5 and 10 Gbits/s, respectively. © 2005 Optical Society of America *OCIS codes:* 230.1150, 190.1450, 140.3520.

All-optical add-drop nodes will be important components of future high-bit-rate optical networks. Most add-drop nodes demonstrated to date convert the packet address headers into electrical signals for processing.¹ Recently we demonstrated an all-optical add-drop node for packet-switched networks that uses two-stage injection-locked Fabry-Perot laser diodes (FP-LDs).² Although the packet-drop function is carried out based on all-optical processing of the packet headers, the packet-add function was implemented by a delay line without header processing. We propose and demonstrate an all-optical add-drop node in which both add and drop of the packets are carried out based on the outcome of all-optical processing of the packet headers. To improve the switching performance we use semiconductor optical amplifiers (SOAs) rather than FP-LDs to achieve the alloptical on-off switches that are used in the add-drop node.

Figure 1 is a schematic of the architecture of the proposed all-optical add-drop node for optical packetswitched networks. Here we assume that the network is slotted. The solid and dashed curves represent data signal wavelength (λ_d) and control signal wavelength (λ_c), respectively. The timing diagrams of the signals at the locations labeled (a) to (j) in Fig. 1 are shown in Fig. 2. The node has four ports; they are the input, the output, the add, and the drop ports as shown in Fig. 1. The node comprises an all-optical header processor (AOHP) and two identical alloptical on-off switches, AOS-1 and AOS-2 (Fig. 1). The add-drop node operates as follows: Data packets at λ_d from the input port are split into two parts. One part of the input data packets is injected into the AOHP, together with a control signal at λ_c . If the address header of a data packet matches that of the control signal, the AOHP will (i) allow the data packet to transmit to the drop port, (ii) send a control signal to AOS-1 to block the other part of the data packet from transmitting to the output port, and (iii) send another control signal to AOS-2 to allow a local packet at the add port to transmit to the output port. If the address of a data packet does not match that of the control signal, the AOHP will (i) block the data packet from transmitting to the drop port, (ii) send a control signal to AOS-1 to allow the other part of the data packet to transmit to the output port, and (iii) send another control signal to AOS-2 to block the local packet at the add port. The two control signals sent from the AOHP to AOS-1 and AOS-2 are logical complements of each other.

We implemented the AOHP by using the bistability characteristic and the multimode injection-locking property of FP-LDs. We have shown that, when a special two-level control signal is used, a single bit at the data packet address can initiate and sustain injection locking of the FP-LD at either λ_c or λ_d for the entire length of the packet.^{3–5} In the current application we used the position of a single 0 bit in the data packet address to designate a node.^{5,6} By this choice of address format, the AOHP will be injection locked at λ_d if the data packet address matches that of the control signal. Thus the AOHP output at λ_d will be high and that at λ_c low. The AOHP will be injection locked at λ_c otherwise; in that case the AOHP output at λ_d will be low and that at λ_c will be high. It is important to note that, even when the AOHP is injection locked by one of the signals, the other signal can still transmit through the AOHP, albeit at a reduced output power level. We chose the powers and detunes of the data signals and control signals such that the



Fig. 1. Schematic of the proposed all-optical add-drop node. Solid and dashed curves represent data signal wavelength (λ_d) and control signal wavelength (λ_c) , respectively. Labels (a)–(j) correspond to those in the timing diagrams in Fig. 2.



Fig. 2. (a)–(d) Synchronized timing diagram at the AOHP: (a) input data packets, (b) input control signal, (c) aligned headers of both input packets and input control signal, switched data packets at (d)(1) 3 ns/division and (d)(2) 1 ns/division. (e)–(j) Synchronized timing diagrams at AOS-1 and AOS-2: (e) local data packets [same as (a) in this demonstration], (f) switched control signal from the AOHP output (OCS_{λc}), (g) switched local data packets from AOS-2 (add port), (h) switched control signals from the AOHP output (OCS_{λd}), (i) switched data packets at the output of AOS-1, (j) data packets at the output port of the node.

states of polarization of the AOHP output at λ_c when the AOHP is injection locked at λ_c are different from those when the AOHP is injection locked at λ_d . As a result, by using polarizers we can obtain two synchronized but logically complementary output control signals from the AOHP, as required in this implementation of the add-drop node. We call the output control signals (OCSs) of the AOHP, when it is injection locked at λ_c and λ_d , $OCS_{\lambda c}$ and $OCS_{\lambda d}$, respectively; the subscripts refer to the wavelengths at which the AOHP is injection locked. The AOHP thus serves as an all-optical on-off switch for the drop port and also a generator for the two logically complementary control signals. We implemented AOS-1 and AOS-2 by using the cross-gain modulation properties of SOAs. The all-optical switch transmits a data packet if the input control signal is low but blocks a data packet if the input control signal is high.

Figure 3 shows the experimental setup of the alloptical packet add-drop node. A single FP-LD serves as the AOHP. The data packets at 1542.76 nm are generated by external modulation of a tunable laser (TL-1) with a 10 Gbit/s nonreturn-to-zero pulse pattern generator and a LiNbO₃ modulator. Four types of packet are used, with header addresses 0111, 1011, 1101, and 1110 for packets pk-1, pk-2, pk-3, and pk-4 intended for nodes 1, 2, 3, and 4, respectively (Fig. 2). The data rates for the header and the payload are 5 and 10 Gbits/s, respectively. The data packets are injected into both the input port and the add port of the node as data packets already in the network as well as local data packets to be placed into the network. The control signals at 1540.16 nm are generated with a 10 Gbit/s non-return-to-zero pulse pattern generator, a 660 MHz pulse pattern generator, and two 10 Gbit/s LiNbO3 modulators on the output of a tunable laser (TL-3; Fig. 3) with 5.9 dBm injected power and +0.22 nm wavelength detuning. The header of the two-level control signal contains the address 0100, the complement of the address of pk-2. Thus



Fig. 3. Experimental setup: TL-1–TL-4,—tunable lasers; EDFA, erbium-doped fiber amplifier; TBPF, tunable bandpass filter; ODL, variable optical delay line; PC, polarization controller; PBC, polarization beam combiner; MOD, modulator; CIR, circulator; PD, photodetector. Other abbreviations defined in text.

only pk-2 will be dropped to the node. Figures 2(a)-2(d) show synchronized timing diagrams for the signals at the AOHP: Fig. 2(a) shows the input data packets; Fig. 2(b) is the input control signal; Fig. 2(c) shows the aligned headers of the input data packets and control signal; and in Fig. 2(d) the switched data packets are shown (1) 3 ns/division and (2) 1 ns/division. We note that at only pk-2 is successfully switched to the drop port. The output of the FP-LD filtered at the control-signal wavelength

fully switched to the drop port. The output of the FP-LD filtered at the control-signal wavelength (1540.16 nm) is then split into two parts and injected into two different SOAs, which serve as switches AOS-1 and AOS-2 with cross-gain modulation. The other parts of the original data signals are further split into two parts and injected into the two SOAs. Figures 2(e)-2(j) show the timing diagrams for switches AOS-1 and AOS-2: Figure 2(e) shows the data at the input AOS-2 (the add port); Fig. 2(f) shows the input control signals to switch AOS-2 $(OCS_{\lambda c})$, which allow only local packets from the add port to pass through if there are packets dropped from the network. In this demonstration we chose to allow pk-2 in the add port to transmit for convenience in synchronization. We can make AOS-2 transmit any one of the four packets by adjusting the delay in the input data signal. Figure 2(g) shows the output of AOS-2 at the data wavelength (1542.76 nm). Note that only pk-2 is allowed to pass through. Figure 2(h) shows the input control packets to switch AOS-1 $(OCS_{\lambda d})$, which performs the clear-packet function for the output port of the node. Figure 2(i) shows the output of switch AOS-1 at data wavelength (1542.76 nm). Note that pk-2 is blocked such that the dropped packet is successfully cleared from the data signal. Figure 2(j) shows the combined output from switches AOS-1 and AOS-2 that has passed through a polarization beam combiner. We intentionally offset the output of switch AOS-2 (the add port) to demonstrate that the add function is properly implemented. We used a polarization beam combiner to eliminate the interference noise when two signals were combined at the same wavelengths.

We have successfully demonstrated an all-optical add-drop node that can perform on-the-fly header processing, packet clearance, and packet add-drop by use of an injection-locked Fabry-Perot laser diode as an all-optical header processor and two semiconductor optical amplifiers as all-optical on-off switches. The header rate is 5 Gbits/s, and the data rate is 10 Gbits/s. The node adds packets to the data signals in the network only when empty slots are available. The add-drop function can be used in construction of a unidirectional bus or ring network. To prevent differentiating an empty time slot from an occupied time slot, we define the addresses of empty packets such that they are accepted by all the nodes in the network. In addition, a node will continue to transmit empty packets even if it has nothing to send. As a result, each node is continuously accepting empty packets from the node upstream and sending empty packets to the node downstream even if there are no user data packets in the network. By this construction, the task of separating empty slots from those that contain user information sent from other nodes is pushed to the local node, thus eliminating the optical signal-processing requirement of the proposed add-drop node.

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