Investigation of Ge nanocrytals in a metal-insulator-semiconductor structure with a HfO$_2$/SiO$_2$ stack as the tunnel dielectric

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A metal-insulator-semiconductor (MIS) structure containing a HfO$_2$ control gate, a Ge nanocrystal-embedded HfO$_2$ dielectric and a HfO$_2$/SiO$_2$ stack layer as tunnel oxide, was fabricated by an electron-beam evaporation method. High-resolution transmission electron microscopy study revealed that the HfO$_2$/SiO$_2$ stack layer minimized Ge penetration, leading to the formation of Ge nanocrystals that are self-aligned between the tunnel oxide and the capping HfO$_2$ layer. Influence of different annealing conditions on the formation and distribution of Ge nanocrystals was studied. Current–voltage (I–V) and capacitance–voltage (C–V) measurements revealed promising electrical characteristics of the MIS structure, and relatively high stored charge density of 10^{12} cm^{-2} was achieved. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1864254]

Recently, much efforts have been made to improve the device performance of nanocrystal memory by replacing the SiO$_2$ with various dielectrics such as oxynitride,[1] Al$_2$O$_3$,[2,3] ZrO$_2$,[4] and SiN$_x$.[5,6] King *et al.*[7] demonstrated that a Ge nanocrystal memory device can be programmed at a relatively low voltage and high speed. In our previous work, electric characteristics, and the negative photoconductivity of Ge nanoclusters embedded in Al$_2$O$_3$ or in ZrO$_2$/Al$_2$O$_3$ gate dielectrics have been investigated.[2,4] Considerable attention is now being paid to HfO$_2$[8–10] as a gate dielectric due to its relatively high dielectric constant (high-k), large band-gap and proper band-offset. Results indicated that the use of high-k dielectric on Si as a tunnel layer offers a lower electron barrier height at the dielectric/Si interface and larger physical thickness, resulting in faster programming and longer retention than is found in a conventional SiO$_2$ tunnel layer.[9] Unfortunately, interfacial oxides, silicates and silicides were often observed during film deposition or subsequent annealing,[11–13] and thus strongly affect the memory device's performance and leads to unstable channel mobility and threshold voltage. Ng *et al.*[14] reported earlier the penetration of Ge through the rapid thermal oxide layer into the

silicon substrate and consequently the absence of hysteresis in the capacitance–voltage (C–V) curves. By implementing a silicon nitride/HfO$_2$ stack as a tunnel dielectric, Ge penetration was suppressed and an excellent C–V hysteresis has been achieved. However, Ge nanocrystals were not uniform distributed and pronounced as illustrated by the transmission electron microscopy (TEM) images. In this letter, we report the implementation of the HfO$_2$/SiO$_2$ stack layer as a tunnel oxide and the formation of uniform Ge nanocrystals, thus improved charge-storage effects.

The HfO$_2$/HfO$_2$+Ge/HfO$_2$/SiO$_2$/Si structure was deposited by high vacuum electron-beam evaporation at room temperature on hydrofluoric acid treated p-type (100) silicon at room temperature. First, a SiO$_2$ film with a thickness of 4 nm was deposited on silicon substrate, and a 3 nm-thick HfO$_2$ film was deposited subsequently. The HfO$_2$/SiO$_2$ stack structure was used as tunneling oxide layer. A HfO$_2$+Ge (HfO$_2$:Ge=5:2) film with a thickness of 8 nm was codeposited on the HfO$_2$ film as a floating gate layer. Finally, the capping HfO$_2$ film with a thickness of 40 nm was deposited. After deposition, the samples were annealed at 600–800 °C for 30–45 min in N$_2$ ambient. Metal electrodes were formed by the evaporation of aluminum. As a comparative experiment, a single layer of HfO$_2$ was also used as tunnel oxide
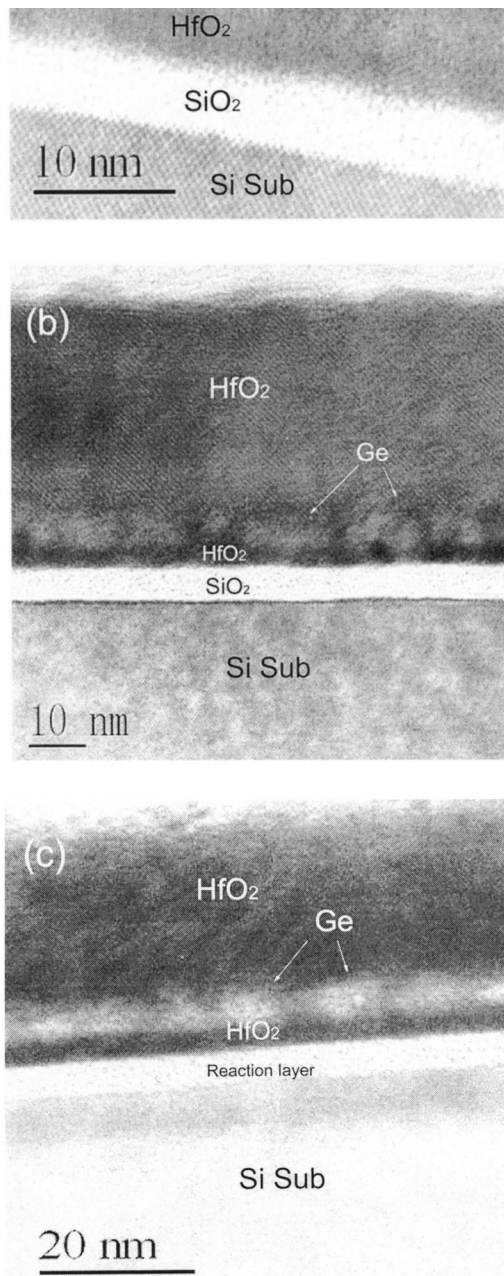
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FIG. 2. Leakage current characteristics of the MIS structures: (a) with a HfO_2/SiO_2 stack tunnel layer annealed at 600 °C for 30 min; (b) with a HfO_2/SiO_2 stack tunnel layer annealed at 800 °C for 45 min; (c) with a HfO_2 tunnel layer only and annealed at 800 °C for 45 min.

This result is similar to that of Si nanocrystals embedded in SiO_2 reported earlier by Ho and co-workers.[15] We believe that the formation of Ge nanocrystals is a physical process containing nucleation and growth, so that an optimized annealing condition is essential for the formation of Ge nanocrystals with the proper size and density. We also believe that the size of nanocrystals can be controlled by varying the thickness of the $HfO_2 + Ge$ mixed layer.

Figure 1(c) is a HRTEM image showing the stack structure using a single 6-nm-thick HfO_2 tunnel layer, which was annealed at 800 °C for 45 min. Uniformly distributed and pronounced Ge nanocrystals with an average size of 6 nm can be clearly seen. However, during the high temperature annealing, a SiO_2 interfacial layer was also formed.

Figure 2 exhibits the $I-V$ characteristics of different samples. As shown Fig. 2(a), the sample with the stack tunnel layer and annealed at 600 °C for 30 min shows the lowest leakage of current. However, the sample annealed at 800 °C for 45 min possesses a larger leakage of current, as shown in Fig. 2(b). The well-crystallized HfO_2 film, as illustrated in Fig. 1(b), may provide channels for the leakage of current. Nevertheless, the amorphous SiO_2 layer ensures the low leakage current. The leakage current of the sample with single HfO_2 tunnel oxide is relatively large, even with the presence of an amorphous layer of SiO_2 post-annealing formed. This may be due to the lack of oxygen in the formed SiO_2 layer (in fact it is SiO_{2-x}), that results in a higher leakage of current.

The charge-storage characteristic of the Ge nanocrystals was characterized by means of a high-frequency (1 MHz) $C-V$ measurement of the MIS structure. It revealed that all of the samples possess counterclockwise hysteresis $C-V$ loops. As a rough estimation, the width of the $C-V$ hysteresis can be determined by the number of charges stored in the Ge nanocrystals. In Fig. 3(a), the maximum hysteresis width is obtained in the sample annealed at 600 °C for 30 min, suggesting maximum nanocrystal density. As the annealing temperature increases further to 800 °C, the hysteresis width (ΔV_{FB}) decreases, suggesting a decrease of nanocrystals density due to the agglomeration of Ge nanocrystals. This result is similar to that of the Ge nanocrystals embedded in SiO_2 as reported earlier by Kim *et al.*[16] Another reason for the reduction of ΔV_{FB} may be attributed to the trapping of electrons or holes in the gate dielectrics and interfaces

FIG. 1. Cross-sectional HRTEM images of the MIS structure with Ge nanocrystals embedded in HfO_2 dielectric with a HfO_2/SiO_2 stack tunnel layer annealed at 600 °C for 30 min (a), and annealed at 800 °C for 45 min (b); (c) with a HfO_2 tunnel layer only and annealed at 800 °C for 45 min.

for the floating gate structure. Ge nanocrystals and interfacial structures were investigated by high-resolution transmission electron microscopy (HRTEM), and the charge storage effect of the MIS structure was characterized by capacitance–voltage ($C-V$) and leakage current measurements.

Figure 1(a) shows the HRTEM image of the $HfO_2/HfO_2 + Ge/HfO_2/SiO_2/Si$ stack structure, which was annealed at 600 °C for 30 min. It can be seen that the interfaces between the Si/SiO_2 and SiO_2/HfO_2 are fairly sharp. Ge nanocrystals can also be identified in the image, even though the layer is somewhat continuous. After being annealed at 800 °C for 45 min, it is apparent, as shown in Fig. 1(b), that the self-aligned Ge nanocrystals with diameters of around 10 nm are much more pronounced compared to Fig. 1(a). It is worthy noting that all of the Ge nanocrystals are located between the HfO_2 tunnel layer and the capping layer.
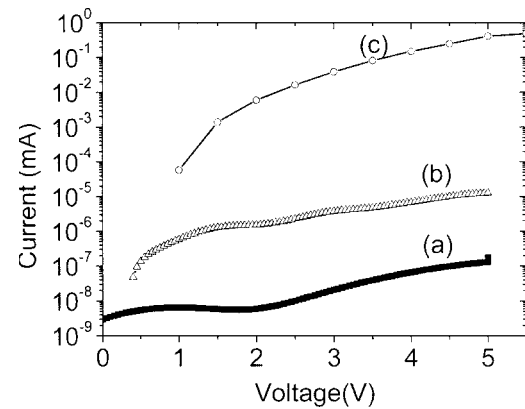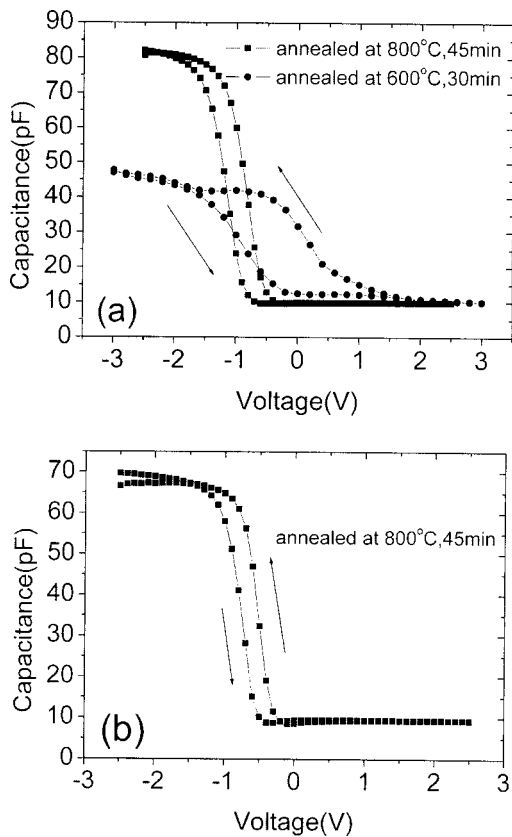
FIG. 3. High-frequency (1 MHz) $C-V$ characteristics of the MIS structures: (a) with a HfO$_2$/SiO$_2$ stack layer as tunnel oxide, and (b) with a HfO$_2$ tunnel layer only.

caused by high temperature annealing.[5] The samples annealed at 600 °C for 30 min (ΔV_{FB}=0.98 V and C_{ox}=46.28 pF) and at 800 °C for 45 min (ΔV_{FB}=0.34 V and C_{ox}=81.34 pF) possess the stored charge densities of 2.3 and 3.3$\times 10^{12}$ cm^{-2}, respectively, as calculated using the formula:[17–19]

$$N = C_{ox}\Delta V_{FB}/qt_{ratio}, \tag{1}$$

where C_{ox} is the oxide capacitance and ΔV_{FB} is the flat-band voltage shift. The factor, t_{ratio} is the thickness ratio of $(t_{gateox}+0.5D_n)/t_{total}$. t_{gateox}, D_n, and t_{total} are the thickness of the cap gate oxide, the nanocrystal diameter and the total thickness of the MIS structure, respectively. Though the sample annealed at 600 °C for 30 min has the largest ΔV_{FB}, its small slope may be attributed to a significant amount of discharging that occurred concurrently with either the charging of holes or electrons,[15] suggesting that it may have a poorer charge retention capability than the other samples. In fact, the continuous nature of the Ge nanocrystals in the sample annealed at 600 °C for 30 min should be responsible for charge loss through lateral paths.

The $C-V$ characteristics of the sample with only a HfO$_2$ tunnel oxide layer is shown in Fig. 3(b). Though we can still observe the hysteresis in $C-V$ curves (ΔV_{FB}=0.28 V and C_{ox}=67 pF), there is an unexpected distortion in the curve

due to the poor quality of the SiO$_2$ tunnel oxide mentioned before. By formula (1), we can also approximately calculate the stored charge density in the sample, i.e., 1.48 $\times 10^{12}$ cm^{-2}, which revealed that the sample with a HfO$_2$/SiO$_2$ stack layer as tunnel oxide has a better capability to store charges.

In conclusion, we have fabricated the HfO$_2$/HfO$_2$ +Ge/HfO$_2$/SiO$_2$/Si structure through high vacuum electron-beam evaporation at room temperature. It has been revealed that the HfO$_2$/SiO$_2$ stack tunnel layer minimizes the Ge penetration into the Si substrate and therefore, uniform and self-aligned Ge nanocrystals can be formed between the tunnel oxide and the capping HfO$_2$ layer, leading to an excellent charge storage capability and an extremely low leakage current. We have also shown that it is possible to control the size and the distribution of the Ge nanocrystals through proper annealing conditions.

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