Memory effects of carbon nanotubes as charge storage nodes for floating gate memory applications

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A nonvolatile flash memory device has been fabricated using carbon nanotubes (CNTs) as a floating gate embedded in HfAlO (the atomic ratio of Hf/Al is 1:2) high-k tunneling/control oxides and its memory effect has been observed. Capacitance-voltage (C-V) measurements illustrated a 400 mV memory window during the double C-V sweep from 3 to −3 V performed at room temperature and 1 MHz. Further studies on their programming characteristics revealed that electron is difficult to be written into the CNTs and the memory effect of the structures is mainly due to the holes traps. The memory window width can remain nearly unchanged even after 10^4 s stressing, indicating excellent long term charge retention characteristics. We therefore suggest that the CNTs embedded in HfAlO can be potentially applied to floating gate flash memory devices. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2179374]

Since their discovery in the early 1990s,[1] carbon nanotubes (CNTs) have attracted much attention, both of scientific and technological interest, for possible nanoelectronic applications. To date, a number of nanoelectronic devices have been realized with CNTs, such as field effect transistors,[2–4] room-temperature single-electron transistors,[5] logic gate circuits,[6] inverters,[7] and electromechanical switches.[8] Very recently, the prototypes of memory devices based on CNT field effect transistors were also reported,[9–12] demonstrating another significant extension of CNTs applications. From then on, several groups have carried out research on the CNT-based memories.[13–17] In these research works, the CNTs were synthesized on a conductive Si substrate capped by several hundred nanometers of SiO_2. Metal electrodes were evaporated on the CNTs to form source and drain electrical contact to them. The conductive Si substrate actually acts as the gate of the memory device. The function of the CNTs was the current channel, and the memory effect of the devices was attributed to the charges injected from the CNTs to the defects or charge traps in the dielectrics or the interface between the CNTs and the oxides.[15–17] The CNTs were not used as the charge storage nodes.

For commonly studied flash memory devices, Si,[18] Ge,[19] and $Si_{1-x}Ge_x$ (Ref. 20) nanocrystals are widely used as the charge storage nodes and the memory structures are sandwiched with nanocrystals embedded in the SiO_2 or high-k dielectrics. But up to now, there is no report on flash memory devices using CNTs as a floating gate. In terms of electrical properties, CNTs have many unique advantages for the application in memory devices such as tunable band gap, high thermal stability and chemical inertness, perfect sidewall structure, and nearly zero surface states.[21,22] These unique properties are very favorable for their application as the charge storage nodes in the memory devices. In this letter, we report the fabrication of the HfAlO/CNTs/HfAlO/Si memory structures and characterization of the unique memory characteristics of CNTs using as the charge storage nodes. HfAlO was chosen as the tunneling and control oxides in the memory structures due to its promising performance for high-k gate dielectric application[23] and floating gate memory device application.[19]

Before tunneling HfAlO film deposition, the p-Si(100) substrate with a resistivity of 4–6 Ω cm was first etched by a HF (10%) solution for 10 s. Then one very thin layer of HfAlO film was deposited on the Si substrate by the laser molecular beam epitaxy (MBE) technique using a KrF excimer laser (LPX 205i, Lambda Physik, 248 nm in wavelength, 30 ns in pulse width, operated at 1 Hz). The ratio of Hf to Al for the ceramic target is 1:2. The commercial CNTs (purity > 90%) were synthesized by chemical vapor deposition and their diameter and length are about 2 nm and 1.5 μm, respectively. The original powder like CNTs were first dispersed in the acetone solution by ultrasonic method. The estimated density for CNTs in the acetone is around 0.1 mg/ml. After immersing into the CNTs containing acetone solution for 10 s, the Si substrate covered with a layer of HfAlO tunneling oxide was pulled out slowly. Finally, another layer of HfAlO was deposited to cover these CNTs and form the structure of HfAlO/CNT/HfAlO/Si. The base vacuum of the laser MBE system before film deposition is 2×10^{-5} Pa and the oxygen pressure for the deposition of HfAlO films was 0.2 Pa. The growth rate for the HfAlO film is about 2 nm/min. To minimize the interfacial reaction between the HfAlO film and the Si substrate, the deposition substrate temperature was selected to be 400 °C. A control sample with only two layers of HfAlO films with the nominal thickness same as the control and tunneling oxide layers of the memory structure was also prepared. To improve the interfacial quality between the Si substrate and the HfAlO film and between the two layers of HfAlO, all the samples were *in situ* annealed in pure N_2 ambient at an elevated temperature of 700 °C for 30 min. Pt top electrodes with an area of 3.14×10^{-4} cm^2 were deposited on the surface of the samples using a shadow mask. Finally, back contact of silver was used to form the metal-oxide-silicon (MOS) memory structures. The hysteresis loop and the charge retention characteristics of the MOS memory devices were evaluated by capacitance-voltage (C-V) and capacitance-time measure-

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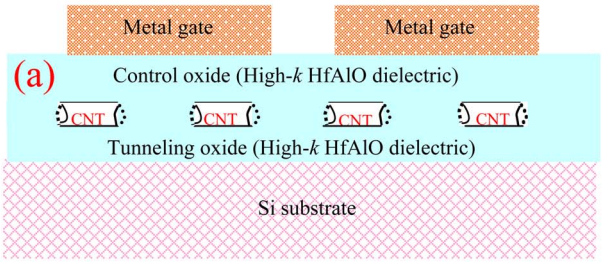

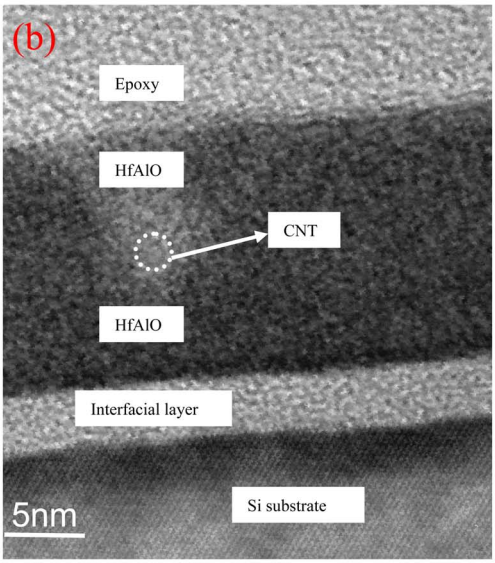

FIG. 1. (Color online) (a) Schematic structure of the HfAlO/CNTs/HfAlO/Si MOS memory structure. and (b) HRTEM image of CNTs embedded in HfAlO control and tunneling layers.

ments with an Agilent 4294A impedance analyzer at room temperature. The cross-sectional structures of the trilayer memory stack were characterized by high-resolution transmission electron microscopy (HRTEM).

The schematic structure of floating gate memory devices using CNTs as floating gate is shown in Fig. 1(a). The *p*-type substrate is designed as the current channel and the CNTs are designed to be embedded in the HfAlO films and act as the charge storage nodes. Figure 1(b) shows the cross-sectional HRTEM images of the actual memory devices, where the bright circle-like regions can be found embedded in the HfAlO film, which are determined to be CNTs. This indicates that the HfAlO/CNT/HfAlO/Si memory structures have been fabricated. It is also apparent that the HfAlO film remains an amorphous structure even after a 30 min N_2 annealing at 700 °C.

To study the charge trapping effect of the samples, double *C-V* sweeps were performed at a high frequency of 1 MHz at room temperature. The gate voltage was swept from inversion to accumulation to obtain the forward high frequency *C-V* characteristics and from the accumulation back to inversion for the reverse *C-V* characteristics. Figure 2 shows the typical *C-V* hysteresis loops of the samples with and without CNTs. A clear hysteresis between subsequent forward and backward *C-V* curves can be observed for the sample containing CNTs. During the voltage sweep range of 3 to −3 V, a memory window width of 400 mV was observed. For the control sample of Pt/HfAlO/Si structures, the backward *C-V* curve nearly overlaps the forward *C-V* curve and no clear hysteresis loop can be observed, indicating that the defects and interfacial states between the control and tunneling oxide or HfAlO/Si have been greatly reduced by postannealing in N_2 ambient. Therefore, it can be concluded that the memory effect of the sample containing CNTs is really due to the incorporation of CNTs into HfAlO dielectrics. This memory window also indicates that a small number of electrons/holes have tunneled into the CNTs and were stored inside. According to Yoneya *et al.*'s report,[12] the CNTs were also suggested to be the charge storage nodes. However, the memory window of their CNTs based flash memory devices was observed only at low temperature. The observation of room temperature memory effect in our CNT based memory devices is most likely due to embedding of CNTs in the HfAlO dielectrics, which makes the trapped charges in the CNTs difficult to tunnel back to the substrate for the high potential barrier between the CNTs and the tunneling HfAlO high-*k* dielectrics.

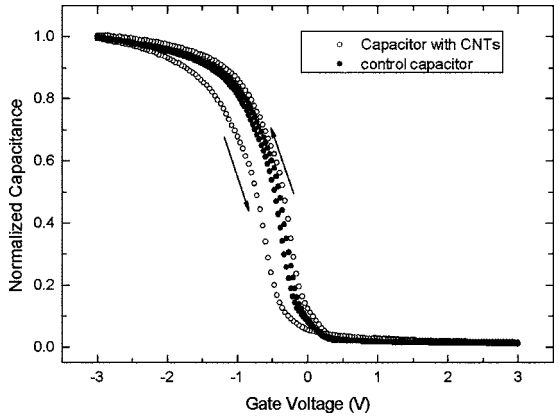

FIG. 2. (Color online) Typical *C-V* hysteresis characteristics of the CNT-based MOS memory devices and the control sample.

The typical programming characteristics of the fabricated CNT based devices under different programming time are shown in Fig. 3. All the flatband voltages in this figure were determined from the forward *C-V* sweep of the voltage range of 2 to −2 V. A positive voltage is generally considered as the programming voltage for the *p*-type flash memory devices using Si, Ge nanocrystals as floating gate. In this letter, a negative charging voltage is also taken for a programming voltage. Figure 3 shows that when a programming voltage of 5 V was applied to the memory devices, the flatband voltage has little change with the increase of the

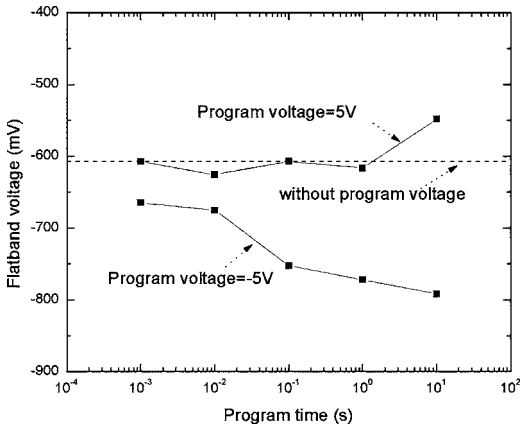

FIG. 3. (Color online) Writing characteristics of the MOS memory devices under different programming time by +5 and −5 V, respectively.

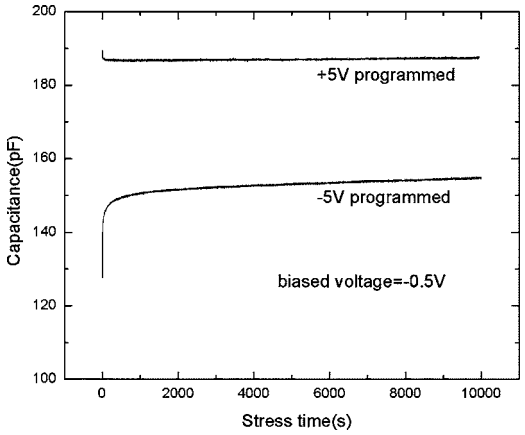

FIG. 4. (Color online) Charge retention characteristics of the CNT-based MOS memory devices using ±5 V programming gate voltages.

programming time, suggesting that electrons are difficult to be *written* into the CNTs even by a long programming time. On the contrary, with the increase of the programming time, a clear increase of the flatband voltage shift can be observed for a negative programming voltage of −5 V, indicating that holes are much easier to be written into the CNTs and are responsible for the memory effect of this kind of memory devices. This result is consistent with the assumption on the hole trapping into the CNTs proposed by Yoneya *et al.*[12]

The charge retention characteristics of the CNTs based memory devices were measured at room temperature after a charging voltage of ±5 V was applied for 1 s. As shown in Fig. 4, the capacitance at the bias voltage of −0.5 V, which is near the flatband point, were monitored as a function of the stressing time. The charge retention characteristics can be divided into two stages. In the first stage, the memory window of capacitance significantly narrows within the first 10^2 s. This quick decrease of the memory window may be due to the lateral charge loss between the CNTs in our structures. Because it is difficult to separate all the CNTs into individual CNT, there always exist some bundles of CNTs or connections between one CNT with another one in neighboring MOS memory devices. Another stage is the long term retention stage. In this stage, excellent long term charge retention characteristics can be observed. The width of the memory window remains nearly unchanged even after 10^4 s stressing.

To explain the excellent charge retention characteristics, we propose the following mechanisms. First, we believe that the excellent retention characteristic is due to the unique structure and electrical properties of the CNTs. To simplify the discussion, we only consider the situation of SWCNT, since the multiwall CNTs are more complicated. As we know, the structure of SWCNTs is one dimensional and the charge carriers in the SWCNTs can only transport along its axis direction.[21,22] Consequently the transport of charge carriers along other directions will be strongly confined. Therefore the charges trapped in the SWCNTs may be difficult to tunnel out. Another important reason may be the nearly perfect surface quality of SWCNTs.[22] Unlike Si and Ge nanocrystals, the SWCNTs have almost no dangling bonds on their surface corresponding to very few or zero surface states. According to the research results of Park *et al.*,[24] the surface states of the Si quantum dots play a very important role in the charge loss of the memory devices. It has also been reported that the charge retention characteristics of the flash memory structures using Si, Ge nanocrystals as floating gate are affected by many other mechanisms, such as the charging characteristics (electron or hole),[25,26] interfacial states between the Si substrate and tunneling oxide,[27] defects and surface states of the nanocrystals,[24] size, shape, and ratio of volume to surface area of the nanocrystals,[27,28] etc. According to the research results in Refs. 25 and 26, memory devices programmed by holes have better retention characteristics than that programmed by electrons due to their higher potential barrier and larger effective mass of holes. Similarly, excellent long term charge retention characteristics can also be expected for the memory structures using CNTs as floating gate due to their hole trapping characteristics as demonstrated in Fig. 3.

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[1] S. Iijima and T. Ichihashi, Nature (London) **363**, 603 (1993).
[2] S. J. Tans, A. R. M. Verschueren, and C. Dekker, Nature (London) **393**, 49 (1998).
[3] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, Science **294**, 1317 (2001).
[4] T. Du1rkop, S. A. Getty, Enrique Cobas, and M. S. Fuhrer, Nano Lett. **4**, 35 (2004).
[5] H. W. C. Postma, T. Teepen, Z. Yao, M. Grifoni, and C. Dekker, Science **293**, 76 (2001).
[6] V. Derycke, R. Martel, J. Appenzeller, and P. Avouris, Nano Lett. **1**, 453 (2001).
[7] X. L. Liu, C. Lee, C. W. Zhou, and J. Han, Appl. Phys. Lett. **79**, 3329 (2001).
[8] T. W. Tombler, C. W. Zhou, L. Alexseyev, J. Kong, H. J. Dai, L. Lei, C. S. Jayanthi, M. J. Tang, and S. Y. Wu, Nature (London) **405**, 769 (2000).
[9] T. Rueckes, K. Kim, E. Joselevich, G. Y. Tseng, C. L. Cheung, and C. M. Lieber, Science **289**, 94 (2000).
[10] M. S. Fuhrer, B. M. Kim, T. Durkop, and T. Brintlinger, Nano Lett. **2**, 755 (2002).
[11] M. Radosavljevic, M. Freitag, K. V. Thadani, and A. T. Johson, Nano Lett. **2**, 761 (2002).
[12] N. Yoneya, K. Tsukagoshi, and Y. Aoyagi, Appl. Phys. Lett. **81**, 2250 (2002).
[13] F. Nihey, H. Hongo, M. Yudasaka, and S. Iijima, Jpn. J. Appl. Phys., Part 2 **41**, L1049 (2002).
[14] A. Star, Y. Lu, K. Bradley, and G. Gru1ner, Nano Lett. **4**, 1587 (2004).
[15] J. B. Cui, R. Sordan, M. Burghard, and K. Kern, Appl. Phys. Lett. **81**, 3260 (2002).
[16] C. H. Lee, K. T. Kang, K. S. Park, M. S. Kim, H. S. Kim, H. G. Kim, J. E. Fischer, and A. T. Johnson, Jpn. J. Appl. Phys., Part 1 **42**, 5392 (2003).
[17] D. J. Yang, Q. Zhang, S. G. Wang, G. F. Zhong, Diamond Relat. Mater. **13**, 1967 (2004).
[18] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, Appl. Phys. Lett. **68**, 1377 (1996).
[19] J. H. Chen, Y. Q. Wang, W. J. Yoo, Y.-C. Yeo, G. Samudra, D. S. H. Chan, A. Y. Du, and D.-L. Kwong, IEEE Trans. Electron Devices **51**, 1840 (2004).
[20] D.-W. Kim, T. Kim, and S. K. Banerjee, IEEE Trans. Electron Devices **50**, 1823 (2003).
[21] P. L. McEuen, M. S. Fuhrer, and H. K. Park, IEEE Trans. Nanotechnol. **1**, 78 (2002).
[22] P. Avouris, J. Appenzeller, R. Martel, and S. J. Wind, Proc. IEEE **91**, 1772 (2003).
[23] P. F. Lee, J. Y. Dai, K. H. Wong, H. L. W. Chan, and C. L. Choy, J. Appl. Phys. **93**, 3665 (2003).
[24] N.-M. Park, S.-H. Choi, and S.-J. Park, Appl. Phys. Lett. **81**, 1092 (2002).
[25] Y. L. Yang and M. H. White, Solid-State Electron. **44**, 949 (2000).
[26] K. Han, I. Kim, and H. Shin, IEEE Electron Device Lett. **21**, 313 (2000).
[27] Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, Jpn. J. Appl. Phys., Part 1 **38**, 425 (1999).
[28] D.-W. Kim, F. E. Prins, T. Kim, S. Hwang, C. H. Lee, D.-L. Kwong, and S. K. Banerjee, IEEE Trans. Electron Devices **50**, 510 (2003).